Modeling the Impact of Random Grain Boundary Traps on the Electrical Behavior of Vertical Gate 3-D NAND Flash Memory Devices

Yi-Hsuan Hsiao, *Student Member, IEEE*, Hang-Ting Lue, *Member, IEEE*, Wei-Chen Chen, Kuo-Pin Chang, Yen-Hao Shih, *Member, IEEE*, Bing-Yue Tsui, *Senior Member, IEEE*, Kuang-Yeu Hsieh, and Chih-Yuan Lu, *Fellow, IEEE*

***Abstract*— The 3-D stacking of multiple layers of NAND using thin-film transistor (TFT) devices is widely accepted as the next step in continuing NAND Flash scaling. Low mobility and reliability problems are two well-known concerns regarding TFT devices. However, another important implication of using TFT devices is that the Vt variation induced by randomly distributed grain boundaries degrades the array performance. In this paper, an extensive TCAD simulation was conducted to systematically investigate how grain boundary generated traps affect NAND Flash devices. Minimizing the density of grain boundary traps is crucial for array performance. In addition, optimal gate control ability reduces the impact of grain boundaries. Thus, using double gate architecture in vertical gate 3-D NAND is favorable. Furthermore, when pitch is scaled in the future, device exhibiting smaller channel thickness should be used to increase the gate control.**

***Index Terms*— 3-D NAND Flash, grain boundary, grain boundary traps, poly Si thin-film transistor (TFT), vertical gate (VG).**

I. Introduction

3-D NAND Flash has attracted great attention in recent years. It overcomes the challenges of pitch scaling limitation faced by conventional 2-D NAND Flash and thus is promising for continuous bit cost scaling without pitch scaling [1], [2]. For 3-D NAND Flash architectures, such as bit-cost scalable, terabit cell array transistor, vertical stack array transistor, and vertical gate (VG) [3], polysilicon material has replaced single crystalline silicon as the channel material. Several critical concerns, such as large variability caused by the random distribution of grain boundaries, lower mobility in the polysilicon channel, and reliability must be addressed [4], [5]. In NAND Flash applications, low mobility is not a critical concern because the large page size compensates for the slow read latency.

Regarding cell distribution, the conductive channel fabricated using polysilicon material in 3-D NAND Flash causes a wider distribution, and larger Vt variability results from the impact of grain boundary and its corresponding traps. Because of the program and erase algorithm, the distribution can be tightened using a well-designed algorithm. Random telegraph noise is enhanced in the conductive channel fabricated using polysilicon material, and its distribution becomes asymmetric after cycling [6]. Regarding temperature sensitivity, a higher temperature causes higher field-effect mobility [7]. However, large variation in thin-film transistor (TFT) device remains a major concern [8]. This is a particular concern in multilevel cell application in which the wide threshold voltage (Vt) distribution caused by the grain boundary traps significantly reduces the memory window.

A previous study demonstrated that the randomly distributed grain boundary traps derived from the imperfect grain-to-grain interface were caused by the creation of dangling bonds [8]. These traps induce a large local band bending and surface potential barrier, and result in poor subthreshold behavior of the TFT device [9]–[12]. The local surface potential barrier from randomly generated grain boundary traps also produces two new effects, gate-induced grain barrier lowering (GIGBL) and drain-induced grain barrier lowering (DIGBL). As a follow-up on a previous study, a TCAD simulator, Sentaurus, was used to simulate the impact of randomly distributed grain boundary traps on cell performance. A forward and reverse read method to distinguish the grain boundary, which strongly affects the cell performance, was then used. After elucidating the impact of grain boundary and its specific grain boundary traps, various crucial device parameters, such as channel thickness and grain boundary traps, were also examined.

II. Device Description

Previous studies, including the experimental and simulation results, have determined that broadened cell distribution and degraded device performance are caused by the impact of a randomly distributed grain boundary location and its specific

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Y.-H. Hsiao is with Macronix International Company, Ltd., Hsinchu 300, Taiwan, and also with the Department of Electrical Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: falahsiao@mxic.com.tw).

H.-T. Lue, W.-C. Chen, K.-P. Chang, Y.-H. Shih, K.-Y. Hsieh, and C.-Y. Lu are with Macronix International Company Ltd., Hsinchu 300, Taiwan (e-mail: htlue@mxic.com.tw; weichenchen@mxic.com.tw; kpchang@mxic.com.tw; yhshih@mxic.com.tw; kenhsieh@mxic.com.tw; cylu@mxic.com.tw).

B.-Y. Tsui is with the Department of Electrical Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: bytsui@mail.nctu.edu.tw).

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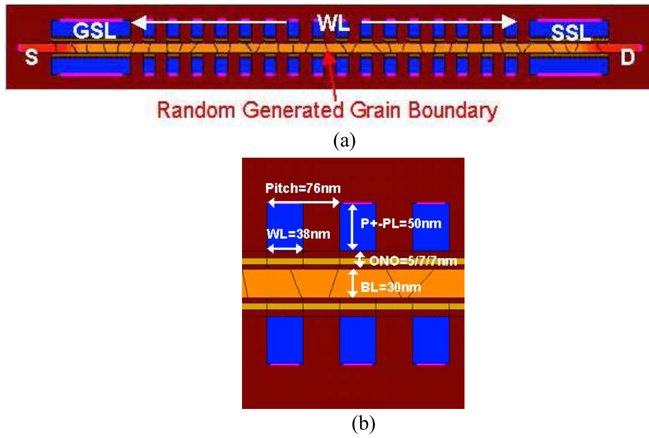


Fig. 1. (a) Schematic architecture of the junction-free DG NAND Flash devices for 2-D simulated with 38-nm half-pitch. Center WL is selected to read. The grain boundary is generated randomly with limited grain size and angle. (b) Zoomed-in view figure describes the pitch and cell dimension.

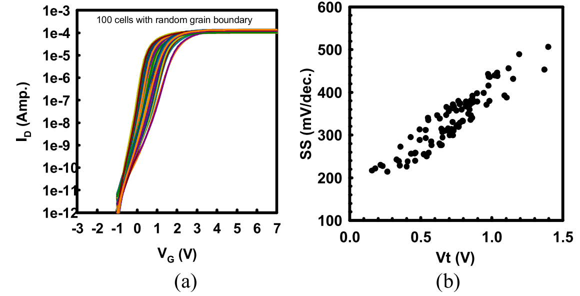


Fig. 2. (a) Collection of 100 simulated I_D–V_G curves using randomly generated grain boundary. Cell-to-cell variation in terms of Vt and SS is obvious. (b) Correlation plot between Vt and SS extracted from the IV curves in Fig. 2(a), which shows that devices with larger Vt have worse SS.

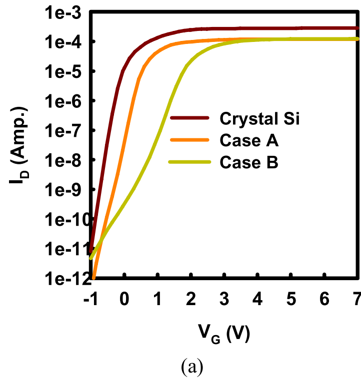
trap density [5]. In this paper, several crucial device parameters related to grain boundary traps are evaluated regarding the cell performance. To simply simulate architecture and improve simulation efficiency, a simple 2-D junction-free double gate (DG) NAND Flash architecture with n-type channel doping and a 38-nm half-pitch is simulated, as shown in Fig. 1(a) and (b) [13]. In this simulation, the channel doping is n-type at a concentration of 1×10^{17} cm^{-3} and the channel width is set as infinite. The crystal channel thickness (BL CD) is 30 nm. The simulated word-line (WL) number is 16 with one string selected line (SSL)/ground selected line (GSL). The critical WL width is 30 nm and the channel length of SSL/GSL is 0.25 μm. The ONO thickness is 5/7/7 nm with a 50-nm-thick p$^+$-poly-Si gate electrode. Regarding the junction profile, n$^+$ junctions are used outside the SSL/GSL whereas devices inside the NAND array are junction-free. To extract cell characteristics, the central WL is selected and read. When the transfer characteristics of the selected cell are read, 7 V is applied as the pass gate voltage and 3.3 V is set at the SSL/GSL. Drain voltage is 1 V. Vt is defined as the gate voltage when drain current = 100 nA and the subthreshold swing (SS) is extracted in the current range from 0.1 to 10 nA. The locations and shapes of grain boundaries are randomly generated using customized code provided by Synopsys [14].

To simplify the analysis of grain boundary effect further, two artificial limitations are imposed in this paper. One limitation is grain size and the other one is grain angle. The typical grain angle is limited to within ±45° and the typical grain size is 50 nm; this facilitated understanding the grain size effect. The grain boundary angle is defined as the angle between the direction parallel with the grain boundary and the direction perpendicular to the current flow. To generate a grain boundary, a fixed point is set at one side of the channel and a cut line is connected to this point across the channel to the other side. In addition, the angle of the generated grain boundary is smaller than the typical grain angle set artificially. Using these settings, multiple grain boundaries are randomly generated and grains grow. The grain angle is also randomly distributed. Regarding the grain boundary trap, the Gaussian distribution of acceptor and donor type traps are used at a trap density of 1×10^{13} cm^{-2}. In the mobility model, several mobility degradation models are considered. The first model is mobility degradation due to impurity scattering. The mobility dependence on the field perpendicular to the semiconductor-insulator interface is also considered. The effective field experienced by the carrier in its direction of motion is also applied. To evaluate the cell distribution, 100 samples are simulated under identical device conditions, using randomly distributed grain boundaries.

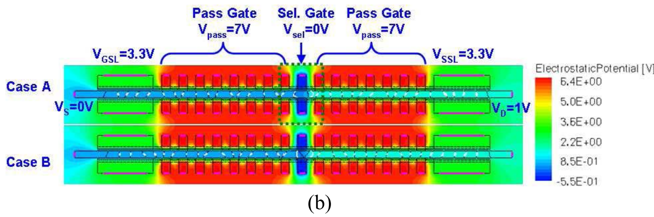
III. Simulation Result of Samples With Randomly Generated Grain Boundary Traps

A collection of 100 I_D–V_G curves is shown in Fig. 2(a). Since all the other geometric conditions are fixed, the variation in I–V curves has to be ascribed to the randomly distributed grain boundaries. In the subthreshold region, the curves merge together at a very low level (<1 fA). The merged point corresponds to the midgap voltage at which the interface traps become charge neutral and do not affect the subthreshold current. Fig. 2(b) shows the corresponding Vt versus SS correlation plot. The positive correlation between Vt and SS suggests that higher Vt and worse SS are both caused by the grain boundary effect. Another remarkable phenomenon is the occurrence of devices exhibiting the same Vt but distinct SS. This implies that various grain boundary conditions can yield the same Vt.

To elucidate this phenomenon further, two typical cases are chosen to evaluate the impact of random grain boundary effect. As shown in Fig. 3(a), the crystal Si curve is the simulated I–V curve lacking a grain boundary in the channel and Cases A and B are the cases of the sample with randomly generated grain boundary traps. In crystal Si, the default orientation is {1 0 0}. In Case A, there is no grain boundary under the selected gate but there is a grain boundary under the selected gate in Case B. Compared with the crystal Si sample, Cases A and B both exhibit degraded I–V curves due to the effect of traps presented at the grain boundary. Cases A and B are simulated based on identical geometric parameters, except for the grain boundary conditions; however, they exhibit distinct cell characteristics. Table I summarizes the cell characteristics extracted from these three samples.



(a)



(b)

Fig. 3. (a) Simulated I–V characteristics of a crystal Si sample (no grain boundary). Cases A and B are both of which have randomly generated grain boundary. (b) Simulated electrostatic potential distribution of Cases A and B in reading condition. Case B performs worse SS due to a grain boundary under the selected gate.

TABLE I

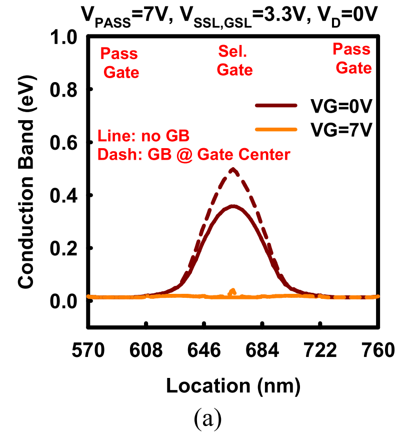
CELL CHARACTERISTICS ARE EXTRACTED FROM THESE THREE SAMPLES IN FIG. 3(a). COMPARED WITH THE FRESH SAMPLE, CASES A AND B SHOW WORSE VT, SS, GM, AND ON-STATE CURRENT

	Vt	SS	Gm	I_{on} (μA)	I_{off} (nA)
Crystal Si	-0.275	135	141	281	
Case A	0.267	214	63.7	120	58
Case B	1.397	506	46.6	124	<1

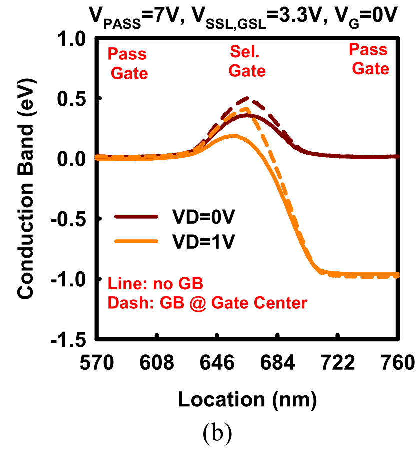
Fig. 3(b) shows the electrostatic potential distribution of Cases A and B under the reading condition. Under the reading condition in this paper, the central cell is selected to read and marked as Sel. gate, and all the other cells are applied by pass gate voltage and marked as pass gate. In a junction-Free NAND, a virtual junction is formed by the pass gate voltage applied. In Case A, grain boundary traps existed outside the selected device exhibits a parallel Vt shift with slightly SS degradation. However, the substantial cell degradation in Case B comes from grain boundary traps existed inside the channel of the selected Gate. They induce higher surface potential and a higher Vt measured. The degraded SS is also performed.

IV. GIGBL AND DIGBL SIMULATION

The impact of grain boundary traps on the subthreshold behavior can be clearly interpreted in Fig. 4, in which two simulated samples are compared. One sample has no grain boundary and the other sample has an artificial grain boundary in the channel under the center of the selected gate. Fig. 4(a) shows the conduction band at gate voltages of 0 and 7 V. Based on the simulated results, the grain boundary traps enlarge local conduction band under the selected gate. The raised conduction band can be reduced by increasing gate voltage. This phenomenon is known as GIGBL [15].



(a)



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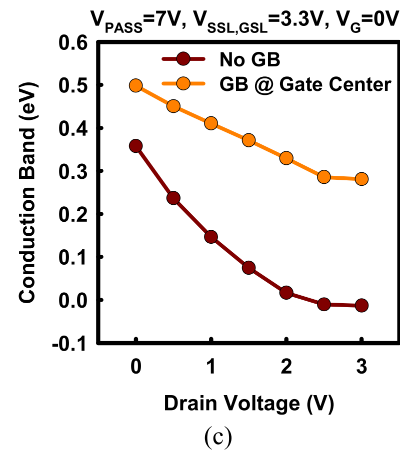

(c)

Fig. 4. (a) Simulated conduction band in the vicinity of the selected gate and its neighboring gates at $V_G = 0$ and 7 V. By applying various gate voltages with drain voltage kept at 0 V, the raised conduction band caused by the grain boundary traps is reduced with increasing gate voltage. (b) Comparison of channel conduction band for the sample with and without the grain boundary traps at VD = 0 V and VD = 1 V. (c) Extracted conduction value at the channel surface under the center of the selected gate.

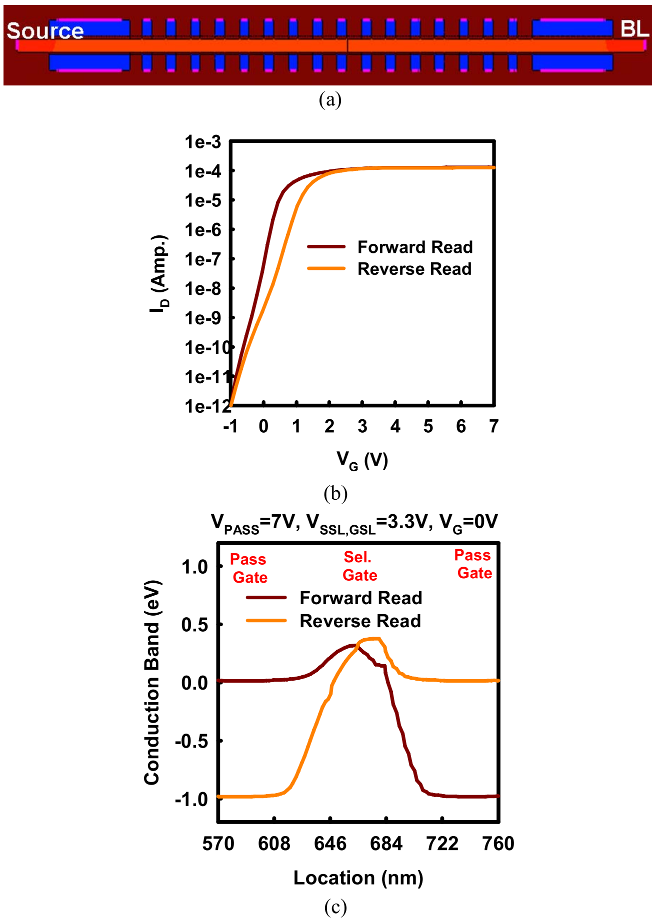

Fig. 5. (a) Simulated architecture with single grain boundary within the channel. The grain boundary is placed under the selected gate edge near the drain side. (b) Simulated IV curves as read from the forward and reverse read schemes. The read voltage is 1 V. (c) Extracted conduction band curvature at the channel surface under forward and reverse read.

The impact of drain voltage on the raised conduction band caused by the grain boundary traps is also explicit, as shown in Fig. 4(b). The already raised peak conduction band is further reduced by a higher drain voltage. Compared with the sample lacking a grain boundary, the peak conduction band value is suppressed by increasing drain voltage. This phenomenon is known as DIGBL [16]. Fig. 4(c) further describes the effect of drain voltage on the conduction band. The conduction band value is extracted at the channel surface under the center of the selected gate. A device containing grain boundary traps enlarges the conduction band and is suppressed by drain voltage. However, DIGBL cannot completely screen the impact of grain boundary traps and causes higher Vt than sample without GB.

V. Forward and Reverse Read

As shown in the previous section, the channel potential barrier is increased by the grain boundary traps. The raised potential barrier can be reduced by either applying a suitable gate or drain voltage, termed GIGBL and DIGBL, respectively. Based on these phenomena, a new method to examine the impact of grain boundary location and grain boundary traps is proposed. The simulation architecture is simplified,

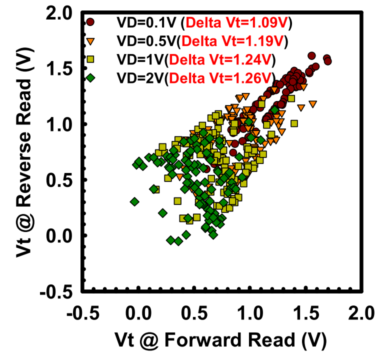

Fig. 6. Extracted Vt of the forward read and reverse read under BL voltage = 0.1, 0, 5, 1, 0, and 2.0 V. Delta Vt means maximum Vt variation between forward read and reverse read.

particularly under the grain boundary condition, as shown in Fig. 5(a). Only one grain boundary is placed in the channel under the selected gate edge near the drain side. The artificial grain boundary is perpendicular to the current flow direction, which eliminates the impact of the two side gates when the slope of the grain boundary is not perpendicular. The results of forward and reverse read at drain voltage = 1 V are shown in Fig. 5(b), which shows dissimilar transfer characteristics. Forward read refers to the scheme when BL is applied with a positive voltage and source is grounded. By contrast, reverse read refers to the scheme when a positive voltage is applied at source and BL is grounded. Fig. 5(c) shows the extracted conduction band profiles at the channel surface in forward read and reverse read. The applied gate voltage and drain voltage are 0 and 1 V, respectively. As shown in this figure, the potential at the grain boundary located near the drain side is higher for the forward than reverse read. Because the same device is simulated under the same grain boundary condition, the potential difference comes from the impact of voltage-dependent grain boundary traps and can be explained by the GIGBL and DIGBL effects. When the grain boundary is closer to the drain side, the DIGBL effect is stronger in the forward read scheme than in the reverse read. Thus, in forward read, the corresponding channel potential barrier at the grain boundary is reduced to a greater extent and the resultant Vt is also lower. By the same token, the Vt in reverse read is lower when grain boundary is located near the source side.

To elucidate this phenomenon, various BL voltages are applied, as shown in Fig. 6. At each BL voltage, 100 samples with randomly generated grain boundary structures are simulated. The typical grain size and grain angle are 50 nm and 45°, respectively. The central WL is selected to read while all the other WLs' are applied with pass gate voltage equal to 7 V. The read voltage is applied at either drain- or source-side. To describe the impact of grain boundary, the Vt difference (delta Vt) between forward read and reverse read are calculated. When the BL voltage is low (0.1 V), the DIGBL effect is not significant and the Vt's from the forward and reverse read are similar. With higher BL voltage, the enhanced DIGBL effect magnifies the difference between the forward and reverse read.

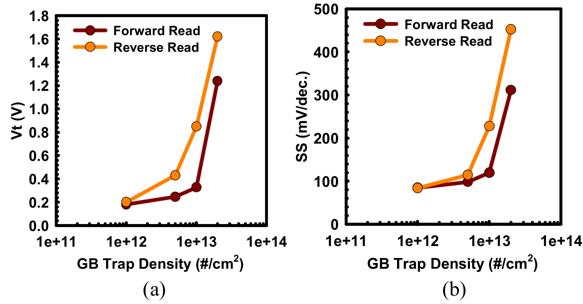

Fig. 7. (a) Extracted Vt of forward read and reverse read under various GB trap density. The GB location is set at the selected gate edge near drain side. (b) Extracted SS under various GB trap density. With increasing GB traps, SS becomes worse.

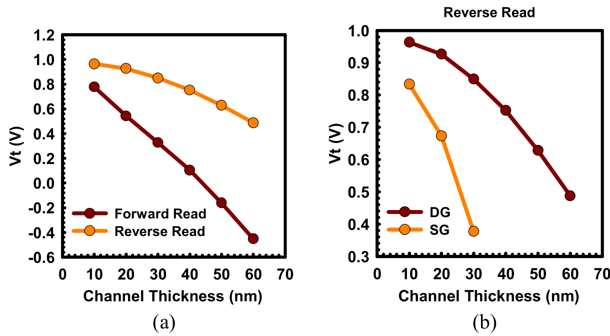

Fig. 8. (a) Extracted Vt of forward read and reverse read under various channel thickness. The GB location is set at the selected gate edge near drain side. (b) Comparison of DG and SG under various channel thickness in the reverse read testing.

The implication of grain boundary traps can be examined from another perspective, as shown in Fig. 7. The location of the grain boundary is still at the selected gate edge near the drain side but with various grain boundary trap densities. When the density of the grain boundary trap is low, the raised local surface potential barrier is low and the Vt difference between forward read and reverse read is small. When the density of grain boundary traps becomes higher, the induced local surface potential barrier is raised. Therefore, the corresponding DIGBL effect is more obvious and the asymmetrical cell Vt in the forward and reverse read starts to manifest itself.

Fig. 8(a) and (b) shows the impacts of channel thickness, which is equivalent to BL width, on the cell behavior of the TFT device. Since an n-type doping channel is used in this simulation study, the thinner channel has a better gate control capability and the Vt difference between the forward and reverse read is reduced, as shown in Fig. 8(a). On the other hand, the thicker channel has weak gate control ability and causes lower Vt and worse SS. Another observation is the Vt roll-off trend. With increasing channel thickness, Vt in the forward read is degraded much more significantly than in reverse read. This can be explained by considering the DIGBL effect. When the channel thickness is thinner, the gate control ability is enhanced and the impact of DIGBL is suppressed. With the thicker channel, the weak gate control ability accentuates the DIGBL effect and Vt in forward read is degraded much more significantly than in reverse read.

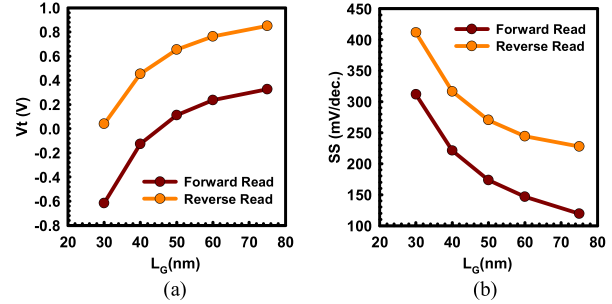

Fig. 9. Extracted (a) Vt and (b) SS of forward read and reverse read as a function of channel length. The GB location is set at the selected gate edge near drain side. Both Vt and SS roll-off show similar behavior regardless of the read scheme.

This effect is further evidenced by the comparison between DG and single gate (SG) architecture, as shown in Fig. 8(b).

Fig. 9(a) and (b) shows Vt and SS, respectively, as a function of channel length. In this simulation study, the channel length is set as equal to the half-pitch. Based on the simulation result, pitch scaling exhibits similar Vt and SS roll-off trend regardless of the read scheme, translating to similar DIGBL and GIGBL effect with respect to pitch scaling. In a previous work on junction-free device with the impact of pass gate voltage, the pass gate voltage does not only turn on its own channel but the adjacent virtual junction nearby gate is also formed [2]. However, with the pitch scaling, not only the pass gate voltage facilitates inverting the virtual junction, but also the fringing field from the pass gate voltage penetrates into the channel of the adjacent cell and causes lower Vt. This phenomenon becomes more severe at shorter channel length.

VI. Conclusion

In a 3-D NAND Flash architecture, polysilicon material facilitates the process integration by providing a simple but flexible process integration. However, polysilicon material with the random distributed grain boundary and its traps affect the device characteristic, causing a wider distribution when such material is used as a conductive channel. The trap and de-trap through grain boundary traps disturb the device characteristic. The wider distribution from the random telegraph noise or cell operation needs the advanced skills to tighten distribution. Regarding the cycling endurance and temperature sensitivities, both are key topics to evaluate. In this paper, the impact of randomly distributed grain boundary is studied comprehensively. Randomly generated grain boundary and its associated traps induce local surface potential barrier and degrade cell characteristics. DIGBL and GIGBL effects are two phenomena that serve as the underlying mechanisms of these impacts. The asymmetrical behavior of forward and reverse read may be used to pinpoint the GB location. With the aid of TCAD simulation, crucial device parameters, such as channel thickness, cell geometric architecture, and grain boundary traps are studied in depth. When pitch is scaled, thinner channel provides better gate control ability and is beneficial for cell performance. As for the cell geometric architecture, DG device, such as used in VG 3-D NAND,

shows better device performance than the SG counterpart. Grain boundary trap is closely related to fabrication process and has strong influence on cell distribution. These insights help to predict the development of 3-D NAND Flash memory.

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Yi-Hsuan Hsiao (S'10) received the B.S and M.S degrees in electrical engineering from the National Chiao- Tung University, Hsinchu, Taiwan, in 2002 and 2004, respectively, where he is currently pursuing the Ph.D. degree.

He joined Emerging Central Laboratory, Macronix International Company, Ltd., Hsinchu, in 2005. His current research interests includes developing the novel 3-D NAND Flash technology.

Hang-Ting Lue (M'05) received the B.S. and M.S. degrees in physics from National Tsing Hua University, Hsinchu, Taiwan, in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering from National Chiao Tung University, Hsinchu, in 2002.

He joined the Emerging Central Laboratory, Macronix International Company, Ltd., Hsinchu, in 2003, where he is currently the Project Leader of 3-D NAND Flash Product Development.

Wei-Chen Chen received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 2011.

He is currently with Macronix International Company, Ltd., Hsinchu, as a Principal Engineer, involved in research and development of 3-D NAND Flash memory technology.

Kuo-Pin Chang received the Ph.D. degree from the Institute of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan, in 2004.

He is currently with Macronix International Company, Ltd., Hsinchu, as a Principal Engineer, involved in research and development of 3-D NAND Flash memory technology.

Yen-Hao Shih (M'03) has been involved in nonvolatile memory technology development since joining Macronix International Company, Ltd., Hsinchu, China.

Dr. Shih was a member of the IEDM CRY subcommittee and the IRPS Memory committee. He has served as an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES since 2010.

Bing-Yue Tsui (S'87–M'93–SM'01) received the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1992.

He is currently a Professor with the Department of Electronics Engineering, National Chiao Tung University.

Kuang-Yeu Hsieh was born in Taiwan in 1958. He received the B.S., M.S., and Ph.D. degrees from National Tsing Hua University, Hsinchu, Taiwan, National Sun Yat-sen University, Kaohsiung, Taiwan, and North Carolina State University, Raleigh, NC, USA, in 1980, 1985, and 1989, respectively.

His current research interests include thin-film growth, solid-state physics, IC fabrication, new device structure, and material for the next generation nonvolatile memory.

Chih-Yuan Lu (M'78–SM'84–F'95) received the Ph.D. degree from Columbia University, New York, NY, USA.

Previously, he was with AT&T Bell Labs, Murray Hill, NJ, USA. He is the Chairman of Ardentec Corporation, Hsinchu, China, and serves as the President of Macronix International Company, Ltd., Hsinchu.

Dr. Lu is an American Physical Society Fellow.