Temperature-Dependent Instability of Bias Stress in InGaZnO Thin-Film Transistors

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***Abstract*— The instability of the gate bias and drain bias stresses is observed at high temperature in amorphous InGaZnO thin-film transistors (a-IGZO TFTs). The transfer characteristics of a-IGZO TFTs at different temperatures are also investigated in this paper. The transfer curve exhibits an apparent subthreshold current stretchout phenomenon at high temperature. The stretchout phenomenon becomes more serious with the increase of the temperature. In addition, thermally induced holes are accumulated by the negative gate voltage and get trapped in the gate dielectric or at the dielectric/channel interface at high temperature. The negative threshold voltage shifts with stress time and this is because the trapped holes induce more electrons. For drain bias stress at high temperature, the transfer curve exhibits an apparent shift during drain bias stress at high temperature compared with the same at room temperature. At high temperature, thermally induced holes are trapped in the gate insulator, especially near the drain region. Capacitance-voltage measurements have been used to prove the nonuniform hole-trapping phenomenon. Furthermore, the simulation of the capacitance-voltage and current-voltage curves also have been applied to confirm the hole-trapping distribution. The obtained results clarify that the instability is caused by nonuniform hole-trapping phenomenon.**

***Index Terms*— Bias stress, indium gallium zinc oxide (IGZO), technology computer-aided design (TCAD), temperature, thin-film transistors (TFTs).**

I. Introduction

RECENTLY, portable electronic products have combined display [1], [2], memory [3]–[7], and logic devices. Amorphous oxide thin-film transistors (TFTs), such as indium-gallium-zinc oxide (IGZO) TFTs have attracted considerable attention for their use in active matrix displays due to their high mobility ($\sim$10 cm^2/V-sec) [8], large ON/OFF current ratio ($>10^8$) [9], fairly good uniformity, and good transparency. Furthermore, the low process temperature and low cost are desirable for large flat panel display applications [10], [11]. In particular, a-IGZO TFT has been recognized as a potential device for switching/driving TFTs in active matrix organic light-emitting diode displays (AMOLED), which require TFTs with high current drivability to achieve uniform brightness. The stability of TFT under long-term current operation is critical in the case of current-driven AMOLED displays because it influences pixel signal level/emission intensity [12]–[14]. For the a-IGZO TFTs to act as the display's backplane electronics, reliability and stability are very important. In previous studies, only the instability caused by gas ambient [15]–[19] and light issue [20], [21] have been proposed as critical issues in the application of display industry. However, TFT in active matrix display is usually influenced by heat from the light source and operated conditions [22], [23]. It should be carefully investigated, because in a real operating situation the effect of temperature influences the TFT under applied bias. Moreover, the reliability issue for a-IGZO TFT operated on turn-OFF state ($V_G = 0$ V and $V_D > 0$ V) stress at high temperature has not yet been studied. In this paper, we investigate gate bias and drain bias stresses at the different temperatures and explain the stress effect with assistance of band diagrams. In addition, we discuss the abnormal subthreshold leakage current with temperature dependence of the a-IGZO TFT. Finally, the capacitance-voltage measurement and technology computer-aided design (TCAD) simulation system are used to confirm the proposed mechanism.

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II. Experimental Setup

Bottom gate coplanar a-IGZO TFTs were produced on a glass substrate in this paper. Plasma-enhanced chemical vapor deposition (PECVD)-derived SiO_x (300 nm) film as the gate insulator was grown at 370 °C over the patterned Ti/Al/Ti trilayer gate electrodes. The Ti/Al/Ti source/drain electrodes were formed by sputtering and then patterned into the dimensions of channel width (W) from 5 to 30 μm and channel length (L) of 10 μm. A 30-nm-thick a-IGZO film was deposited by dc magnetron sputtering system at room temperature using a target of In:Ga:Zn = 1:1:1 in atomic ratio. The plasma discharge power was 300 W under the pressure of 5 mTorr ambiance of O_2/Ar gas mixture at the ratio of 6.7%.

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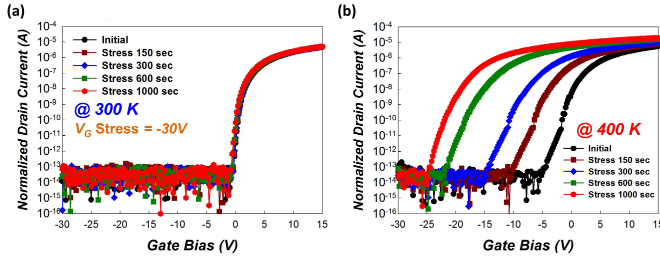

Fig. 1. I_D–V_G curves of a-IGZO TFTs under negative gate bias ($V_G = -30$ V) at (a) 300 K and (b) 400 K.

After defining the active region, the devices were capped with a 200 nm SiO_x layer by PECVD at 170 °C and sequentially annealed in oven at 330 °C for 2 h. The electrical properties of the a-IGZO TFTs were analyzed using Agilent B1500A Semiconductor Device Analyzer in a dark environment. The threshold voltage (V_T) is defined as the gate voltage when the normalized drain current ($NI_D = I_D \times L/W$) reaches 10^{-10} A.

III. Results and Discussion

Fig. 1(a) and (b) shows the transfer characteristics of as-fabricated a-IGZO TFTs in the experiment of negative bias temperature instability (NBTI) stress with $Vg = -30$ V at 300 and 400 K, respectively. The stress time is from 150 to 1000 s. At 300 K, the transfer curves hardly shift under negative gate bias stress, which is consistent with previous reports [24]–[26]. The invariability of curves can be explained by the lack of holes in channel. There are no holes that could be attracted into gate insulator by the negative gate bias. On the other hand, when the temperature is increased to 400 K with -30 V stress, the V_T under stress time of 1000 s shifts significantly to the negative direction by 20.21 V compared with the V_T at the initial state, that is, stress time is 0 s. At high temperature with negative gate bias stress, the thermal induced holes from defect states are accumulated by the negative gate voltage and trapped in the gate dielectric or at the dielectric/channel interface. The trapped holes induce more electrons to shift the curves negatively with stress time.

In general, a-IGZO-TFTs have no holes in channel [24], [25]. However, after negative gate bias stress at 400 K, the transfer curves clearly shift to left direction. Moreover, the transfer curves stretch out and abnormal subthreshold leakage current is significant before negative bias stress at 400 K as shown in Fig. 1(b) with black line. Next, we discuss the unique behavior of the subthreshold leakage current for a-IGZO TFTs at high temperature. Fig. 2 shows the transfer characteristics of a-IGZO TFTs at the different temperatures between 300 and 450 K. As seen in this figure, the I–V curves shift to the negative direction and drain current (I_D) raises with increasing temperature. It is well known for oxide semiconductors that the free electrons in the materials are mainly due to the detrapping from sub-bandgap trap states and the generation of oxygen vacancies [27], [28]. Thermally excited electrons are detrapped from relatively shallow sub-bandgap trap states. In addition, more oxygen vacancies are induced by thermal excitation, therefore, more free electrons

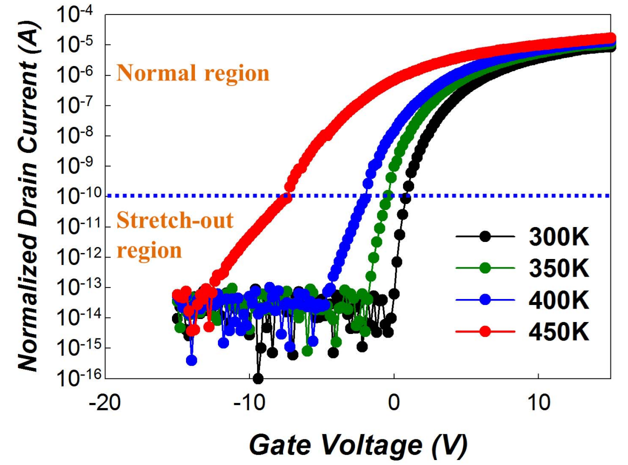

Fig. 2. I_D–V_G curves of a-IGZO TFTs at the different temperatures between 300 and 450 K.

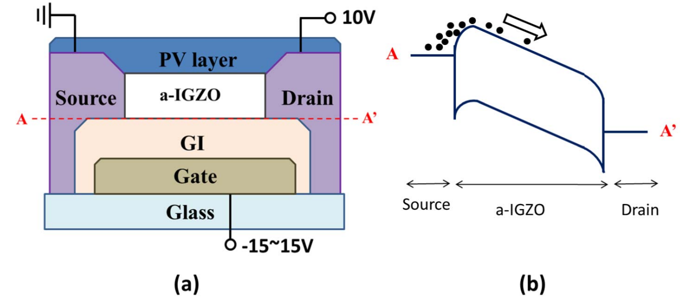

Fig. 3. (a) Schematic of the device structure with basic device operation. (b) Energy band diagram at 300 K.

are generated. The lower V_T observed at the higher temperature can be because of these free electrons from the sub-bandgap trap states and generated along with the oxygen vacancies [29], [30]. Furthermore, the significant abnormal subthreshold leakage current that is observed at 400 K and this stretchout phenomenon becomes more serious with increasing the temperature. However, this temperature effect is reversible in that the transfer characteristics at 300 K can be restored after the high-temperature measurements.

While the IGZO TFT is turned on at 300 K, a positive bias was applied to the gate and drain was given a constant positive bias as shown in Fig. 3(a). Electrons could overcome the barrier between source and channel and move to drain through channel as shown in Fig. 3(b). Unlike those at 300 K, the transfer characteristics at 400 K can be separated into stretchout and normal regions by V_T as can be seen from Fig. 2. The mechanisms for these two distinctive regions are proposed in Fig. 4(a) and (b). As shown in Fig. 4(a), when the gate voltage is below V_T, the trap-induced thermal-generation holes moves to the source side owing to the transverse electric field, the holes accumulate at the source region that leads to the source side barrier lowering. The lowering enhances electrons injection from the source and causes an apparent subthreshold leakage current. When V_G is larger than V_T, the transfer characteristics are dominated by the barrier between

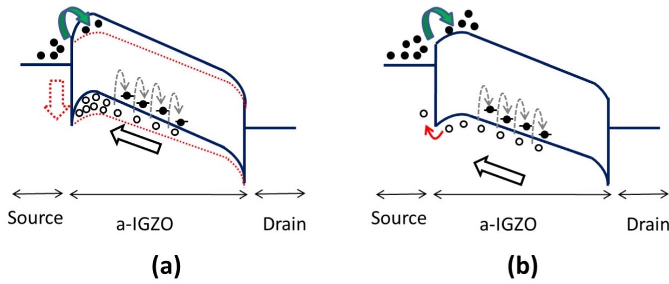

Fig. 4. Energy band diagram of proposed mechanisms for these two distinctive regions (a) gate voltage is below V_T and (b) gate voltage is above V_T at 400 K.

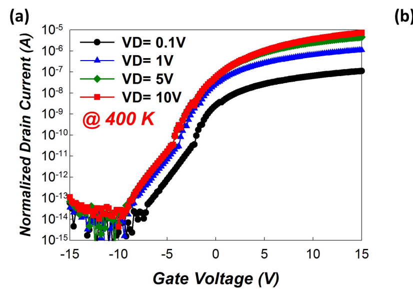

Fig. 5. (a) Normalized current–voltage characteristics at the different drain voltages. (b) Energy band diagram with the different drain voltages.

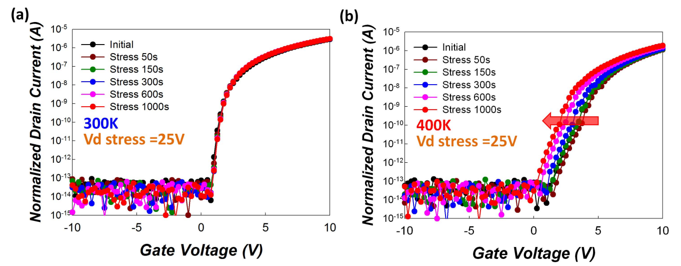

Fig. 6. Characteristics of transfer curves I_D–V_G before and after drain bias stress at (a) 300 K and (b) 400 K.

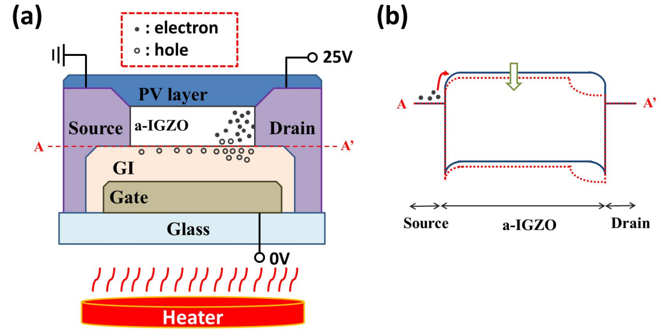

Fig. 7. (a) Schematic diagram of hole-trapping mechanism under after bias stress. (b) Energy band diagram from A to A′.

the a-IGZO and source. The holes accumulation on the source-side would flow to the source when the a-IGZO TFTs turned on. The barrier height becomes much lower with the increase of the gate voltage; therefore, the holes cannot accumulate at source-side, as shown in Fig. 4(b).

The status of hole accumulation is further examined by measuring the normalized current–voltage (V_G–I_D) characteristics at the different drain voltages, as shown in Fig. 5(a). At 400 K, the subthreshold leakage current increases significantly with the drain bias increase. Furthermore, the stretchout voltage is more negative when the drain bias becomes larger and the subthreshold leakage current saturates when the drain voltage (V_D) above 5 V. It is implied that the thermal-induced holes could drift to the source barrier owing to the transverse electrical field by the drain bias. The holes accumulate at the source region which leads to the source side barrier lowering. The lower source side barrier enhances electrons injection from the source and causes an apparent subthreshold leakage current. When the drain bias increase, the large transverse electrical field results in the more holes drift to the source region, as shown as Fig. 5(b). This phenomenon makes the source barrier lowering become more serious. Thus, the subthreshold leakage current raises with the drain bias increase. On the other hand, when the drain bias is larger than 5 V, the source barrier lowering saturates since all the thermal excited holes drift to the source region. Therefore, the stretchout phenomenon saturates when the drain bias is above 5 V.

In addition to NBTI, the reliability issue for a-IGZO TFT operated in the turn-OFF state ($V_G = 0$ V and $V_D > 0$ V) at high temperature was investigated. Fig. 6(a) shows the transfer curves of I_D–V_G for a-IGZO TFT before and after drain bias stress at 300 K with a bias stress condition of $V_D = 25$ V and $V_{G,S} = 0$ V for 50–1000 s. The electrical curves almost exhibit no shift under positive drain bias stress. By contrast with drain stress at 300 K, Fig. 6(b) shows the electrical curves for a-IGZO TFT before and after drain bias stress at 400 K operated under the similar stress condition. At 400 K, the transfer curves stretch out in the subthreshold region. The stretchout phenomenon is caused by the same reason as discussed in Fig. 2. After stress at 400 K, the V_T shifts significantly to the negative Vg direction by 1.68 V. The subthreshold swing (SS) before drain stress and after 1000 s drain stress is 347 and 376 mV/dec, respectively. The subthreshold swing fractional change (ΔSS) value is 29 mV/dec which is defined by $\Delta \mathrm{SS}\ (\mathrm{mV/dec}) = \mathrm{SS}^a - \mathrm{SS}^b$, where SS^a refer to after stress and SS^b refer to before stress, respectively. The negative Vg shift with slight degradation of SS indicates that the state creation is negligible. It is suggested that electrons are attracted to the drain electrode owing to the positive drain bias, as shown in Fig. 7(a). The thermal-induced holes are repelled simultaneously to the gate dielectric layer by positive drain voltage and trapped in the gate dielectric or dielectric/channel interface. Fig. 7(b) shows the corresponding band diagram from A to A′ in Fig. 7(a). The trapped holes in the gate dielectric lead to channel barrier lowering. The channel barrier lowering enhances electrons injection from source to channel which makes it easier to turn on TFT. Furthermore, the barrier lowering near drain side is more serious than that of the source side because of the larger electrical field of the former. However, the V_T is decided on the highest barrier side. Therefore, the V_T is determined by the source side barrier. In addition, the invariability of V_T at 300 K

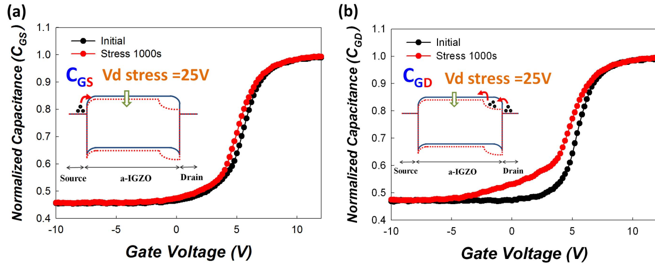

Fig. 8. (a) $C_{GS} - V_G$ and (b) $C_{GD} - V_G$ transfer characteristics of a-IGZO TFT before and after drain bias stress.

can be explained by the lack of holes in channel. Therefore, the instability of drain bias stress is more pronouonced at the high temperature.

To further clarify the instability effect, the capacitance-voltage (C–V) measurement of a-IGZO TFT was used to prove the proposed mechanism. Fig. 8(a) shows the C_{GS}–V_G curves before and after drain bias stress ($V_D = 25$ V) at 400 K. In the C_{GS}–V_G measurement, capacitance measurement high (CMH) is applied to the gate electrode and the source electrode is connected to capacitance measurement low (CML). After 1000 s drain stress, V_T variation with no degradation of SS is observed, which is similar to the I_D–V_G transfer curves as shown in Fig. 6(b). In C_{GS-VG} measurement, the amount of carrier is measured from source region to channel as shown the inset of Fig. 8(a). The barrier lowering induced easier carrier injection to the channel that results in a smaller V_T. Therefore, the $C_{GS-}V_G$ curve after drain bias stress shifts in parallel with original curve to the negative direction. However, the $C_{GD-}V_G$ curves, that is, CMH is applied to the gate electrode while the CML is connected to the drain electrode, exhibit an obvious degradation by hump effect and negative V_T shift after the drain bias stress, as shown in Fig. 8(b). The result indicates this only occurs in the channel near the drain region. As larger bias is applied at the drain electrode, a stronger vertical electric field exists in the channel near this area. This result shows the severe hole-trapping phenomenon near the drain region which induces serious barrier-lowering in the channel near drain region as shown in Fig. 7(b). The serious barrier-lowering induces hump effect of $C_{GD-}V_G$ curve. Therefore, the two-stage degradation in C_{GD}–V_G curve which includes hump effect and negative V_T shift occurs after drain bias stress at the high temperature.

According to the above discussion, the hump effect of $C_{GD-}V_G$ curve is correlated to the gate-drain vertical electrical field. To further examine the proposed mechanism, TCAD simulation system was employed. Fig. 9(b) shows the simulation results of $C_{GD-}V_G$ curves for the nonuniform hole-trapping model after drain bias stress. Fig. 9(a) shows the simulation device structure. In this simulation, hole trapping in the dielectric is 1×10^{15}/cm^3 and the concentration of hole injection near the drain is adjusted to 1.2×10^{16}/cm^3. Combined with the experimental data, we can find that the simulation of hump behavior matches with the experimental results after drain bias stress. In addition to $C_{GD-}V_G$ curves, the transfer curve of I_D–V_G is simulated as shown in Fig. 9(b). The V_T after stress shifts to the negative direction by 1.79 V compared with the

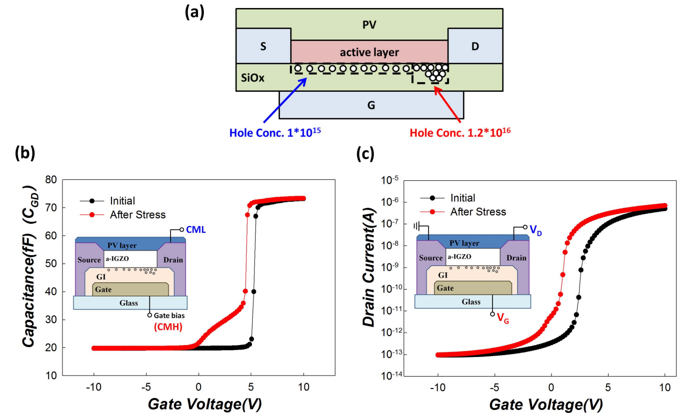

Fig. 9. (a) Schematic of simulation device structure and the simulation results of electrical properties of (a) $C_{GD} - V_G$ and (b) $I_D - V_G$ curves.

V_T at the initial state and ΔSS value is 35 mV/dec. The curve shifts to left with slight SS degradation is consistent with the experimental results shown in Fig. 6(b). These simulation results further verify the characteristic degradation after drain bias stress, which is also proved by our nonuniform hole-trapping model.

IV. Conclusion

The transfer characteristics of a-IGZO TFTs at the different temperatures and the instability of bias stress at high temperature have been investigated. The transfer curve exhibits an apparent subthreshold current stretchout phenomenon at high temperature and this phenomenon becomes more serious with the increase of the temperature. The negative gate bias temperature instability experiment has been used to prove the thermally induced holes generation. In addition, the transfer characteristics with different drain voltages have been used to confirm the status of holes accumulation. Moreover, the temperature instability of the drain bias can be observed at high temperature. During drain bias stress at high temperature, thermally induced holes are trapped in gate insulator, especially near the drain region. The C–V measurement and the simulation results are applied to prove the nonuniform hole-trapping phenomenon. These results clarify the temperature is a critical parameter on the operation of a-IGZO TFT device.

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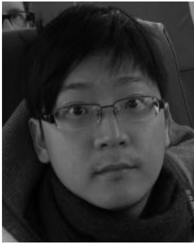

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