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Planar junctionless poly-Si thin-film transistors with single gate and double gate

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In this letter, single- and double-gate (SG and DG) planar junctionless (JL) thin-film transistors fabricated via a simple process with an in situ-doped active layer is discussed. The DG structure demonstrated a superior subthreshold swing of 160 mV/dec and a lower off-current of 1.3×10^{-13} A than those of 329 mV/dec and 2.1×10^{-12} A for the SG structure, respectively. It contributes to the enhancement of the gate controllability and ultrathin channel. Consequently, the simple fabrication process of the DG JL device is suitable for future application on system-on-panel and three-dimensional integrated circuits. © 2014 The Japan Society of Applied Physics

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been successfully used in active-matrix organic light-emitting displays (AMOLEDs) and attract considerable interest for system-on-panel (SOP) and three-dimensional integrated circuit (3D IC) applications owing to their prominent mobility performance.[1–8)]

However, scaling down the conventional planar transistors to realize the high-speed operation is excessively challenging as the dimensions of devices are shrunk toward the nanometer region. The electric field lines from source and drain would significantly encroach the channel region with the reduction in gate length, giving rise to a remarkable increase in short-channel effects.[9,10)] Moreover, the thermal budget of dopant activation is a big challenge in fabricating nanoscale devices.[11,12)]

Recently, a nanowire transistor without junctions, called the junctionless (JL) transistor, has been demonstrated on the silicon-on-insulator wafer.[13–25)] The device structure of the JL transistor is directly descended from the conventional FinFET by homogeneous doping of silicon nanowire. The tremendous advantages of JL devices include good control of short-channel effect, immunity from the ultrashallow junction formation and therefore elimination of highly expensive annealing equipment, suppression of the mobility degradation from surface roughness scattering, and repression of the intrinsic delay time by increasing the doping concentration. These excellent features would permit a much greater scaling down of the MOSFET. However, the JL devices are very sensitive to the channel size, the channel size of JL devices has to be very small and show good uniformity.[25–27)] Therefore, the channels of planar JL devices should be ultrathin.

However, achieving high performance by scaling down the channel size has many process challenges, such as precise control of etching back, ability of deposition of ultrathin film, or deposition uniformity. In this work, we propose a double-gate structure via in situ phosphorous-doped poly-Si deposition processes by low-pressure chemical vapor deposition (LPCVD) to enhance the feasibility of JL TFTs.[28–30)] Following the transfer characteristics and simulation results, single- and double-gate (SG and DG) JL TFT devices are discussed and proposed.

Figures 1(a)–1(f) show the process flow schematic of the DG JL TFTs. Initially, an in situ phosphorous-doped polycrystalline silicon of 200 nm thickness was deposited using an LPCVD system on the oxided silicon wafer. Then, the patterned bottom gate was transferred using the RIE system [Fig. 1(a)]. Next, a tetraethylorthosilicate (TEOS) bottom-gate oxide of 10 nm thickness, in situ phosphorous-doped poly-Si n-type channel of 10 nm thickness, and TEOS top-gate oxide of 10 nm thickness were sequentially deposited by LPCVD, and then the active region was patterned [Fig. 1(b)]. Subsequently, to form a top-gate electrode, an in situ phosphorous-doped poly-Si of 200 nm thickness was deposited and then patterned, as shown in Fig. 1(c). Before finishing the JL devices, the source and drain regions have to have larger thickness to reduce the series resistance. However, the source/drain (S/D) region should avoid contact with the top-gate electrode; hence, the S/D and top-gate regions should be separated. Silicon nitride (Si_3N_4) of 300 nm thickness was deposited and etched by RIE, and the sidewall spacer of Si_3N_4 was used to separate the top gate and S/D regions [Fig. 1(d)]. Then, we increased the thickness of the S/D region to reduce the series resistance; hence, an in situ phosphorous-doped poly-Si of 200 nm thickness was deposited [Fig. 1(e)]. After a passivation oxide layer was deposited, the contact hole opening and metallization were completed to fabricate the proposed DG JL TFTs. We also fabricated SG JL TFTs without a bottom gate process, as shown in Fig. 1(f).

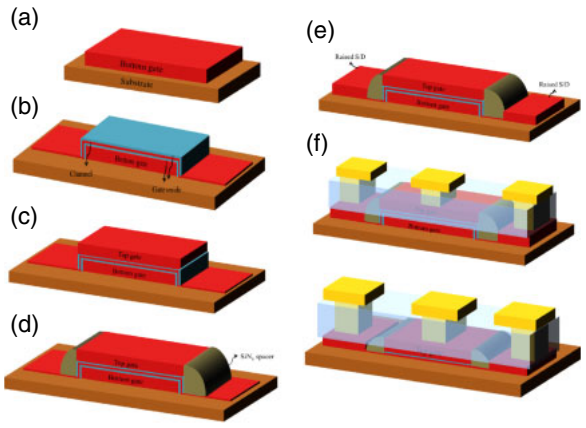

Fig. 1. (Color online) (a)–(e) Schematic diagram of process flow for DG junctionless device. (f) Final DG and SG junctionless device structures.

After SG and DG device formation, a semiconductor parameter analyzer (Agilent 4156C Technologies) and a probe station were used to measure the current–voltage (I–V) characteristics. Analytical field-emission transmission electron microscopy (TEM; JEM-2100F) was employed to analyze the device structure and identify the channel thickness of fabricated devices. The samples for cross-

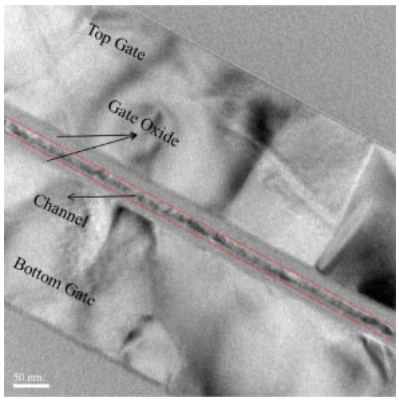

Fig. 2. (Color online) Cross-sectional transmission electron microscopy image of DG structure with top TEOS gate dielectric/in situ-doped poly-Si channel/bottom TEOS gate oxide.

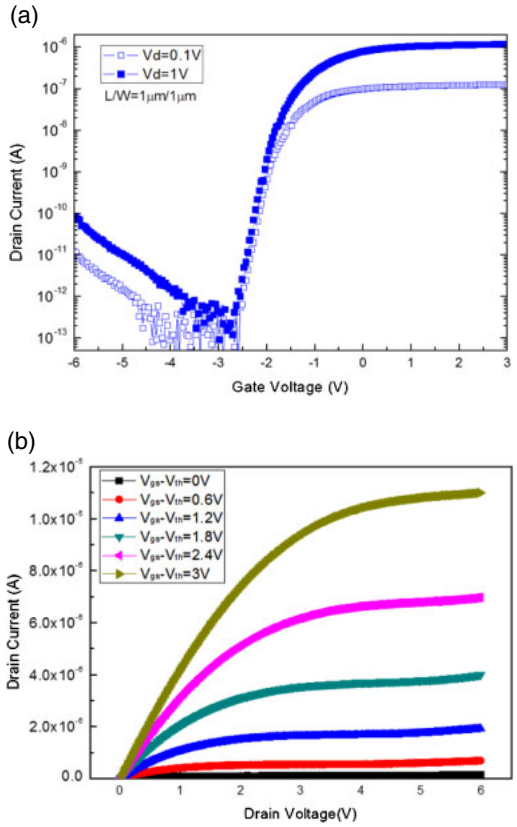

Fig. 3. (Color online) Typical transfer and output characteristic of DG JL device for $W = L = 1\,\mu\text{m}$.

sectional TEM were prepared by the focused-ion-beam (FIB) technique (FEI Nova 200).

Figure 2 shows the cross-sectional TEM image of the DG JL TFT. It can be seen that the thickness of the top-gate oxide, bottom-gate oxide, and device channel is about 10 nm and very uniform.

Typical transfer and output characteristics of the DG JL device for $W = L = 1\,\mu\text{m}$ are shown in Figs. 3(a) and 3(b), respectively. For comparison, Fig. 4 shows the transfer characteristics of the SG and DG JL TFTs. Obviously, the DG JL TFT has better electrical transfer characteristics than the SG JL one. Table I shows a summary of the several important parameters of the device characteristics of SG

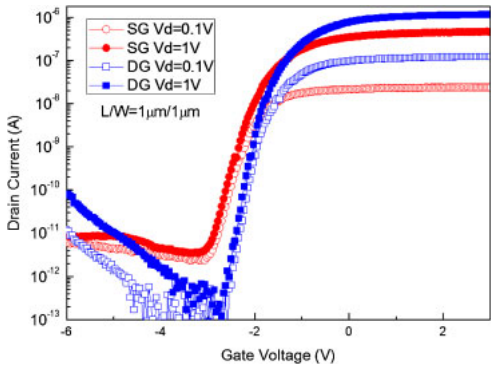

Fig. 4. (Color online) Comparisons of transfer characteristics of SG and DG JL TFTs.

Table I. Comparisons of electrical characteristic of SG and DG junctionless TFTs for $W = L = 1\,\mu\text{m}$.

	DG	SG
Threshold voltage (V)	−1.56	−2.14
Subthreshold Swing (mV/dec)	160	329
Off-current (A)	$\sim 1.3 \times 10^{-13}$	$\sim 2.1 \times 10^{-12}$
On/off current ratio	1.1×10^{7}	1.4×10^{5}

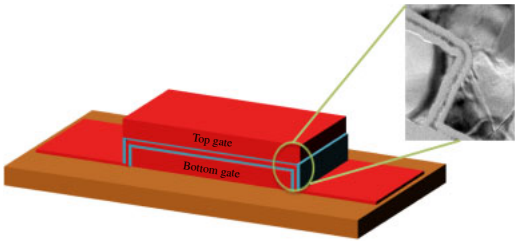

Fig. 5. (Color online) Cross-sectional diagram and TEM image of bottom-gate corner structure.

and DG JL TFTs. The subthreshold swing is extracted from the linear region at $V_{ds} = 0.1\,\text{V}$, and the on/off current ratio is defined at $V_{ds} = 1\,\text{V}$. The threshold voltage is defined according to the normalized drain current of $I_{ds} = (L/W) \times 10^{-8}$ at $V_{ds} = 0.1\,\text{V}$. The DG JL device achieved a better threshold voltage of $-1.56\,\text{V}$, a lower subthreshold swing of 160 mV/dec, and a higher on/off current ratio of 1.1×10^{7}, whereas the SG one showed a poorer threshold voltage of $-2.14\,\text{V}$, a larger subthreshold swing of 329 mV/dec, and a smaller on/off ratio of 1.4×10^{5}. The DG structure demonstrated the enhanced gate controllability at the same channel thickness with the SG one. Therefore, the DG device could completely deplete the carriers at the depletion region without a thinner channel, similarly to the SG device. Consequently, the DG device displayed a lower off-current than the SG one.

However, the off-current leakage of the DG JL TFT increased with increasing negative gate bias, which contributes to the corner effect of the bottom-gate structure. Figure 5 shows the cross-sectional diagram of the DG device and the TEM image of the material sample without patterning the top gate. It can be seen that a corner exists in the structure caused by the bottom gate. The corner structure enhanced the electrical field, and hence, the carriers were easy to pass

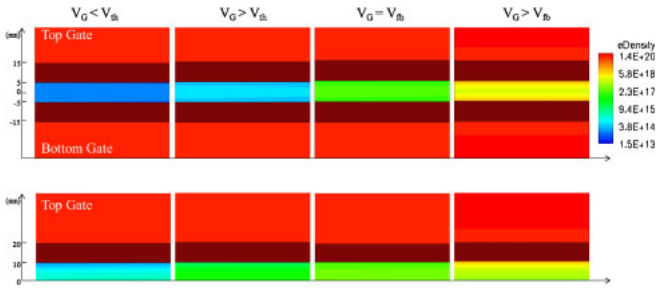

Fig. 6. (Color online) Simulation of electron density with SG and DG JL devices at different gate voltages.

through the 10-nm-thick bottom TEOS gate oxide when the negative gate voltage was increased. Consequently, the leakage of the DG structure was increased with increasing negative gate voltage.

Figure 6 shows the simulation of electron densities with SG and DG structures at different gate voltages. Since the JL devices generally have a highly doped channel, the JL devices operate as a depletion-mode device. First, in the depletion region ($V_g < V_{th}$), the carriers were depleted by the electrical field from negative gate bias. The channel electron density of the DG structure was lower than that of SG ones; the experiment results also show that the off-current of the DG structure is one order lower than that of the SG structure. Although the sidewall channels did not cover the top gate, the DG devices also showed better electrical characteristics than the SG ones, such as a steeper subthreshold swing and a lower off-current. It contributes to the better gate controllability and higher conduction current. In the case of the SG structure, fewer carriers formed near the top-gate channel but more carriers formed away from the top-gate channel in the subthreshold region ($V_g > V_{th}$). While the opposite spatial carrier distribution was formed in the DG structure, more carriers formed near the top- and bottom-gate channels. Thus, the DG device exhibited a steeper subthreshold swing (160 mV/dec) than the SG one (329 mV/dec). For this reason, the DG structure was more able to accomplish the purpose of enhancing the controllability of the JL devices at the same channel thickness, and it also eliminated the issues of ultrathin thickness and uniformity. In the end, when the gate voltage was larger than the flat-band voltage, the accumulated carriers were increased at the channel surface. The simulation result of the DG JL devices shows that they could induce more carriers than the SG ones at the accumulation region. As an experiment result, the DG devices achieved a lower off-current (1.3×10^{-13} A) than the SG ones (2.1×10^{-12} A). Consequently, the DG JL device exhibited large on-current and on/off current ratio.

SG and DG planar JL TFTs have been successfully fabricated via a simple process with in situ-doped polycrystalline silicon by LPCVD. The DG JL TFT enhanced the gate controllability; hence, the electrical characteristic exhibited a superior subthreshold swing of 160 mV/dec, which is lower than 329 mV/dec for SG ones. Following the simulation result, the channel electron density of the DG structure was lower than that of the SG structure at the depletion region ($V_g < V_{th}$), and the DG structure could induce more carriers at the channel interface at the accumulation region ($V_g \gg V_{FB}$). Therefore, the DG structure achieved a higher on/off current ratio (1.1×10^7) than the SG ones (1.4×10^5). Consequently, the DG structure eliminated the problem of channel thickness and improved the device performance. These indicate that the proposed DG JL TFTs are promising for application in SOP and 3D-ICs.

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1) K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, Proc. IEEE **89**, 602 (2001).
2) T. Morita, AMLCD Tech. Dig., 1995, p. 1.
3) K. Yoneda, R. Yokoyama, and T. Yamada, VLSI Circuits Symp. Dig., 2001, p. 85.
4) T. Nishibe and H. Nakamura, SID Symp. Dig. Tech. Pap. **37**, 1091 (2006).
5) C. S. Tan, W. T. Sun, S. H. Lu, C. H. Kuo, I. T. Chang, S. H. Yeh, C. C. Chen, L. Liu, Y. C. Lin, and C. S. Yang, SID Symp. Dig. Tech. Pap. **36**, 336 (2005).
6) B. Lee, Y. Hirayama, Y. Kubota, S. Imai, A. Imaya, M. Katayama, K. Kato, A. Ishikawa, T. Ikeda, Y. Kurokawa, T. Ozaki, K. Mutaguch, and S. Yamazaki, ISSCC Tech. Dig., 2003, p. 164.
7) S. M. Jung, J. Jang, W. Cho, H. Cho, J. Jeong, Y. Chang, J. Kim, Y. Rah, Y. Son, J. Park, M. S. Song, K. H. Kim, J. S. Lim, and K. Kim, IEDM Tech. Dig., 2006, p. 37.
8) E.-K. Lai, H.-T. Lue, Y.-H. Hsiao, J.-Y. Hsieh, C.-P. Lu, S.-Y. Wang, L.-W. Yang, T. Yang, K.-C. Chen, J. Gong, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, IEDM Tech. Dig., 2006, p. 41.
9) T. Skotnicki, G. Merckel, and T. Pedron, IEEE Electron Device Lett. **9**, 109 (1988).
10) Y. Taur, IBM J. Res. Dev. **46**, 213 (2002).
11) T. Fukano, T. Ito, and H. Ishikawa, IEDM Tech. Dig., 1985, p. 224.
12) P. Vittorio, S. Corrado, F. Guglielmo, and M. Luigi, Appl. Phys. Lett. **77**, 552 (2000).
13) J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. **5**, 225 (2010).
14) C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge, Solid-State Electron. **54**, 97 (2010).
15) P. Singh, N. Singh, S. Member, J. Miao, W.-T. Park, and D.-L. Kwong, IEEE Electron Device Lett. **32**, 1752 (2011).
16) J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, Appl. Phys. Lett. **96**, 073510 (2010).
17) J. T. Park, J. Y. Kim, and J. P. Colinge, Appl. Phys. Lett. **100**, 083504 (2012).
18) J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan, P. Razavi, R. Yan, and R. Yu, Sci. Adv. Mater. **3**, 477 (2011).
19) C. W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti, and J. P. Colinge, IEEE Trans. Electron Devices **57**, 620 (2010).
20) C. W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J. P. Colinge, Appl. Phys. Lett. **96**, 102106 (2010).
21) D. I. Moon, S. J. Choi, J. P. Duarte, and Y. K. Choi, IEEE Trans. Electron Devices **60**, 1355 (2013).
22) C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Appl. Phys. Lett. **94**, 053511 (2009).
23) S. Barraud, M. Berthomé, R. Coquand, M. Cassé, T. Ernst, M. P. Samson, P. Perreau, K. K. Bourdelle, O. Faynot, and T. Poiroux, IEEE Electron Device Lett. **33**, 1225 (2012).
24) S. J. Choi, D. I. Moon, S. Kim, J. P. Duarte, and Y. K. Choi, IEEE Electron Device Lett. **32**, 125 (2011).
25) R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, IEEE Electron Device Lett. **32**, 1170 (2011).
26) P. Francis, A. Terao, D. Flandre, and F. Van de Wiele, IEEE Trans. Electron Devices **41**, 715 (1994).
27) J. P. Duarte, S. J. Choi, and Y. K. Choi, IEEE Trans. Electron Devices **58**, 4219 (2011).
28) C. J. Su, T. I. Tsai, Y. L. Liou, Z. M. Lin, H. C. Lin, and T. S. Chao, IEEE Electron Device Lett. **32**, 521 (2011).
29) H. C. Lin, C. I. Lin, and T. Y. Huang, IEEE Electron Device Lett. **33**, 53 (2012).
30) H. C. Lin, C. I. Lin, Z. M. Lin, B. S. Shie, and T. Y. Huang, IEEE Trans. Electron Devices **60**, 1142 (2013).