A Novel 3D Integration Scheme for Backside Illuminated CMOS Image Sensor Devices

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***Abstract*—A novel backside-illuminated CMOS image sensor (BSI-CIS) scheme and process are developed and demonstrated. This innovative scheme can be realized without fusion oxide bonding and through-silicon via (TSV) fabrication. This wafer-level TSV-less BSI-CIS scheme includes transparent ultrathin silicon ($\sim$ 3.6 μm) and uses several bonding technologies. The characterization and assessment results indicate that the integration scheme possesses excellent electrical integrity and reliability. In addition, good quality results of the image functional test demonstrate the excellent performance of this scheme. This novel scheme also provides a realizable low-cost solution for the next-generation CIS and further 3-D novel BSI-CIS scheme.**

***Index Terms*—CMOS image sensor, backside illuminated, 3D integration.**

I. Introduction

THREE-DIMENSIONAL integrated circuit (3D IC) provides a promising solution to extend beyond Moore's Law in the next generation semiconductor technology. In addition, it could be extensively applied for the different products such as CMOS imager sensor (CIS) module, MEMS, LED, memory stacking, and logic/memory stacking. Among these CIS has been led into mass production by using through-silicon via (TSV) wafer-level package. There are two different schemes for CIS. One is front side illuminated (FSI) [1], [2], and the other is backside illuminated (BSI) [3]–[7] image sensor. The traditional FSI-CIS has suffered the quantum efficiency issue [8] as the pixel size down to less than 1.4 μm. In FSI-CIS, the metal interconnects are formed above the sensing area, which leads to a narrow optical path and makes worse sensitivity (fill factor $< 50\%$) as pixel size becomes smaller and smaller. The quantity of the input light is only half compared with BSI-CIS which makes the sensing area above the metal interconnects.

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For the BSI-CIS process, the CIS wafer is generally bonded to a carrier wafer by oxide-oxide fusion bonding and followed by a high temperature ($> 300\,^{\circ}$C usually) annealing [9]–[11]. In order to obtain a good bonding quality and strength, chemical-mechanical polishing (CMP) is necessary to obtain a surface roughness less than 1 nm. After bonding, the CIS wafer is thinned down to few microns, and followed by color filter formation and glass bonding for protection. Subsequently, the carrier wafer is thinned and the TSVs are fabricated for power and signal interconnection. However, the oxide fusion bonding is an expensive and complex process inclusive of PECVD oxide, CMP, surface clean, plasma activation, wafer bonding, and post-bond annealing. In addition, the processes for TSV fabrication are also very complex and expensive. In this paper, we demonstrate a novel BSI-CIS structure and process, where no carrier wafer required and the complex fusion bonding and TSV fabrication processes can be skipped accordingly. The electrical characteristics and reliability assessment of this scheme are also investigated and discussed in the paper.

II. Structural Design and Comparison

In BSI-CIS, as shown in Fig. 1(a), the CIS wafer is generally attached to a carrier TSV wafer by oxide-oxide fusion bonding, followed by a high temperature ($> 300\,^{\circ}$C) annealing [4]–[6]. For good bonding quality and strength, chemical-mechanical polishing (CMP) is necessary to obtain a surface roughness less than 1 nm. After bonding, the CIS wafer is thinned down to few microns, followed by color filter formation and glass bonding for protection. Finally, carrier wafer thinning and TSV fabrication are performed to complete process. However, this scheme includes the oxide fusion bonding and TSV fabrication, both are costly and complicated.

Compared to Fig. 1(a), Fig. 1(b) shows our novel BSI-CIS scheme. With the wafer handling technology, the innovative scheme can be realized without the complex fusion bonding and TSV fabrication processes. As the process steps shown in Fig. 1, where the italic type (blue color) presents the different process required, this novel TSV-less scheme simplifies the steps significantly, which can lead the fabrication cost reduced greatly. The thermal budget and stress can be saved with low temperature ($< 200\,^{\circ}$C) adhesive bonding instead of high temperature ($> 300\,^{\circ}$C) annealing for oxide fusion bond. In addition, without the carrier TSV wafer, the overall thickness of this CIS module can be reduced significantly for future 3D applications.

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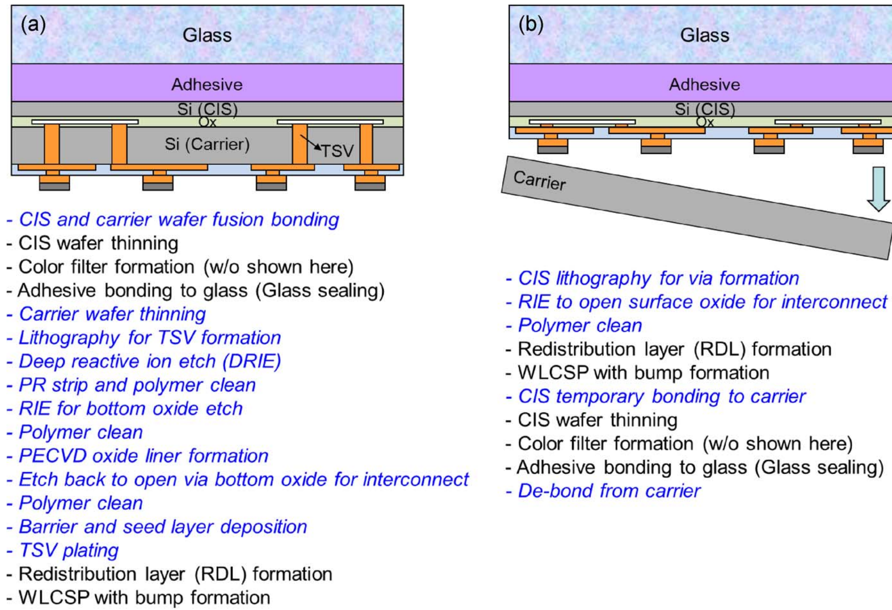

Fig. 1. Structural design and process comparison between (a) conventional and (b) our novel BSI-CIS scheme. The italic wording presents the different processes required in these two schemes, which indicates the novel BSI-CIS scheme simplifies process steps significantly.

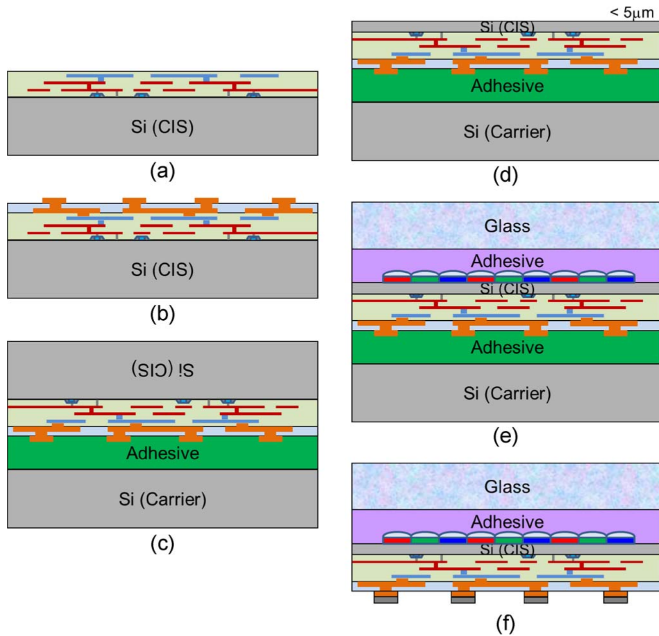

Fig. 2. The schematic process flow of the novel TSV-less BSI-CIS structure, including the following steps: (a) CIS wafer with photodiode and multilayer metallization; (b) WLCSP with RDL and bump formation; (c) CIS temporary bonding to carrier; (d) CIS wafer thinning down to less than 5 μm; (e) color filter formation and glass sealing; and (f) carrier de-bond and soldering.

III. Process and Integration Demonstration

Fig. 2 shows the detailed schematic process flow of this TSV-less BSI-CIS structure: (a) CIS wafer is prepared with photodiode formation and multilayer metallization; (b) the passivation is opened to reveal the metal pads, followed by WLCSP with redistribution layer (RDL) and Ti/Cu under-bump metallization (UBM) formation; (c) CIS wafer is then temporarily bonded to a silicon carrier with adhesive material; (d) CIS wafer is thinned down to less than 5 μm; (e) the ultra-thinned CIS wafer is executed color filter formation, and then permanently bonded to a 500 μm glass wafer for the sensing area protection and handling carrier; (f) with the backside glass wafer handling, the front side silicon carrier is de-bonded followed by the solder bump formation on top of CIS wafer for I/O fan out interconnect.

Critical process and integration steps are presented in Fig. 3. Fig. 3(a) shows the fabricated CIS wafer with RDL and Cu pad formation. The micro-bump is processed at the front side of the wafer after sputtering. The wafer then is temporarily bonded to a silicon carrier with HT-10.10, a thermal plastic material from Brewer Science. Next, the CIS is thinned down to less than 5 μm by DISCO grinding and CMP system. It should be noted that the total thickness variation (TTV) control after temporary bonding is very important, as shown in Fig. 3(b). Fig. 3(c) shows the ultra-thinned wafer without any chipping and cracks. This CIS wafer is then permanently bonded to a 500-μm-thick glass wafer for the sensing area protection and handling. After edge cutting treatment, the silicon carrier is de-bonded by SUSS DB12T de-bonder, and then the CIS surface is cleaned by SUSS AR12 cleaner. Finally, 30-μm-diameter and 3-μm-thick Cu/Sn micro-bumps are formed on the front side of the CIS based on the pre-sputtered Ti/Cu UBM, as shown in Fig. 3(d). Fig. 3(e) presents the completed 300 mm TSV-less BSI-CIS wafer with well-developed process and integration. With ultra-thin silicon, the final wafer is visible-light transparent as Fig. 3(f) presents. Therefore, without oxide fusion bonding and TSV fabrication, this scheme successfully provides a potential low cost solution for BSI-CIS applications.

IV. Electrical Characterization and Reliability Assessment

In this study, the packaged BSI-CIS module was assembled onto a silicon interposer substrate by flip chip bonding

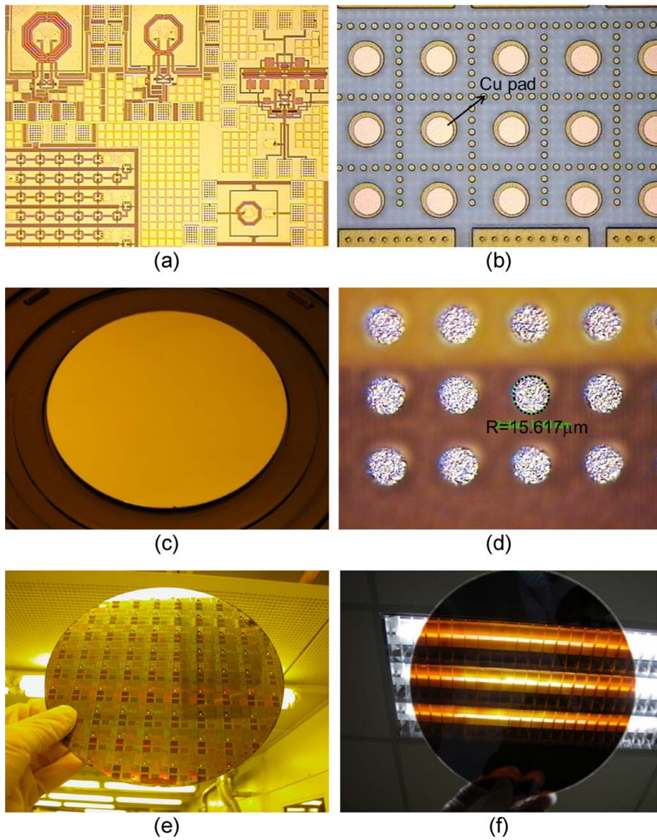

Fig. 3. Process and integration demonstration of TSV-less BSI-CIS scheme, including the following steps: (a) CIS wafer with circuits and metallization; (b) WLCSP with RDL and Cu pad formation, and ready for temporary bonding; (c) CIS wafer thinning to < 5 μm without any chipping and cracks; (d) 30-μm-diameter Cu/Sn micro-bump formation on the front side of the CIS; (e) a completed TSV-less BSI-CIS wafer-level packaging; and (f) demonstration of transparent BSI-CIS with ultra-thinned silicon.

technology. The silicon substrate was prepared with RDL, electroless nickel, and immersion gold (ENIG) UBM formation. Fig. 4(a) shows the assembled CIS/substrate bonding module. Daisy chain feature and Kelvin structure were designed in the scheme for electrical characterization and reliability assessment. Fig. 4(b) shows the cross-sectional SEM image of the ultra-thin silicon ($\sim$3.6 μm) BSI-CIS bonding with substrate through the Cu/Sn micro-bump and ENIG UBM.

The characteristics and reliability of the bonding module were analyzed. Agilent 4156C probe station with four-point probes was adopted for electrical measurement. The bond chain structure with a series of Cu RDL and Cu/Sn/ENIG micro-joint interconnect was applied to investigate the electrical characteristics of the integrated scheme, and the results are shown in Fig. 5(a). The linear characteristic of total resistance versus number of bond chain indicates excellent bonding integrity and electrical performance. Fig. 5(b) shows the stable electrical performance of four different structures under current stressing. In addition, the characteristic of micro-joint interconnect was investigated by Kelvin structure, and the results show the contact resistance of single 30-μm-diameter Cu/Sn/ENIG bonded interconnect is about 1.26 mΩ.

The bonded structure was fabricated for multiple cycles of current stressing test, preconditioning test (JESD22-A113D,

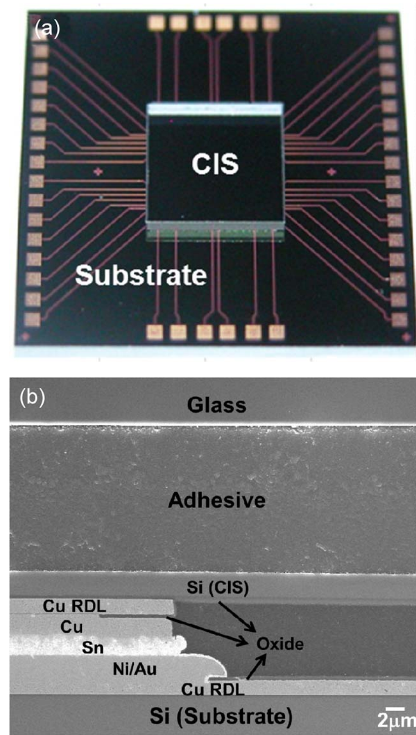

Fig. 4. (a) Integrated CIS/Si substrate module. (b) SEM image of bonded structure.

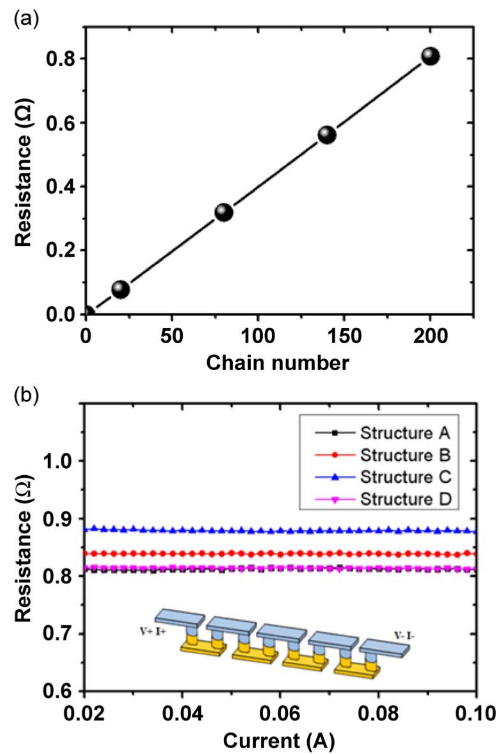

Fig. 5. (a) Electrical characteristic of total resistance under different chain numbers. (b) Electrical performances of four different structure designs.

LV3), and temperature cycling test (TCT) (JESD22-A104B) for reliability assessment. Fig. 6(a) and (b) shows the excellent electrical stability even after 1000 cycles current stressing. The test conditions of preconditioning and TCT are indicated in Table I.

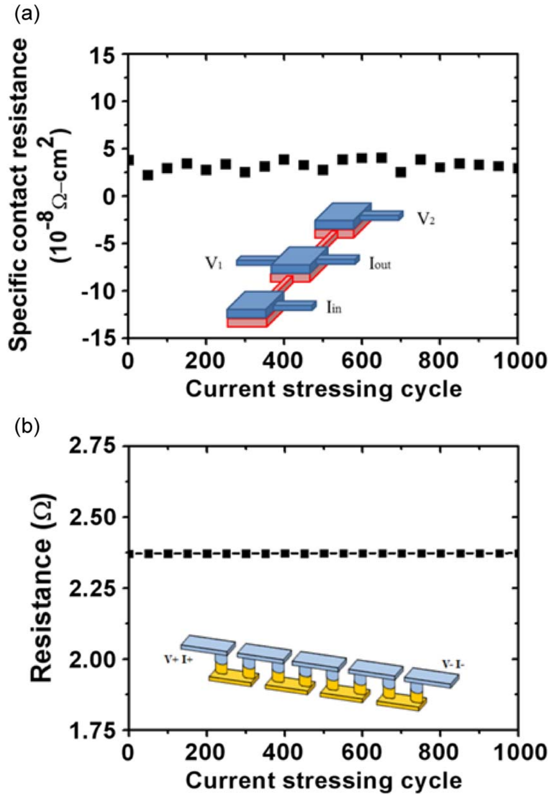

Fig. 6. (a) Specific contact resistance results under multiple current stressing. (b) Daisy chain measurement results under multiple current stressing.

TABLE I
THE TEST CONDITIONS OF PRECONDITIONING AND TCT RELIABILITY ASSESSMENT

Item	Test condition
Preconditioning	Baking (125°C, 24 hrs) → Soaking (30°C /60%RH, 192 hrs) → Reflow (260°C, 3 times)
TCT	-55°C ~ 125°C, 3000 cycles, Dwell time = 5 mins, Ramp rate =15°C / min

As the results shown in Fig. 7(a), these structures can pass 1000 cycles of TCT test without apparent resistance variation. The small specific contact resistance of single bonded interconnect is even reduced from 3.94E-8 Ω-cm^2 to 2.42E-8 Ω-cm^2 after 1000 cycles of TCT as Fig. 7(b) presents. The reduction may come from the improvement of bonded interface, such as the grain growth and removal of defects [12]. These assessment results indicate that the integration scheme possesses excellent reliability and electrical stability, which is beneficial for the further 3D integrated imager applications.

V. CMOS Image Sensor Functional Test

The integrated CIS module was verified with the image functional test. Fig. 8(a) shows the developed system for the image functional test, and Fig. 8(b) presents the image output result. Herein the CIS device was fabricated with 0.18 μm generic 1P6M CMOS technology from TSMC, and packaged with our novel TSV-less BSI-CIS WLP scheme. The pixel size is 3 μm with three mega pixels (2048 $\times$ 1536) resolution. Because the color filter formation was skipped, the image is black-white color only. However, the image function is successfully verified with good quality, which indicates the excellent performance with this novel scheme and process integration. Based on these results, this novel 3D-integration BSI-CIS scheme, including analog-to-digital converter (ADC) and image signal processor (ISP) integration with specific array design, can be fabricated for a possible high resolution and frame rate ($>$ 100 fps) application.

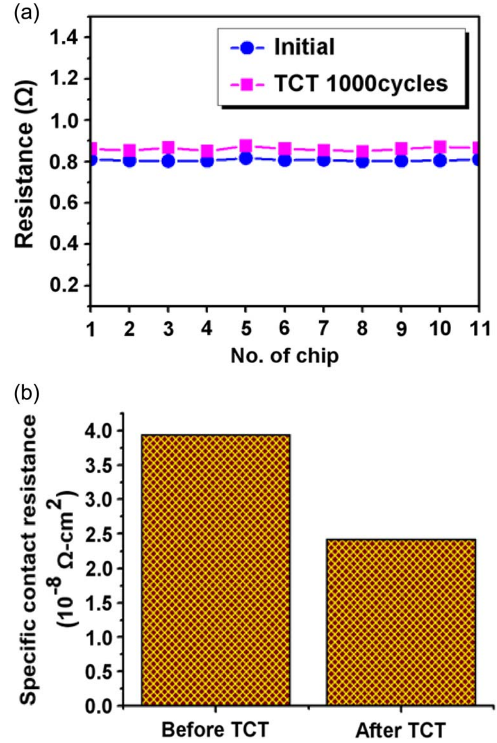

Fig. 7. (a) Resistance values before and after TCT. (b) Measurement results of specific contact resistance before and after TCT.

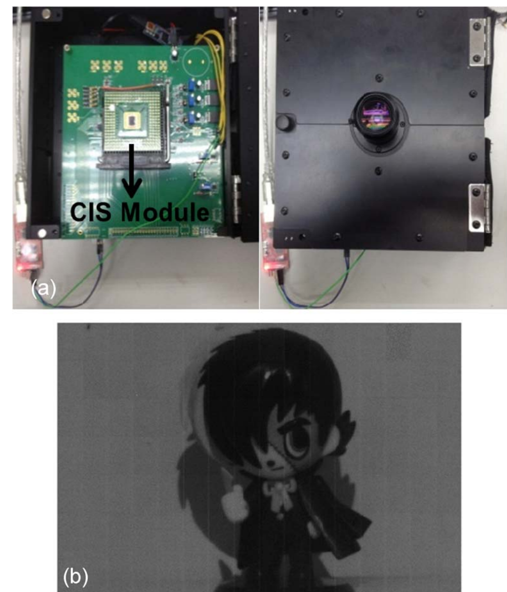

Fig. 8. (a) System development and set-up for the image functional test. (b) Image output result.

VI. Conclusion

In this study, we successfully develop and demonstrate a novel BSI-CIS structure and process flow based on 3D integration technologies. The innovative scheme can be realized without the complex fusion bonding and TSV fabrication processes. The characteristics and reliability of the scheme are investigated, indicating excellent integration integrity and reliability. In addition, the image function is successfully verified with good quality, which indicates the excellent performance as well. This scheme provides a realizable low cost solution for the next generation CIS and further 3D integrated imager applications.

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