Optimization on Layout Style of Diode Stackup for On-Chip ESD Protection

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***Abstract*—The diode stackup has been used as on-chip electrostatic discharge (ESD) protection for some applications in which the input/output signal swing is higher than V_{DD} or lower than V_{SS}. A novel ESD protection structure of diode stackup is proposed for effective on-chip ESD protection. Experimental results in 65-nm CMOS process show that the optimization on layout style can improve the ESD robustness, decrease the turn-on resistance, and lessen the parasitic capacitance of the diode stackup.**

***Index Terms*—Diode, electrostatic discharge (ESD), layout, stackup.**

I. Introduction

CMOS technologies have been widely used to design and fabricate all kinds of integrated circuits due to the advantages of high integration and potential for mass production. However, the integrated circuits realized in CMOS technologies are susceptible to electrostatic discharge (ESD) events that may damage the IC products. Therefore, on-chip ESD protection must be equipped for the pads that may be stressed by ESD, including the input/output (I/O) pads. A typical specification for IC products on human-body-model (HBM) ESD robustness was 2 kV [1].

Diode has been used as an effective on-chip ESD protection device due to the small parasitic loading effect and high ESD robustness [2]. To adapt for some applications in which the I/O signal swing is higher than V_{DD} or lower than V_{SS}, such as the neural stimulator [3] or power amplifier [4], the diode stackup was attached to the I/O pads, as shown in Fig. 1 [5]. However, the diode stackup is adverse to ESD protection because the overall turn-on resistance and the clamping voltage of the diodes during ESD stresses are increased. In this letter, an optimization on layout style of diode stackup was proposed for on-chip ESD protection. The diode stackup with two diodes will be studied. The target of this design includes low turn-on resistance, low parasitic effects, and high ESD robustness.

II. Conventional Diode Stackup

The layout top view and the device cross-sectional view of the conventional diode stackup are shown in Figs. 2 and 3, respectively. In Figs. 2(a) and 3(a), two STI-bound P+/N-well diodes can apply to I/O-to-V_{DD}. In Figs. 2(b) and 3(b), two STI-bound P-well/N+ diodes can apply to V_{SS}-to-I/O. The deep N-well structure is needed to isolate the P-well from the common P-substrate.

Manuscript received November 30, 2013; accepted March 7, 2014. Date of publication March 11, 2014; date of current version June 3, 2014. This work was supported by Taiwan Semiconductor Manufacturing Company (TSMC); by the National Science Council, Taiwan, under Contract NSC 102-2220-E-003-001; and by the "Aim for the Top University Plan" of the National Chiao Tung University and Ministry of Education, Taiwan.

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Digital Object Identifier 10.1109/TDMR.2014.2311130

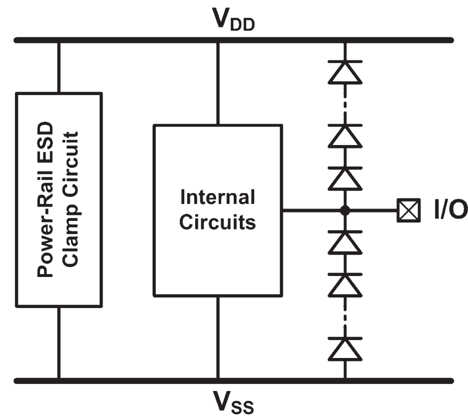

Fig. 1. ESD protection circuit with diode stackup at I/O pads.

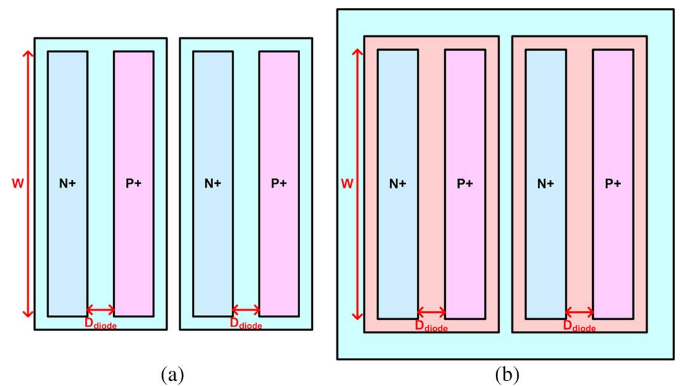

Fig. 2. Layout top view of conventional (a) P diode stackup and (b) N diode stackup.

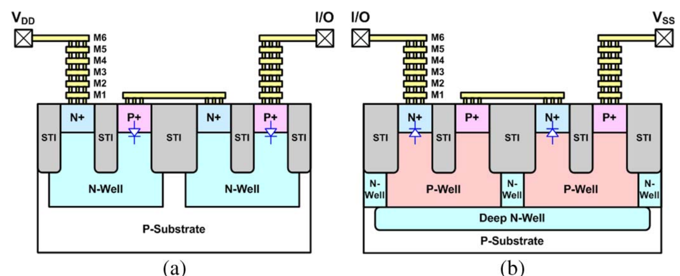

Fig. 3. Cross-sectional view of conventional (a) P diode stackup and (b) N diode stackup.

III. Optimization on Layout Style of Diode Stackup

In this work, the novel diode stackup combines one P+/N-well diode and one P-well/N+ diode. The layout top view and the device cross-sectional view of the novel diode stackup are shown in Figs. 4 and 5, respectively. This diode stackup can apply to I/O-to-V_{DD} or V_{SS}-to-I/O. The ESD current path along the A-A′ direction consists of the P+/N-well diode and the P-well/N+ diode. The ESD current path along the B-B′ direction consists of the P+/N-well/P-well/N+ silicon-controlled rectifier (SCR). The SCR device has been reported to be useful for ESD protection with low turn-on resistance, low parasitic effects, and high ESD robustness [6]. The width of diode path (T) is defined as the sum of all segments of t in Fig. 4, and the width of SCR

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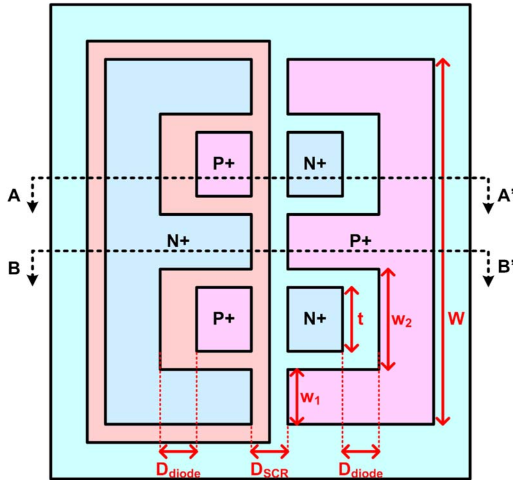

Fig. 4. Layout top view of novel diode stackup.

path (W) is the sum of all segments of w_1 and w_2. In the beginning of ESD stress, the diode path (A-A′) will turn on to discharge the initial current, and then, the SCR path (B-B′) will take over to discharge the primary current. The diode path also plays the role of trigger circuit of the SCR device, because the current drawn from the N-well (injected into P-well) of diode can also trigger the parasitic PNP (NPN) of SCR. Since the primary ESD current is designed to be discharged through the SCR path in this structure, the distance from anode to cathode of SCR (D_{SCR}) is wished to be minimized. The turn-on resistance of SCR can be lowered by using this layout style.

IV. Experimental Results

The test devices of conventional and novel diode stackup have been fabricated in a 65-nm CMOS process. To facilitate two-port measurement on a probe station, the test devices are arranged with ground-signal-ground (GSG) pads. The P diode stackup and N diode stackup with a single finger of W = 40 μm are implemented for reference. The distance from anode to cathode of each diode (D_{diode}) is 0.2 μm. The top metal (M6 in the given CMOS process) is used for connecting between the devices and pads, while the bottom metal (M1) is used for connecting between two diodes, as shown in Fig. 3.

The widths of the novel diode stackup (W) are arranged as 20 μm, 30 μm, and 40 μm. The dimensions of diode path (T) are equal to W, W/4, or W/8. The distance from anode to cathode of SCR (D_{SCR}) is 0.32 μm. The metal routing style of the novel diode stackup is identical to that of the conventional diode stackup, so the difference caused by the metal routing can be ignored. It should be noted that the contacts in the center of Fig. 5(b) are removed. All these dimensions of test devices are listed in Table I.

A. Parasitic Capacitance

The two-port S-parameters of the test devices are measured on wafer. The parasitic effects of the GSG pads and metal routing have been removed by using the de-embedding technique [7]. The parasitic capacitance of each test device was extracted from the S-parameters. Fig. 6 shows the extracted parasitic capacitances of the test devices from 1 to 30 GHz. The parasitic capacitances of the novel diode stackup with W = 20 μm/30 μm/40 μm are about 20 fF/30 fF/40 fF, respectively. With the narrower T, which is identical to the narrowed w_2 and the widened w_1, the parasitic capacitances are slightly increased.

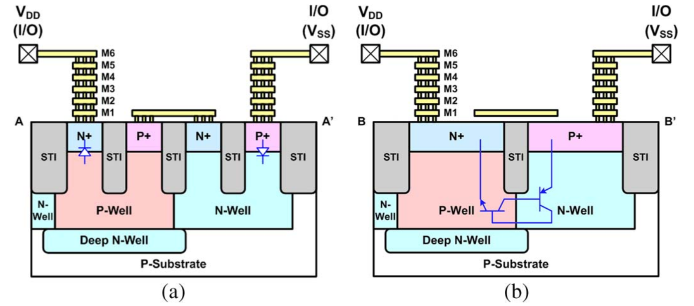

Fig. 5. Cross-sectional view of novel diode stackup along (a) A-A′ and (b) B-B′.

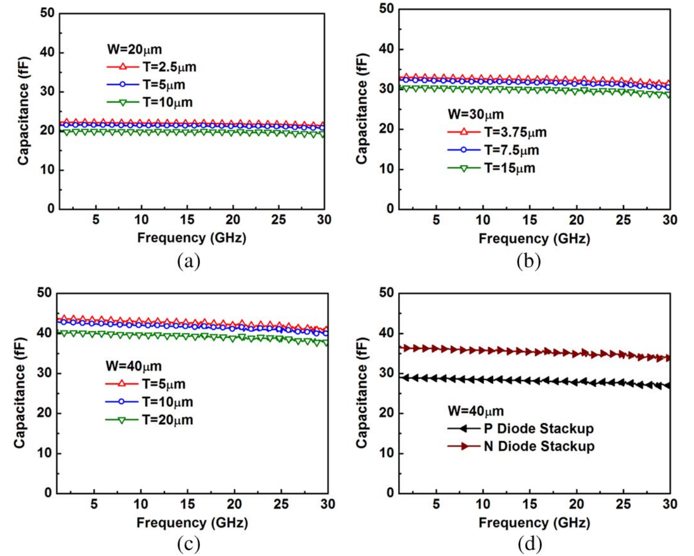

Fig. 6. Measured parasitic capacitances of novel diode stackup with (a) W = 20 μm, (b) W = 30 μm, and (c) W = 40 μm, and those of conventional diode stackup with (d) W = 40 μm.

B. ESD Robustness

The HBM ESD robustness of the test devices are evaluated by the ESD tester. All these measured ESD robustness are listed in Table I. According to the measurement results, the novel diode stackup with W = 40 μm and T = 5 μm can pass 3.5 kV HBM ESD tests, while the P diode stackup or N diode stackup with the same width has only 1.5 kV HBM ESD robustness. The novel diode stackup with the narrower T, which is identical to the narrowed diode path and the widened SCR path, has the better ESD robustness.

To investigate the turn-on behavior and the *I–V* characteristics in high-current regions of the test devices, the transmission-line-pulsing (TLP) system is used to measure the *I–V* characteristics, as shown in Fig. 7. The trigger voltage (V_{t1}) and the turn-on resistance (R_{on}) of all test devices are summarized in Table I. Besides, the current compression point (I_{CP}), which is defined as the current level deviates from the linearly extrapolated low-current curve by 20% [8], of the test devices are also summarized in Table I.

The ratio of HBM ESD robustness and parasitic capacitance and the product of turn-on resistance and parasitic capacitance of the test devices are compared in Table I. The novel diode stackup has the better ratio and product.

Another very-fast-TLP (vfTLP) system is used to measure the *I–V* characteristics of the test devices in faster ESD-transient events, as shown in Fig. 8. The novel diode stackup is fast enough to be turned on under such a fast-transient pulse to improve the ESD robustness.

TABLE I
DEVICE DIMENSIONS AND MEASUREMENT RESULTS OF TEST DEVICES

Structure	W (μm)	T (μm)	D_{SCR} (μm)	C@2.4 GHz (fF)	TLP V_{t1} (V)	TLP R_{on} (Ω)	TLP I_{CP} (A)	HBM (kV)	HBM / C@2.4GHz (V/fF)	TLP R_{on}× C@2.4GHz (Ω×fF)
Novel	20	2.5	0.32	22.3	1.29	1.19	0.72	1.75	78.5	26.5
		5		21.5	1.30	1.24	0.67	1.50	69.8	26.7
		10		19.9	1.62	1.62	0.60	1.25	62.8	32.2
	30	3.75		33.0	1.30	1.02	1.20	2.50	75.6	33.7
		7.5		32.3	1.30	1.17	1.16	2.25	69.7	37.8
		15		30.4	1.60	1.35	1.00	2.00	65.8	41.0
	40	5		43.6	1.30	0.66	1.66	3.50	80.3	28.8
		10		42.7	1.30	0.76	1.62	3.25	76.1	32.5
		20		40.2	1.58	1.12	1.45	2.75	68.4	45.0
P Diode Stackup	40	N/A	N/A	28.9	1.61	3.02	0.91	1.50	51.9	87.3
N Diode Stackup	40	N/A	N/A	36.3	1.61	3.14	0.90	1.50	41.3	114.0

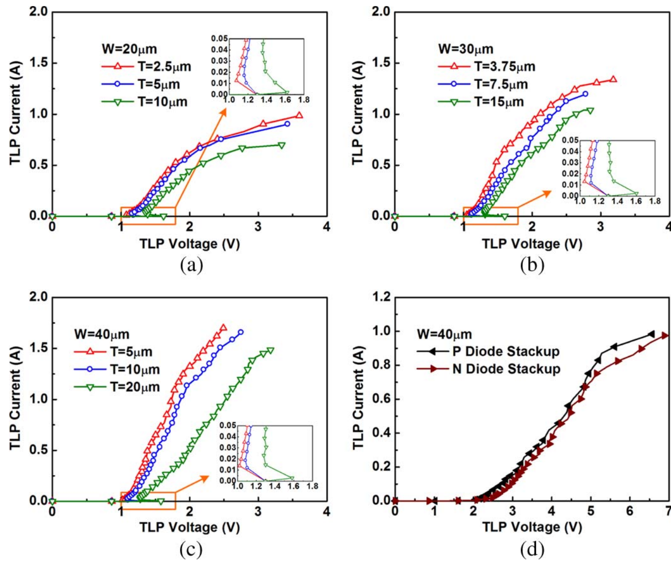

Fig. 7. Measured TLP I–V curves of novel diode stackup with (a) W = 20 μm, (b) W = 30 μm, and (c) W = 40 μm, and those of conventional diode stackup with (d) W = 40 μm.

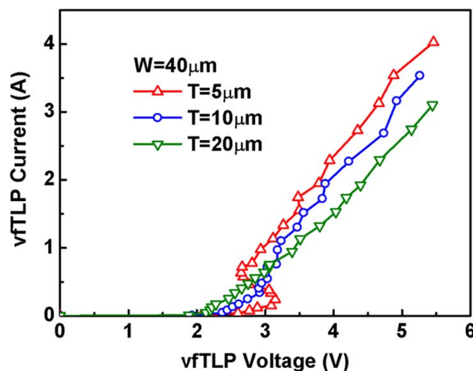

Fig. 8. Measured vfTLP I–V curves of novel diode stackup with W = 40 μm.

V. CONCLUSION

The novel diode stackup with two diodes has been designed, fabricated, and characterized in a 65-nm CMOS process. The optimization on layout style of diode stackup is more suitable for ESD protection due to its low turn-on resistance, low parasitic capacitance, and high ESD robustness. This layout style can be extended to the diode stackup with more diodes.

ACKNOWLEDGMENT

The authors would like to thank Prof. M.-D. Ker, National Chiao Tung University, Taiwan, and M.-H. Song, J.-C. Tseng, L.-W. Chu, K.-J. Chen, S.-M. Cheng, B.-T. Chen, C.-P. Jou, and M.-H. Tsai, Taiwan Semiconductor Manufacturing Company, for their valuable suggestions during circuit design. They would also like to thank TSMC for chip fabrication.

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