14 GSps Four-Bit Noninterleaved Data Converter Pair in 90 nm CMOS With Built-In Eye Diagram Testability

Hao-Chiao Hong, *Senior Member, IEEE,* Yung-Shun Chen, and Wei-Chieh Fang

***Abstract*— This paper presents the design and test of a 14 GSps, four-bit data converter pair in 90 nm CMOS suitable for implementing advanced serial links. The data converter pair consists of a noninterleaved flash analog-to-digital converter (ADC) and a noninterleaved current-steering digital-to-analog converter (DAC). Both the converter designs adopt the wave-pipelining technique to increase the available signal settling time. Through detailed analysis, we show that cascading three active feedback preamplifiers to implement the cores of the comparators in the ADC balances the power budget and the design difficulty when we push the sampling rate to the process limit. Current mode logic gates are used to alleviate the power bouncing issue. To address the difficulty and high cost of testing the extremely high-speed converters, the design embeds the simple design-for-testability circuits cooperating with the on-chip resources to provide two cost-effective test modes. The first test mode cascades the ADC and DAC so that they can be tested at the rated speed without the need of a very high speed logic analyzer. The second test mode enables the eye diagram tests by shuffling the digital outputs of ADC as the inputs of the DAC instead of adopting conventional linear feedback shift register. The experimental results show that the cascaded ADC and DAC pair achieves a 31.0 dBc spurious-free dynamic range and a 25.9 dB signal-to-noise-and-distortion ratio with a 1.11 GHz, −1 dBFS stimulus at 14 GSps. The ADC and DAC consume 214 mW and 85 mW from a 1.0-V supply and occupy 0.1575 mm^2 and 0.0636 mm^2, respectively.**

***Index Terms*— Analog-to-digital converter (ADC), design-for-testability, digital loopback, digital-to-analog converter (DAC), eye diagram test, high-speed.**

I. Introduction

SERIAL links become the main stream of modern wired or wireless communication systems because of their cost effectiveness and power efficiency [1]. Commercial products such as PCI-Express and Serial ATA accommodate data rates over Gb/s. The IEEE Standard 802.3ba-2010 further defines 40 Gb/s and 100 Gb/s Ethernet [2]. Without doubt, the endless demands for faster and faster communication and the continuously advancing technology push the data rates of future serial links higher than ever.

Two fundamental factors would limit the enhancement of the data rate: the intrinsic bandwidth of the transmission medium and unavoidable noise. According to the Shannon–Hartley theorem, an error-correction coding scheme that provides a channel capacity of C bits per second through a specified communication channel exits. Mathematically, C can be expressed as

$$C = \mathrm{BW} \log_2(1 + \mathrm{SNR}) \tag{1}$$

where BW is the bandwidth of the channel in hertz, and the SNR represents the signal-to-noise ratio (SNR) of the communication signal to the Gaussian noise interference. Given the same SNR, (1) indicates that the only way to increase the channel capacity is to increase BW. However, it is usually very costly to have a communication channel with a wider bandwidth, no matter it is wired or wireless.

An alternative to increase the channel capacity is to increase the SNR. In a panel of experts at the International Solid State Circuits Conference (ISSCC) 2009, serializer/deserializer (SerDes) chip designers argued that analog-to-digital converters (ADCs) combined with multilevel coding techniques enable lower cost designs, following the successful pattern set by the digital subscriber line and voice-band modems years ago [3].

High-speed ADCs and digital-to-analog converters (DACs) with moderate resolution are the key enablers of the above idea: Enhancing the SNR term in (1) regardless of the channel bandwidth so as to increase the overall channel capacity [4], [5].

Several state-of-the-art designs have demonstrated serial-link transceivers that achieve data rates over 5 Gb/s [6]–[8]. Most of them employ the interleaved ADCs and DACs as their building blocks. Such designs relax the speed requirement of individual converter, but require more complex and accurate timing and more areas.

This paper demonstrates the design and test of a 14 GSps, four-bit ADC and DAC pair without interleaving for the design of advanced serial-link transceivers. To address the difficulty and high cost of conducting at-speed tests and eye diagram tests of these extremely fast converters, we also propose a low-cost design-for-testability (DfT) scheme. The reminder of this paper is organized as follows. Section II describes the detailed circuit designs of the ADC and DAC. Section III depicts the

Manuscript received January 22, 2013; revised May 2, 2013; accepted June 9, 2013. Date of publication October 7, 2013; date of current version May 20, 2014. This work was supported in part by the National Science Council, Taiwan, under Grant NSC101-2221-E009-166 and the Ministry of Economic Affairs, Taiwan, under Grant 94-EC-17-A-01-S1-002, Grant 95-EC-17-A-01-S1-037, and Grant 96-EC-17-A-01-S1-037.

H.-C. Hong is with the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: hchong@cn.nctu.edu.tw).

Y.-S. Chen and W.-C. Fang were with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: shun0316@gmail.com; wejayfang@gmail.com).

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Digital Object Identifier 10.1109/TVLSI.2013.2270362

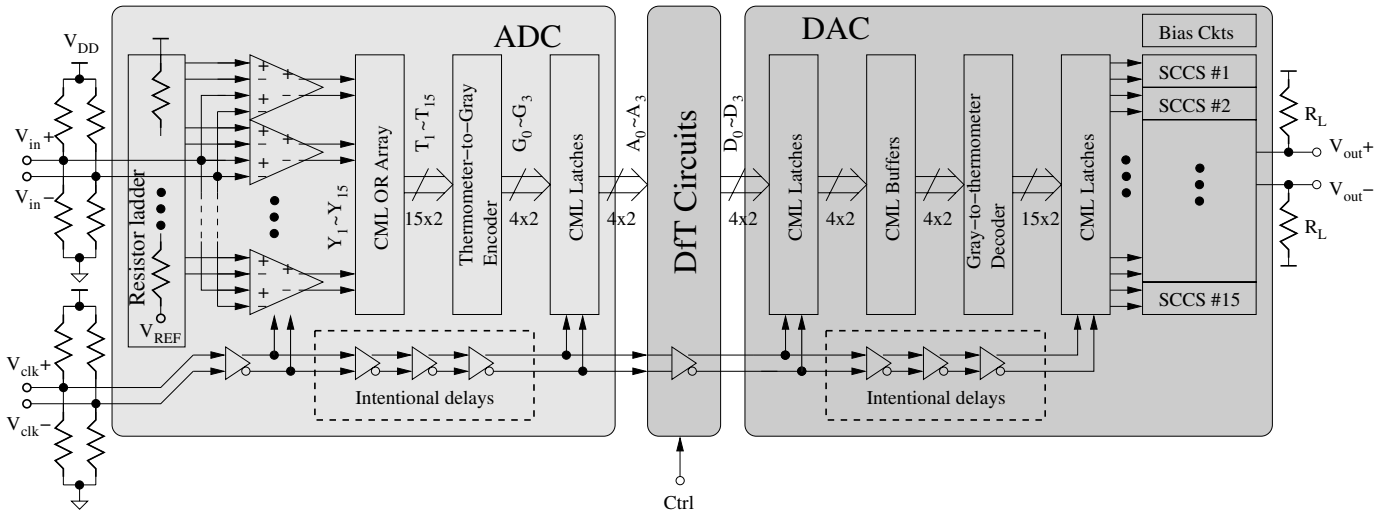

Fig. 1. Block diagram of the test chip.

DfT scheme and circuits. Measurement results are illustrated in Section IV. Finally, Section V draws our conclusions.

II. Circuit Design

Fig. 1 depicts the block diagram of our design. It consists of the four-bit flash ADC, the four-bit current-steering DAC, and the DfT circuits. All circuits including the digital circuits are realized using fully differential structures to alleviate the common-mode interference and noise. The differential input range of the ADC and the differential output range of the DAC are set to ±400 mV. It corresponds to an LSB of 50 mV.

We use the Gray codes to represent the primary outputs of the ADC and the primary inputs of the DAC. Adopting the Gray codes benefits from that a single-bit error induces less significant error to a Gray code than to a binary code. The reason is two consecutive Gray codes always differ from each other at most by one bit. Hence, a single-bit error most likely leads to an LSB difference.

A. Analog-to-Digital Converter

The ADC is a noninterleaved flash ADC without a preceding sampled-and-hold (S/H) stage similar to that in [9]. The primary inputs of ADC directly connect to two resistor dividers which provide 50-ohm terminations and bias the inputs of the ADC core at the desired voltage. The ADC core consists of 15 comparators which convert the analog inputs to the corresponding thermometer-coded outputs. The following logic OR array eliminates the single-bubble errors of the thermometer-coded outputs. Finally, the thermometer-to-Gray encoder encodes the outputs of the OR array and produces the four-bit Gray-code outputs.

1) Design of the Comparator: Each of the comparator compares the differential primary input with the corresponding differential reference voltage and produces a digital bit of the thermometer code. The main design goal of the comparator is to achieve the specified gain A_{CP} and bandwidth $\mathrm{BW_{CP}}$ with the least power.

In the worst case, the comparator must resolve a difference less than one LSB within a half clock cycle which is <36 ps. A conservative design constraint of the comparator is that a $1/\sqrt{2}$ LSB input is amplified to a full-scale digital signal. An additional conservative design constraint asks the comparator for a bandwidth as wide as the Nyquist bandwidth of the ADC. For this ADC design, the design targets are $A_{\mathrm{CP}} = 27$ dB and $\mathrm{BW_{CP}} = 7$ GHz. Realizing the comparator by a simple single-stage differential amplifier requests the amplifier to achieve a gain-bandwidth product (GBWP) >158 GHz. Such a design is not practical because the ultimate GBWP is already around the intrinsic unit-gain frequency of the MOSFET. Even if the MOSFET were fast enough, the single-stage design consumes too much power. Cascading several identical preamplifiers (PreAmps) is a low-power alternative [10], [11].

Let the comparator be implemented by cascading N identical PreAmps and every PreAmp has a bandwidth of $\mathrm{BW_{PA}}$, a dc gain of A_{PA}, and a first- or second-order transfer function. In particular, the second-order transfer function is assumed to have a maximally flat frequency response. Then, the ith-order PreAmp design should follow [10]

$$\mathrm{BW_{PA}} = \frac{\mathrm{BW_{CP}}}{\sqrt[2^i]{\sqrt[N]{2}-1}}$$
$$A_{\mathrm{PA}} = \sqrt[N]{A_{\mathrm{CP}}} \tag{2}$$

and its GBWP equals to

$$\frac{BW_{\mathrm{CP}}\sqrt[N]{A_{\mathrm{CP}}}}{\sqrt[2^i]{\sqrt[N]{2}-1}}. \tag{3}$$

Fig. 2 plots the required GBWPs for the first- and second-order PreAmps to meet the design targets according to (3). The minimal required GBWP of the first-order PreAmp is 35 GHz, while that of the second-order PreAmp is only 18 GHz. It is noteworthy that the required GBWP of the PreAmp does not keep decreasing by cascading more PreAmps in both the cases. In addition, the first-order PreAmp case requires a higher minimal GBWP. Because our design targets at pushing the sampling rate to the limit, the implementation with the second-order PreAmps is preferred from the minimized GBWP point of view.

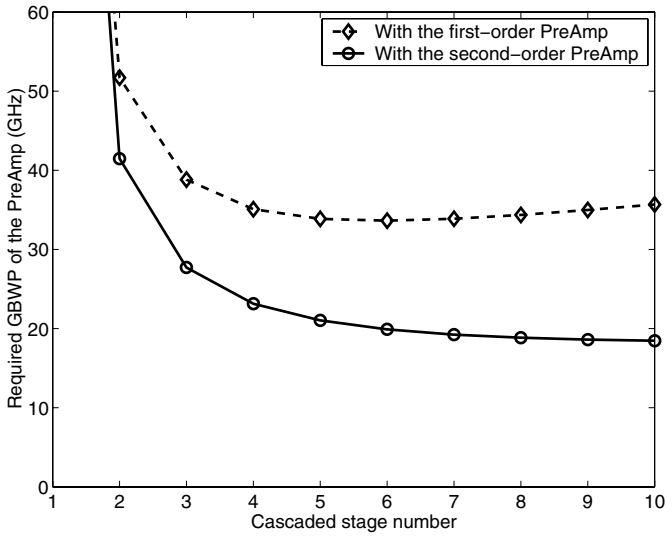

Fig. 2. Required GBWP of the PreAmp versus the cascaded stage number.

We adopted the differential amplifier with active feedback to implement the second-order PreAmp [10]. Fig. 3 shows the schematic. The active feedback configuration extends the bandwidth of the PreAmp as our desire. The transfer function of the active feedback PreAmp is shown [10] to be

$$\frac{V_o}{V_{\text{in}}} = \frac{A_{\text{PA}}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4}$$

where

$$\begin{aligned} A_{\text{PA}} &= \frac{g_{m1}g_{m2}R_{L1}R_{L2}}{1 + g_{m2}g_{mf}R_{L1}R_{L2}} \\ \zeta &= \frac{R_{L1}C_{L1} + R_{L2}C_{L2}}{2\sqrt{R_{L1}C_{L1}R_{L2}C_{L2}(1 + g_{m2}g_{mf}R_{L1}R_{L2})}} \\ \omega_n &= \sqrt{\frac{1 + g_{m2}g_{mf}R_{L1}R_{L2}}{R_{L1}C_{L1}R_{L2}C_{L2}}}. \end{aligned} \tag{5}$$

By designating $g_{m1} \simeq g_{m2} = g_m$, $R_{L1} \simeq R_{L2} = R_L$, $C_{L1} \simeq C_{L2} = C_L$, and $\zeta = 1/\sqrt{2}$, the active feedback PreAmp has the following design parameters:

$$\begin{aligned} A_{\text{PA}} &= \left(\frac{g_m R_L}{2}\right) g_m R_L \\ \text{BW}_{\text{PA}} &= \left(\sqrt{2}\right) \frac{1}{2\pi R_L C_L} \end{aligned} \tag{6}$$

where $g_m R_L$ and $1/(2\pi R_L C_L)$ can be regarded as the gain and bandwidth of a first-order PreAmp, respectively. Equation (6) explains the major benefit of adopting the active feedback PreAmp, especially when we want to achieve the ultimate sampling rate: the bandwidth is boosted by a factor of $\sqrt{2}$ comparing that of a first-order PreAmp. It is because the desired gain can always be achieved by cascading more stages while the bandwidth would not. Besides, the required GBWP of the first-order Preamp is higher than that of the second-order PreAmp according to Fig. 2. It makes the PreAmp design much difficult because of the process limitation. To sum up, the active feedback technique is useful when trying to push the comparator's speed to the limit.

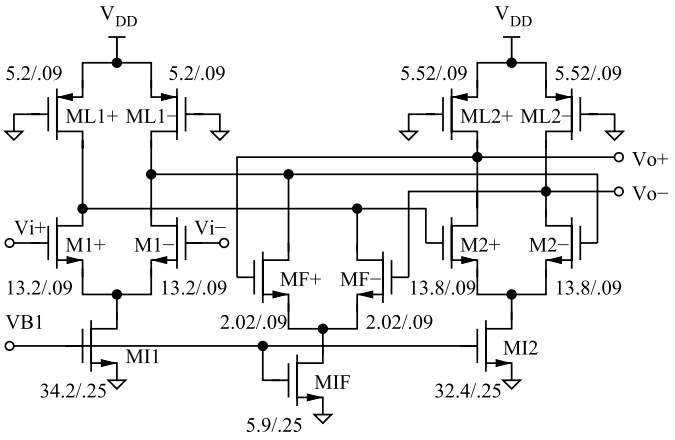

Fig. 3. Schematic of the second-order PreAmp with active feedback [10].

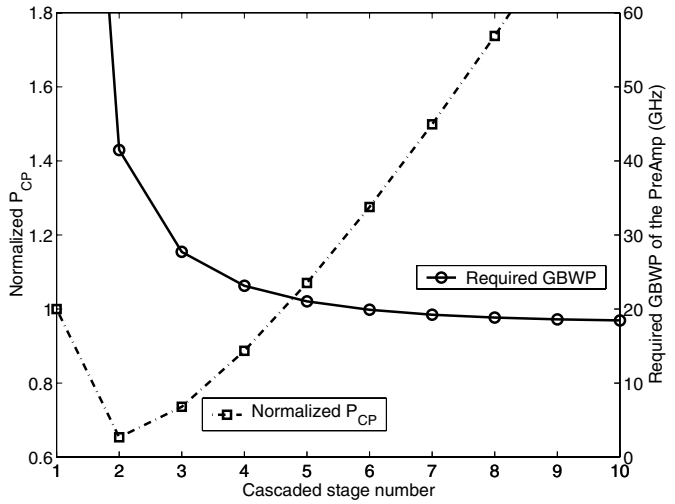

Fig. 4. Normalized P_{CP} and the required PreAmp's GBWP when the comparator is made of the second-order PreAmps.

Another design target of us is to keep a good energy efficiency. According to Fig. 2, the more the cascaded second-order PreAmps, the smaller is the GBWP that the PreAmp requires. Although a PreAmp with a smaller GBWP consumes less power, however, the total power of the cascaded chain is proportional to the stage number of the PreAmps. Consequently, there exists an optimal stage number. In our design, the active feedback PreAmp totally consumes about twice the bias current of the major current source ($MI1$) in it. Hence, the total power of the comparator is expressed as

$$\begin{aligned} P_{\text{CP}}(N) &\simeq V_{\text{DD}} N \left(4 I_{DS,M1}\right) \\ &= \frac{2V_{\text{DD}}}{\beta_n} N g_m^2 \end{aligned} \tag{7}$$

where $\beta_n = \mu_n C_{\text{ox}} W/L$ is the process transconductance parameter. Given the specified C_L and BW_{CP}, we have

$$P_{\text{CP}}(N) = \left(\frac{8\pi^2 V_{\text{DD}} C_L^2 BW_{\text{CP}}^2}{\beta_n}\right) \frac{N \sqrt[N]{A_{\text{CP}}}}{\sqrt{\sqrt[N]{2} - 1}} \tag{8}$$

according to (2), (5), and (6).

Fig. 4 plots the results of (8) normalized to $P_{\text{CP}}(1)$. The required GBWP values of the corresponding PreAmp designs

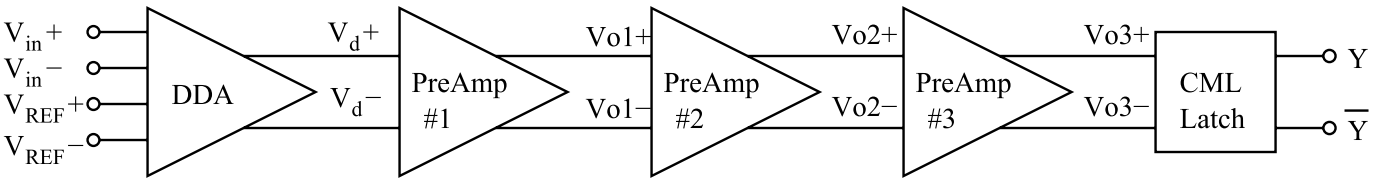

Fig. 5. Block diagram of the proposed comparator.

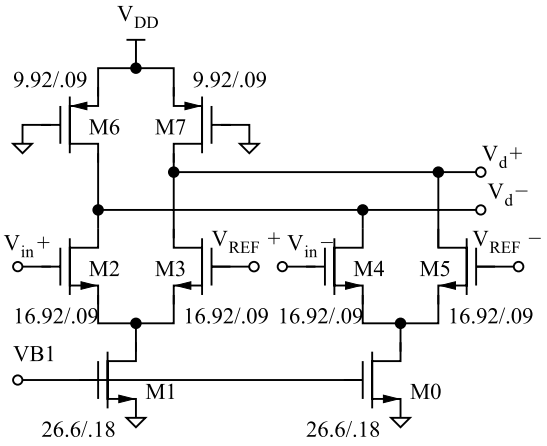

Fig. 6. Schematic of DDA.

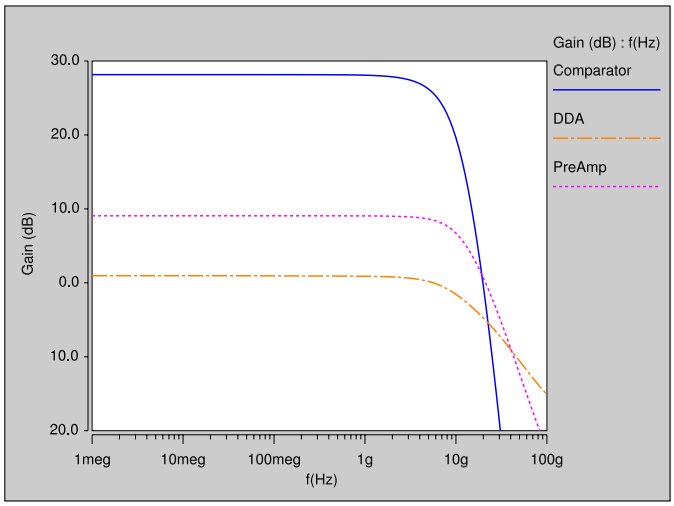

Fig. 7. AC simulation results of the DDA, PreAmp, and comparator.

are also shown on the figure. The figure depicts that cascading two active feedback PreAmps minimizes the total power of the comparator. However, it asks the PreAmp design for a GBWP as high as 41.5 GHz which is still difficult to realize. On the other hand, the implementation of cascading three PreAmps reduces the GBWP of each PreAmp to 27.7 GHz and the total power increases slightly. Further increasing the cascade stage number does not significantly loosen the GBWP requirement, while the total power increases rapidly. Consequently, we choose $N = 3$ for our implementation as a compromise between the power and the design difficulty.

Fig. 5 shows the block diagram of the final comparator design. The comparator is a cascade of a differential difference amplifier (DDA), aforementioned three second-order PreAmp

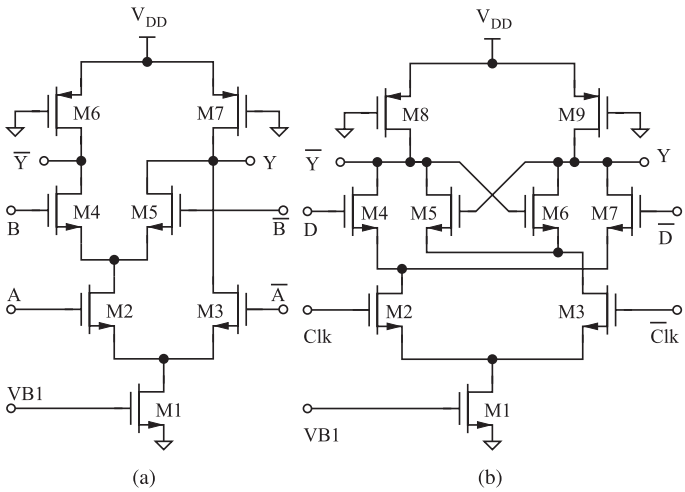

Fig. 8. CML gates [13]. (a) AND/NAND/OR/NOR. (b) Latch.

stages, and a current mode logic (CML) latch. The DDA is not counted as a PreAmp stage because its designated gain is close to unity and its bandwidth is much higher than the specification of the comparator.

Fig. 6 shows the schematic of DDA. It generates the amplified difference of the primary differential input and the corresponding differential reference voltage [12]. Note that the DDA design pairs the positive input and the positive reference instead of the negative input. Such an arrangement eliminates the design difficulty of keeping the differential pair functioning with a differential reference input as high as 800 mV.

Fig. 7 shows the typical simulation results of the comparator. The DDA has a gain of 0.9 dB and a -3 dB bandwidth of 11.5 GHz so that it does not influence the comparator's performance. Each PreAmp has a gain of 9.07 dB and a 11.3 GHz bandwidth, corresponding to a GBWP of 32.1 GHz which conforms to the requirement obtained from Fig. 4. The DDA and each PreAmp consume 1.63 and 2.19 mW, respectively. The simulated gain and unit-gain bandwidth of the cascaded DDA and the three PreAmps are 28.1 dB and 19.8 GHz, respectively.

2) Design of the Digital Blocks: Making the logic functions fast and quiet are another design challenges. Standard CMOS logic gates generate significant switching noise on the power rails. They also consume considerable power when operating at 14 GHz because of their rail-to-rail input/output (I/O) swings. To address these issues, all digital circuits are implemented with the CML family proposed in [13].

Fig. 8 shows some CML gates used in our design. The CML gates achieve faster logic switching because a small input voltage difference is sufficient to fully switch the currents of

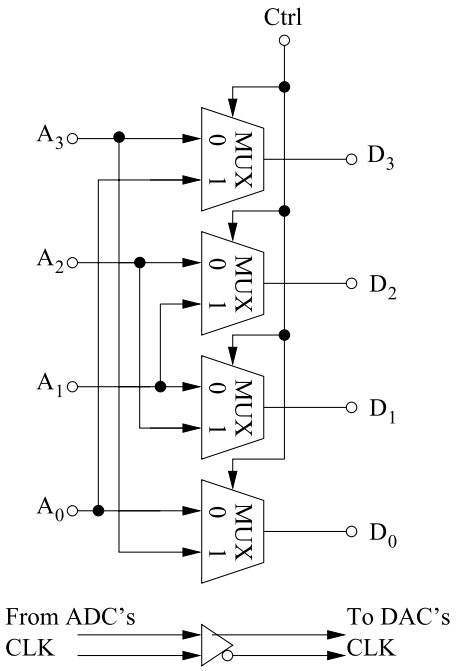

Fig. 9. Schematic of the DfT block.

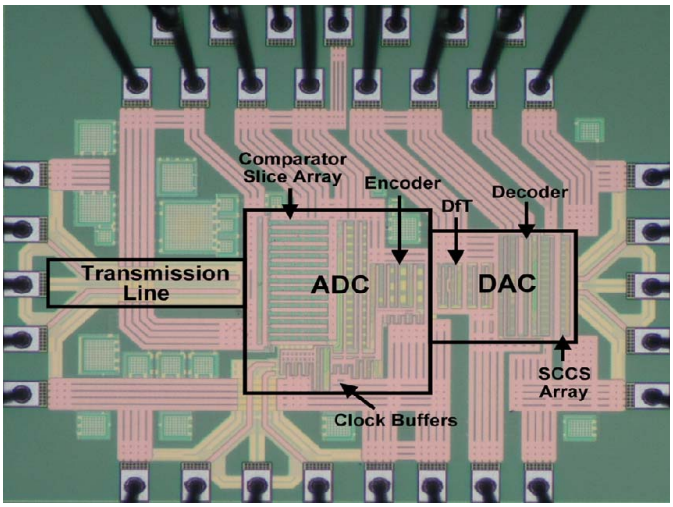

Fig. 10. Micrograph of the test chip.

the differential pair. Besides, the constant tail current sources of the CML gates alleviate severe power bouncing. The CML gates also consume less power than their CMOS counterparts when operate at 14 GHz because the I/O swings of the CML gates are not rail-to-rail. The I/O swings of the CML gates are designed to be the same as the full-scale I/O swings of the ADC and DAC.

Even with the CML circuits, the critical delay of the ADC's logic part is still too long for 14-GHz operation. Hence we apply the wave-pipelining technique [14] to address this issue. As shown in Fig. 1, intentional clock buffers are inserted to the clock paths to compensate for the delay time of the signal paths to gain some extra timing margins.

B. Digital-to-Analog Converter

The DAC comprises a Gray-to-thermometer decoder followed by the switched current source array. Each switched current source is implemented using the switched cascode current source (SCCS) configuration because of a higher output impedance and a better spurious free dynamic range (SFDR) [15]. CML latches are inserted between the decoder's outputs and every SCCS cell to ensure that all SCCS cells are simultaneously switched.

Similar to the ADC design, the DAC also suffers from a very short period for its logic parts. The same wave-pipelining technique by adding some intentional delays on the clock paths is also used to compensate for the critical delay of the DAC's logic part.

III. Design-for-Testability Circuitry

The proposed data converters operate at 14 GSps. Because of the lack of the logic analyzer (LA) and pattern generator that can operate at such a high speed, the ADC and DAC cannot be tested at the rated speed in conventional ways. There are three ways to test very high speed data converters. The first method is down-sampling the ADC's output with an on-chip demultiplexer and using a conventional LA to capture the digital data for analysis [16]. Usually, the outputs are directly downsampled without filtering because it is very costly and hard to implement an at-speed decimation filter on-chip. As a result, the measured noise floor increases because the high frequency noise folds back to the baseband of the downsampled spectrum.

The second method is implementing superfast on-chip memory to stored the ADC's output [17]. Similarly, the hardware cost is high and the design is difficult.

The third method is using digital loop-back [9], [18]. This method requires the simplest and the least on-chip circuits and thus well suits for our design.

Fig. 9 shows the proposed cost-effective DfT block for addressing the testing issues. The DfT block enables the test chip to conduct the at-speed tests in the cascaded mode, or to perform the eye diagram tests in the shuffled mode. A control pin Ctrl is used to switch between the two modes.

A. Cascaded Mode

Given Ctrl $= 0$, the digital outputs of ADC are connected to the corresponding inputs of the DAC in order. That is, the DfT design uses the digital loop-back technique to address the at-speed testing issues.

The differential nonlinearity (DNL) and integral nonlinearity (INL) values are measured by periodically applying a slow ramp input to the ADC in this mode. Then, the output waveform of the DAC is captured for plotting the transfer curve of the ADC's input and the DAC's output. The transition voltages of this staircase plot is used to derive the DNL and INL of the ADC, while the analog output levels of the DAC is used to compute the DNL and INL values of the DAC.

In addition to the static parameters INL and DNL, the dynamic performance of the data converters is also tested at full speed by inputting the ADC with a sinusoidal waveform using an analog signal generator. A spectrum analyzer

then analyzes the output of the DAC. The necessary test results including the SNDR, SNR, and harmonic distortion are measured according to the resulted spectra. Note that both the ADC and the DAC contribute the noise and harmonic distortion to the measurement results. Therefore, their intrinsic performances are expected to be better than the results acquired by the test.

A conservative way to estimate the ADC's performance is assuming the DAC to be ideal. Because an ideal DAC does not introduce any noise or distortion, the ADC is therefore considered as the root cause of the measurement results in the cascade mode.

Note that the inherent zero-order-hold behavior of the DAC's output shapes the measured spectra in the cascade mode even with the ideal DAC assumption. Theoretically, the measured spectrum is the result of filtering the ADC's output spectrum with

$$H_{\mathrm{SH}}(\omega) = e^{-j\omega T/2} T \frac{\sin(\omega T/2)}{(\omega T/2)} \tag{9}$$

where T represents the sampling period of the DAC [19]. $H_{\mathrm{SH}}(\omega)$ has low-pass responses and thus suppresses the noise of the test results. In other words, the raw test data of the cascaded mode is too optimistic. It is necessary to compensate for the low-pass responses of $H_{\mathrm{SH}}(\omega)$ to estimate the conservative performance of the ADC. It is done by filtering the measured spectrum in this mode with the inverse function of (9).

B. Shuffled Mode

The eye diagram is a common test item for serial links. Conventionally, the linear feedback shift register (LFSR) is used to generate pseudo-random patterns as the stimuli of the transmitter (TX) to observe the eye diagrams at the TX or at the receiver (RX) end. The output patterns of an n-bit LFSR repeats every $2^n - 1$ cycles. However, it is difficult to realize an LFSR capable of operating at such a high speed and providing a long pattern period. Even though it could be realized, the LFSR consumes a lot of power and area.

The proposed shuffled mode offers a cost-effective way to generate the random patterns for very high-speed eye diagram tests. By setting Ctrl to one, the DfT circuitry shuffles the connection order of the digital loop-back such that the LSB of the ADC A_0 connects to the MSB of the DAC D_3, A_1 to D_2, and so forth. Because the LSB of the ADC's output is the most random bit while the MSB is the least random bit, the shuffled codes become a randomized digital signal that is suitable for testing the eye-diagrams.

To explain how it works, let us examine the I/O relationships of a four-bit binary-coded ADC which can be expressed as

$$\begin{aligned}\frac{V_{\mathrm{in}}}{V_{\mathrm{REF}}} &= \frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} + q_4 \\ &= \frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + q_3 \\ &= \frac{b_1}{2} + \frac{b_2}{2^2} + q_2 \\ &= \frac{b_1}{2} + q_1 \end{aligned} \tag{10}$$

where b_1 to b_4 are the output bits of the ADC, and q_4 and q_1 represent the quantization noise sources of the ADC when we operate it as a four-bit ADC to a one-bit ADC, respectively. By (10), we have

$$\begin{aligned} b_4 &= 2^4(q_3 - q_4) \\ b_3 &= 2^3(q_2 - q_3) \\ b_2 &= 2^2(q_1 - q_2). \end{aligned} \tag{11}$$

Consequently, the shuffled ADC output D_{SFL} is written as

$$\begin{aligned} D_{\mathrm{SFL}} &= \frac{b_4}{2} + \frac{b_3}{2^2} + \frac{b_2}{2^3} + \frac{b_1}{2^4} \\ &= -8q_4 + 6q_3 + 1.5q_2 - 0.5q_1 + 2^{-4}b_1. \end{aligned} \tag{12}$$

Because q_4 to q_1 are all quantization noises, they approximate to random processes with uniform distribution. Equation (12) depicts the shuffled output inheres the randomness of the quantization noises and thus is suitable for testing eye diagrams.

Given q_4 to q_1 are uncorrelated to each other and uniformly distributed, the variance of the shuffled output $\sigma^2(D_{\mathrm{SFL}})$ normalized to the full scale of the ADC's output is calculated as

$$\begin{aligned} \sigma^2(D_{\mathrm{SFL}}) &\simeq \frac{1}{12}\left(\left(\frac{-8}{2^4}\right)^2 + \left(\frac{6}{2^3}\right)^2 + \left(\frac{1.5}{2^2}\right)^2 + \left(\frac{-0.5}{2^1}\right)^2\right) \\ &= \frac{1.0078}{12}. \end{aligned} \tag{13}$$

The result shows that the shuffled output of the binary-coded ADC has almost the same variance as that of the ideal random sequence with uniform distribution which is $1/12$. The same conclusion applies to a Gray-coded ADC like the proposed one.

The pattern period of the generated pseudo-random sequence is controlled by the input frequency of the ADC. Let the test setup follows the coherent test criteria $f_{\mathrm{in}} = \frac{I}{M} f_s$ where I and M are coprime and positive integers. Then, the shuffled output has a pattern period of M. Theoretically, M can be set to any integer by adjusting the stimulus frequency.

IV. Measurement Results

The ADC and DAC pair with the DfT circuitry are designed and fabricated in a 90-nm CMOS process. Fig. 10 shows the micrograph of the test chip. The test chip occupies 1.09×0.903 mm^2. The active area of the ADC and DAC are 0.10 and 0.04 mm^2, respectively. The test chip is directly mounted on an evaluation board for the following measurements.

A. Static Parameters

Fig. 11 shows the measured transfer function of the data converter pair in the cascaded mode at a sampling rate of 14 GSps. The INL and DNL plots of the ADC and DAC are shown in Figs. 12 and 13, respectively.

The INL and DNL errors of the ADC are within -0.22 to 0.18 LSB and -0.23 to 0.29 LSB, respectively. Meanwhile, the INL and DNL errors of the DAC are within ± 0.13 LSB and -0.21 to 0.16 LSB, respectively.

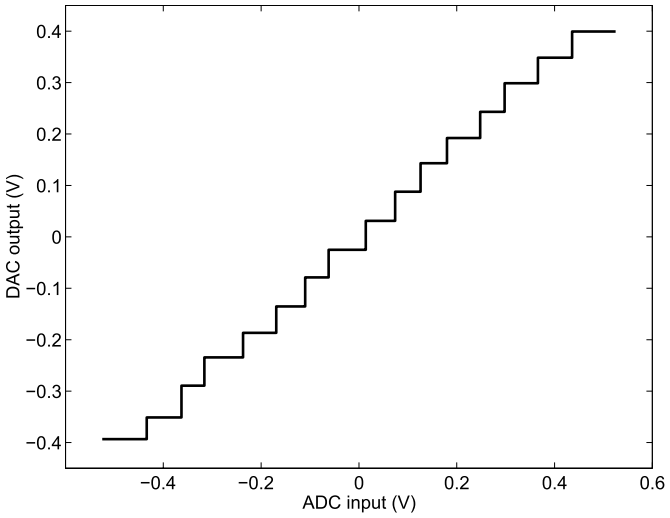

Fig. 11. Measured transfer curve of the data converter pair in the cascaded mode.

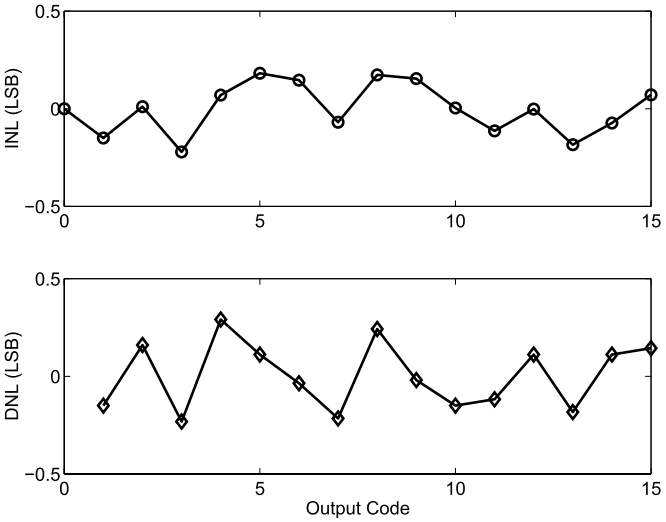

Fig. 12. Measured INL and DNL plots of the ADC.

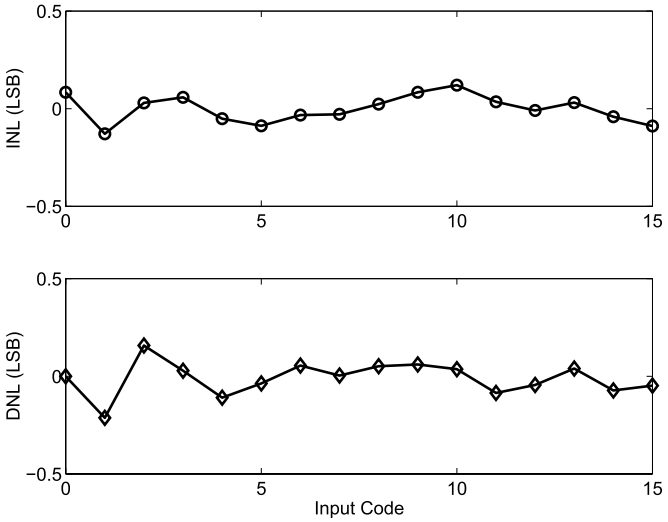

Fig. 13. Measured INL and DNL plots of the DAC.

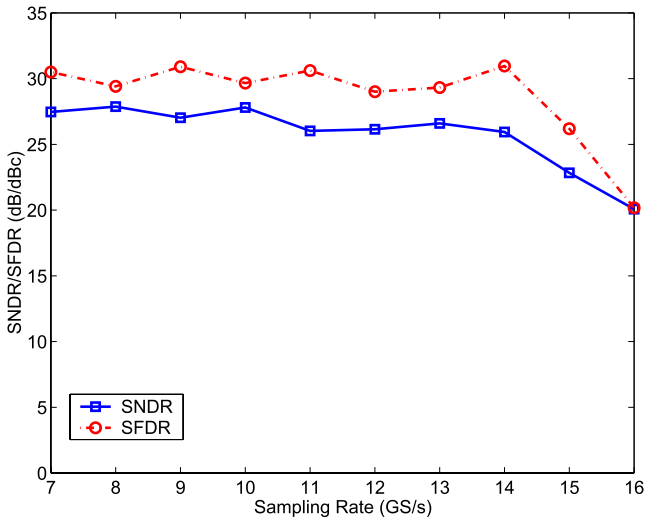

Fig. 14. Measured SNDR and SFDR versus sampling frequency in the cascaded mode without compensating for the S/H effects. The same 1.11 GHz, −1 dBFS sinusoidal stimulus is applied.

B. Dynamic Performance

Fig. 14 shows the dynamic performance of the data converter pair versus the sampling rate in the cascaded mode with the same 1.11 GHz stimulus. The SNDR has no significant degradation until the sampling rate is >14 GSps.

Fig. 15 depicts the measured SNDR and SFDR of the data converter pair versus the stimulus frequency operating in the cascaded mode at 14 GSps. The effective resolution bandwidth (ERBW) of the cascaded data converter pair is >3.1 GHz. The root cause of the SNDR droop is because of the increased noise floor.

Fig. 16 shows the measured output spectrum of the test chip in the cascaded mode at 14 GSps. The test stimulus is a −1 dBFS, 1.11 GHz sinusoidal signal. The raw data of the test shows the cascaded ADC and DAC achieves an SNDR of 25.9 dB and an SFDR of 31.0 dB. It corresponds to an effective number of bit (ENOB) of 4.00 bits. Note that the noise floor of the output spectrum indeed has a low-pass filtered trend because of the intrinsic zero-order hold outputs of the DAC.

As discussed in Section III, a conservative estimation of the ADC's performance is derived by compensating the raw data with $1/|H_{\text{sinc}}(j\omega)|^2$. The resulted spectrum is shown in Fig. 16 and it shows a flatter noise floor within the frequencies <5 GHz. However, the noise power spectral density within 5–7 GHz is higher than that of the averaged noise floor. It seems that the environmental noise instead of quantization noise of the data converters dominates in this frequency range. Consequently, the results after compensation overestimate the noise power of the ADC. Even though, the compensated results still indicate that the data converter pair achieves an SNDR of 25.1 dB and an SFDR of 29.1 dB. The corresponding ENOB is 3.88 bits.

Figs. 17 and 18 show the conservatively estimated performance of the ADC by compensating the output spectra of Figs. 14 and 15 with $1/|H_{\text{sinc}}(j\omega)|^2$, respectively. The estimated ERBW of the ADC is 3.1 GHz.

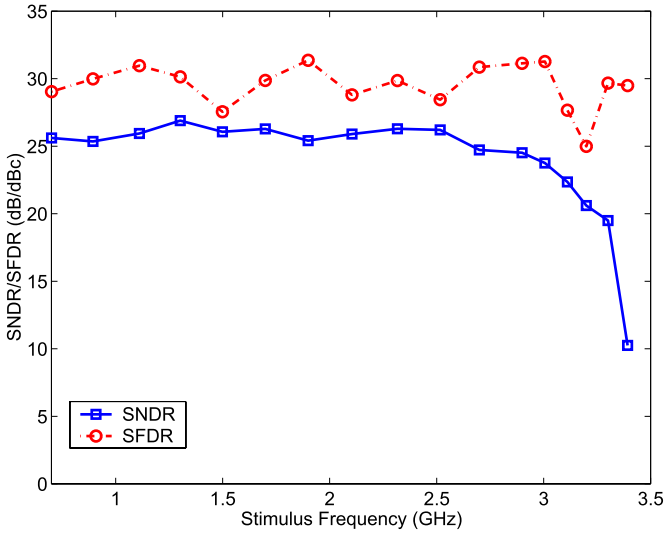

Fig. 15. Measured SNDR and SFDR versus input frequency in the cascaded mode without compensating for the S/H effects. The data converter pair operates at 14 GSps and the stimulus amplitude is fixed at −1 dBFS.

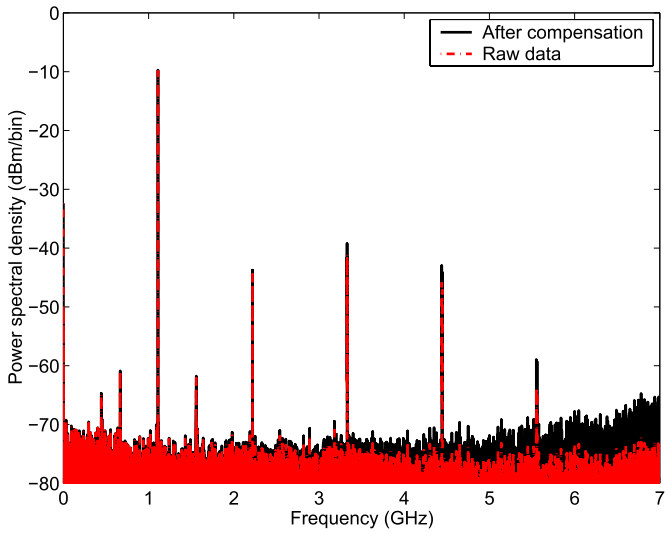

Fig. 16. Measured output spectrum in the cascaded mode at 14 GSps. The input of the ADC is 1.11 GHz, −1 dBFS sinusoidal stimulus.

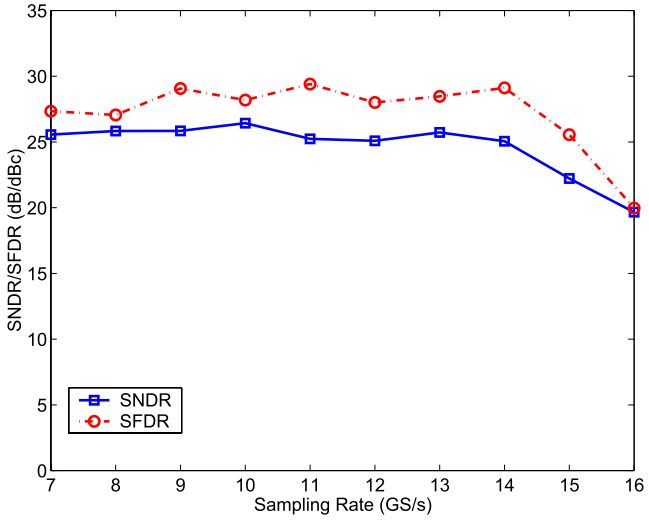

Fig. 17. Estimated SNDR and SFDR of the ADC versus sampling frequency from the measured results in the cascaded mode after compensating for the S/H effects. The same 1.11 GHz, −1 dBFS sinusoidal stimulus is applied.

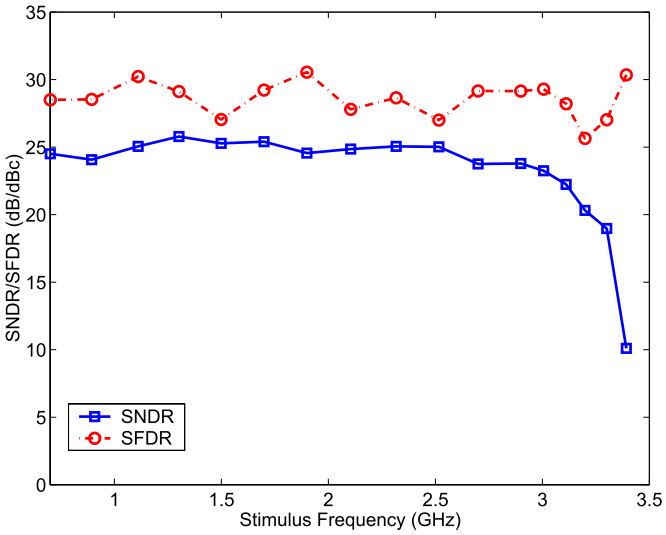

Fig. 18. Estimated SNDR and SFDR of the ADC versus input frequency in the cascaded mode at 14 GSps after compensating for the S/H effects.

C. Power Consumption

The test chip including the clock buffers and the DfT circuitry totally consumes 323 mW from a 1.0 V supply when operates at 14 GSps. Table I summarizes the ADC performance and compares with the state-of-the-art designs. We define a figure of merit (FOM) as

$$\text{FOM} = \frac{\text{Power}}{\text{ERBW} \cdot \text{ENOB}} \tag{14}$$

for the ADC where the term (ERBW · ENOB) approximates to the channel capacity defined by (1). This FOM indicates the energy that an ADC needs to effectively resolve a data bit when the ADC is applied to the receiver of a serial link. The proposed design achieves a good FOM.

D. Eye Diagram

Fig. 19 shows the measured eye diagram of the data converter pair clocked at 1 GSps in the shuffled mode. It is noteworthy that the stimulus frequency and amplitude of the eye diagram test are carefully chosen so that all the possible code transitions occur as evenly as possible. This is done by conducting behavioral simulations. In this test, the stimulus is an 88.77 MHz sinusoidal input.

All the 15 eyes in Fig. 19 are clearly open though the widths of the eyes are somewhat smaller. The widths of the open eyes indicate not only the best position for placing the sampling edges of the RX, but also the timing jitter that can be tolerated. On the other hand, the heights of the open eyes tell the largest tolerable amplitude noise. Fig. 19 also depicts the reasons of the smaller eyes. First, the rise time and fall time of the output are both around 70 ps. Second, the transient responses ring

TABLE I
ADC PERFORMANCE SUMMARY AND COMPARISON

Source	[20]	[16]	[21]	[17]	[22]	[18]	This work
Technology	180nm CMOS	130nm CMOS	130nm CMOS	90nm CMOS	65nm CMOS	0.18μm BiCMOS	90nm CMOS
Power supply	1.8V/2.5V	1.2V	1.3V	1V/2.5V	1.2V	3.3V	1.0V
Sampling rate (f_s)	4 GSps	2.0/3.5 GSps	12 GSps	24 GSps	5 GSps	35 GSps	14 GSps
Design	Flash ADC	Flash ADC	4× Interleaved Flash ADC	16× Interleaved SAR ADC	Flash ADC	Flash ADC	Flash ADC
f_s per ADC	4 GSps	2.0/3.5 GSps	3 GSps	1.5 GSps	5 GSps	35 GSps	14 GSps
Resolution	4 bits	5 bits	4 bits	6 bits	4 bits	4 bits	4 bits
INL (LSB)	$0.20 \sim -0.24$	< 0.39	$0.13 \sim -0.30$	< 0.5	$0.44 \sim -0.39$	$0.44 \sim -0.38$	$0.18 \sim -0.22$
DNL (LSB)	$0.15 \sim -0.14$	< 0.24	$0.36 \sim -0.24$	< 0.5	$0.41 \sim -0.44$	$0.35 \sim -0.44$	$0.29 \sim -0.23$
SNDR (dB) @f_{in}	22.71 100MHz	29.1 $\simeq$ 210MHz	24.2/19.2 $23.4M/2.9$GHz	33.3 $\simeq$ 1GHz	25.4 4MHz	$24.1^{\dagger}$ $\leq$1GHz	$25.9^{\dagger}/25.1^{\ddagger}$ 1.11 GHz
SFDR (dBc) @f_{in}	30.0 700 MHz	38.0 $\simeq$ 210 MHz	34.7/27.0 $23.4M/2.9$GHz	40 8 GHz	N/A	$27.3^{\dagger}$ $\leq$ 1GHz	$31.0^{\dagger}/29.1^{\ddagger}$ 1.11 GHz
ENOB (bits)	3.48	4.44/4.54	3.73/2.90	5.25	3.93	$3.71^{\dagger}$	$4.00^{\dagger}/3.88^{\ddagger}$
ERBW (GHz)	≤ 1.3	0.9/0.6	2.9	5.6	~ 2.5	$8^{\dagger}$	$3.1^{\dagger\ddagger}$
Power (mW)	608	120	260	1200	34.3	4500	214
FOM[1] (pJ/conv.-step)	21.0	3.07/4.30	2.92	2.82	0.45	$21.5^{\dagger}$	$2.16^{\dagger}/2.34^{\ddagger}$
FOM[2] (pJ/bit)	134	30.0/44.1	24.04	40.8	3.49	$152^{\dagger}$	$17.25^{\dagger}/17.8^{\ddagger}$

†: Measurement results by cascading the ADC and the DAC.
‡: After compensating for $H_{SH}(z)$.
[1]: $= \frac{Power}{2 \cdot ERBW \cdot 2^{ENOB@DC}}$.
[2]: by (14).

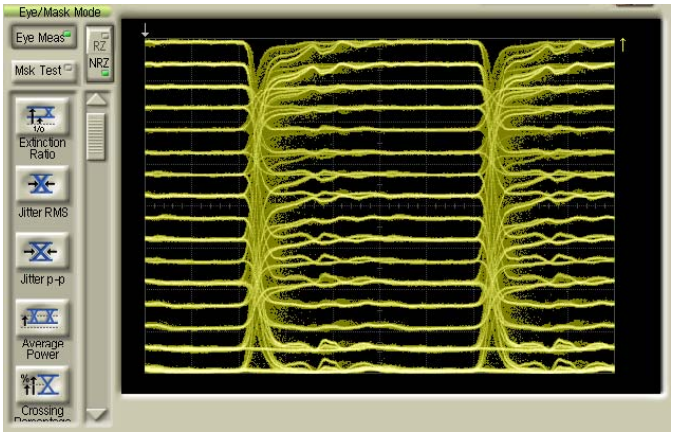

Fig. 19. Measured eye diagram in the shuffled mode at 1 GSps.

for a long time due to the imperfectly matched impedances in the testing environment. The ringings make the eyes' widths smaller.

V. CONCLUSION

A 14 GSps four-bit ADC and DAC pair in 90-nm CMOS for the design of advanced serial-link transceivers was presented. The active feedback amplifiers, CML, and wave-pipelining technique were applied to alleviate the severe power bouncing and to achieve the ultimate 14 GSps sampling rate. The DfT circuits used the digital loop-back scheme to enable the at-speed measurements in the cascade mode. We pointed out that compensating the measured output spectra for the S/H effects in the cascade mode improved the measurement accuracy. By shuffling the connection order of the digital loop-back in the other shuffled mode, the eye diagrams were also tested. The experimental results showed that the cascaded ADC and DAC pair achieved a 25.9 dB SNDR and a 31.0 dBc SFDR with the 1.11 GHz stimulus, and consumed 323 mW from a 1.0 V supply.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC), Hsinchu, Taiwan, for fabricating the test chips.

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Hao-Chiao Hong (S'98–M'04–SM'12) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Tsing-Hua University, Hsinchu, Taiwan, in 1990, 1992, and 2003, respectively.

He was with Taiwan Semiconductor Manufacturing Company, Hsinchu, from 1997 to 2001, where he has developed mixed-signal IPs for customers and process vehicles. He joined Intellectual Property Library Company, Hsinchu, as the Senior Manager of the Analog IP Department in 2001. He has been with National Chiao-Tung University, Hsinchu, since 2004, where he is currently a Full Professor of the Electrical and Computer Engineering Department. He holds three U.S. patents, two R.O.C. patents, and one P.O.C. patent. His current research interests include the design-for-testability, built-in self test, and calibration techniques for mixed-signal circuits and high performance mixed-signal IC design.

Dr. Hong received the Best Paper Award from the 2009 International Symposium on VLSI Design, Automation & Test and the Best Advisor Award in the IC design competition of the 12th Macronix Golden Silicon Award in 2012. He has served as the Executive Secretary of the mixed-signal and RF consortium of the Ministry of Education, Taiwan, from 2006 to 2008, and the Executive Secretary of the Heterogeneous Integration Consortium of the Ministry of Education, Taiwan, from 2008 to 2009. He was the General Chair of the sixth VLSI Test Technology Workshop (VTTW) and the Program Chair of the fifth VTTW. He is a Life Member of the Taiwan IC Design Association and the VLSI Test Technology Forum, Taiwan.

Yung-Shun Chen was born in Taoyuan, Taiwan, in 1984. He received the B.S. degree in electronic engineering from the National Taipei University of Technology, Taipei, Taiwan, in 2006, and the M.S. degree from the Institute of Electrical Control Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2008.

He is currently with the MS/RF Solution Division, Taiwan Semiconductor Manufacturing Company, Hsinchu. His current research interests include CMOS high-speed circuit design for data communication.

Wei-Chieh Fang was born in Tainan, Taiwan, in 1985. He received the B.S. and M.S. degrees from the Department of Electrical and Computer Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2007 and 2009, respectively.

He joined the Advanced Mixed-Signal IC Design and Design-for-Testability Laboratory in 2007, where he was engaged in the development of high-speed A/D converters. From 2009 to 2010, he served in the R.O.C. Army as a Logistic Officer. He has been with the Analog IP Department, ALi Corporation, Taipei, Taiwan, since 2010, where he is currently developing AD/DA IPs for set-top box products.