Fast Thermal Aware Placement With Accurate Thermal Analysis Based on Green Function

Sean Shih-Ying Liu, Ren-Guo Luo, Suradeth Aroonsantidecha, Ching-Yu Chin, and Hung-Ming Chen

***Abstract*— In this paper, we present a fast and accurate thermal aware analytical placer. A thermal model is constructed based on a Green function with discrete cosine transform (DCT) to generate full chip temperature profile. Our thermal model is tightly integrated with an analytical placer implemented based on the SimPL framework. A temperature spreading force based on the Gaussian model is proposed to reduce the maximum on-chip temperature and optimize tradeoff between total half-perimeter wirelength and on-chip maximum temperature. The temperature profile generated using our thermal model is verified by the ANSYS ICEPAK and obtains an average deviation within 3.0% with 240× speedup.**

***Index Terms*— Design for manufacture, design for quality, design methodology, electronic design automation, logic design, placement, temperature control, thermal analysis.**

I. Introduction

THE problem of degradation on chip performance due to temperature issues becomes more critical in the advanced node technology. The benefit of a smaller transistor comes with the cost of higher power density per unit area. Higher power density translates to more dissipation of heat and this exorbitant amount of heat rapidly increases on-chip temperature. Recent studies have shown that chip performance and reliability can deteriorate significantly due to temperature variation. Evidence has shown that a 10 °C variation in temperature can induce 5% increase in interconnect delay, 25% increase in crosstalk-induced noise and reduce component lifetime by 50% [3], [4]. Thus, reducing the maximum on-chip temperature to eliminate the hot spots is critical to chip's reliability and performance.

The situation for on-chip temperature and variation will only deteriorate as the technology advances. As node size scales down, components are placed more compactly, which means higher power density per unit area. Shrinking in interconnect dimension also has an adverse effect of increase in higher power and heat dissipation due increase in interconnect resistance. Viewed in this light, the effect of chip temperature and variation must be addressed when considering chip performance and reliability.

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A. Previous Works

To tackle the temperature issue at transistor level, many of the previous works proposed several methods to reduce the temperature through replacement of cells or propose more efficient method to obtain the temperature profile of a chip.

Regarding previous works on the thermal model, the most recent approaches can be categorized as numerical and analytical approaches. Numerical approach generally uses finite-difference method (FDM) [5] or finite-element method (FEM) [6] by meshing the given silicon substrate and then solves a set of linear equation to obtain the temperature profile. FDM discretize the partial differential equation of heat conduction and uses forward-difference method to approximate the temperature profile. FEM discretize the given temperature for each grid point in design space and then points elsewhere are calculated using interpolation. Generally, numerical approach can achieve high accuracy at the expense of relatively long run time, making it suitable for postlayout thermal verification.

Analytical approach solves the differential equation of heat problem by first generating the fundamental solution of one unit heat source and then exploiting the linearity of the heat equation to obtain the general solution of overall temperature distribution [7]–[9]. In contrast to the numerical approach, analytical approach can quickly obtain an approximate solution in a closed form representation without volume meshing, making it suitable for where approximate solution is adequate.

Regarding previous works on thermal aware placement, a thermal aware placer generally consists of two main components: a thermal model to conduct the full chip thermal analysis and a placer to place the design. Previous works on thermal aware placement based on their thermal model and placement algorithm are listed in Table I. Tsai *et al.* [6] constructed the lumped RC matrix to model the substrate heat conduction and obtain a thermal profile using FDM, then simulated annealing is applied to evenly spread out hot spots. Kahng *et al.* [10] adopts its thermal model from [6] and integrates the model to APlace [11]. Chen *et al.* [12] simplifies the model in [6] and applies partition-based placement to consider thermal effect. Goplen *et al.* [5] uses the FEM method to conduct full chip temperature analysis and uses linear force directed placer based on star net model to mediate thermal effect. Jing *et al.* [13] constructed RC equivalent matrix to model heat transfer and obtain a thermal profile using FDM, Fiduccia-Mattheyses partition is then applied as their placement strategy. Berned *et al.* [14] proposed a methodology to reduce the weighted net length with height power dissipation. To obtain a smooth tempera-

TABLE I
PREVIOUS WORK ON THERMAL AWARE PLACEMENT

	Thermal Model	
Placement Strategy	**FEM**	**FDM**
Simulated Annealing		Tsai et al. [6]
Partition-Based	Goplen et al. [5]	Chen et al. [12], Jing et al. [13]
Quadratic Model		Obermeier et al. [14]
Non-Linear Model		Kahng et al. [10]

ture profile, Kraftwerk2 [15] is used as base kernel engine and then modify the gradient model to reduce the maximum temperature.

B. Our Contributions

In spite of past efforts, thermal aware placement today still suffers from deficiency in terms of: 1) accuracy of full-chip analysis; 2) quality of placement; and 3) execution time. The accuracy of some thermal models is unknown as it lacks in evaluation to a reliable source. The placement quality for some algorithms is unable to deal with complex designs either because it greedily focuses on the temperature reduction or its placement strategy targets smaller designs. Some methods are impractical to handle million-gate design due to execution speed due to time complexity of its algorithm (e.g., simulated annealing). In addition, none of our surveyed thermal-aware placers have experimented on modern million-gate designs.

In this paper, we present a thermal aware placer to reduce the maximum on-chip temperature using an analytical thermal model combined with an analytical placer using quadratic wirelength model. Both of the thermal model and placer are analytical, making the execution time inherently fast.

The thermal model in this paper is a Green function-based analytical method. In comparison with previous work [7], which neglects boundary condition in z-direction, we consider the additional boundary condition by formulating it as a Class I eigenvalue problem and solved it using a method described in [16]. The run time bottleneck of the thermal model is during the dicrete cosine transform (DCT) calculation. We reduce the time complexity to $O(n\log n)$ by reordering inputs using discrete Fourier transform (DFT).

The placer implemented in this paper was based on the framework proposed in SimPL [2]. The reason to use SimPL is because the framework divides the mechanism of wirelength minimization and cell spreading to two independent placers. Such framework making it relatively easy to incorporate an additional temperature spreading mechanism without changing the original placer engine too much.

Both the thermal model and placer implemented in this paper are verified with reliable sources. The thermal model is verified with commercial tool ANSYS ICEPAK and has a deviation within 3.0% with 242× speedup. The placer implemented in this paper is evaluated with Gigascale System Research Center (GSRC) [17] and achieves comparable performance compared with APlace2 [11] and Capo10.5 [18].

In contrast to numerical approach, which is ideal for high accurate temperature profile, analytical thermal model offers closed form expression, which is ideal to integrate with early floorplanning or placement stage [19]. The thermal model in this paper is integrated with a flat global placer based on quadratic wirelength model. We propose the concept of a thermal anchor combined with dynamic hot region resizing to optimize between maximum temperature and total half-perimeter wirelength (HPWL). Experiments have performed on weight adjustment by using quadratic model and force adjustment using Gaussian model to demonstrate the effectiveness of our thermal aware placer.

The following sections are organized as follows. Section II gives the preliminary background and formulates the problem. Section III derives the analytical thermal model. Section IV integrates the thermal analysis model to a global placer and describes how integration is achieved. Section V presents the experimental result and Section VI concludes this paper.

II. PRELIMINARIES AND PROBLEM FORMULATION

The analytical thermal analysis conducted in this research generates a steady-state temperature profile. In other words, given with a consistent power density distribution, the obtained temperature profile is when time approaches infinity. It is relatively difficult to deal with the dynamic power dissipation due to several reasons. First, it requires an input activity factor for each net. Second, it needs to consider an interconnect wirelength and clock tree network for capacitance load.

In addition, optimization for static power consumption and dynamic power consumption can be handled separately. The work done in [20] and [21] is proposed to optimize a dynamic power consumption for a given clock network. Thus, to divide and conquer the problem, we focus our attention on static power dissipation. We assume a given power density for each cell and use the information to obtain a temperature profile.

Although temperature begins to become a critical issue in chip design, it should be regarded as a secondary objective at placement stage. Temperature reduction should not come before routability of the placement. At placement stage, HPWL is a widely accepted perimeter to evaluate quality of placement [15], [22], [23]. Thus, we define the thermal aware placement problem as follows.

Thermal Aware Placement Problem: Given a net list $N = \{n_1, n_2, n_3, \ldots, n_i\}$, cell list $C = \{c_1, c_2, c_3, \ldots, c_j\}$ where each cell c_j is given with a power density p_j. Assume the wirelength driven placement has a maximum temperature $T_{\max}$ and the thermal aware placement has a maximum temperature $T'_{\max}$. Place the design with minimal half HPWL and maximize $T_{\max} - T'_{\max}$.

III. ANALYTICAL THERMAL MODEL

During floorplanning or placement stage, the primary focus of thermal analysis is on its execution time rather than its accuracy. At this stage, information on interconnect capacitance load is missing as routing is not performed and thus temperature analysis cannot accurately capture dynamic power consumption of the design. Therefore, rather than focusing our attention on achieving high accuracy, we adopt our thermal model using Green function to quickly obtain a temperature profile to guide placer. The concept of the Green function is

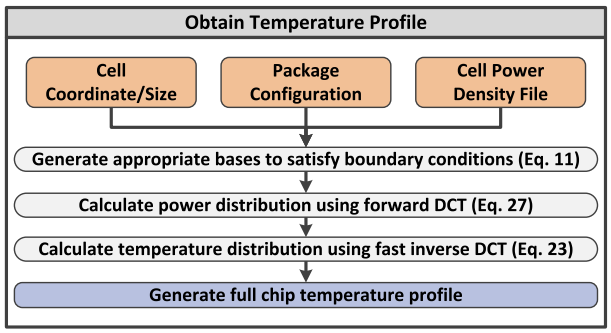

Fig. 1. Flow diagram to solve the heat conduction problem.

TABLE II
VARIABLES USED IN A THERMAL MODEL

Variable	Definition
T	Temperature in Celsius $(^{\circ}C)$
r	Dimension in x,y and z direction
κ	Thermal conductivity $(W/m^{\circ}C)$
c_p	Specific heat
ρ	Heat capacity
$\sigma = c_p\rho$	Variable with unit of $(J/m^{3\circ}C)$.
$p(r,t)$	Power density with unit of (W/m^3)
$D = (0, L_x) * (0, L_y) * (-L_z, 0)$	Dimension of die

to first derive the fundamental solution then obtain the general solution for chip's temperature profile.

The general structure of this section is organized as follows. First, the problem is formulated based on general heat conduction problem. The problem is first solved by assuming the power density equal to zero to obtain a set of eigenvectors. The concept of the Green function is applied using obtained eigenvectors to consider the presence of power density. Finally, the solution to the heat conduction problem is in form of DCT and input reordering is applied to realize DCT using DFT. A flow diagram of our procedure to solve the heat conduction problem is shown in Fig. 1.

A. Heat Conduction in Chip Level

Given the law of conservation of energy, it states that the total amount of energy in a system remains constant over time. In other words, change in heat energy is equivalent to the summation of heat flowing into the unit volume with its pre-existing power density. Hence, the temperature distribution inside a specific region can be expressed as

$$\sigma \frac{\partial T(r,t)}{\partial t} = \nabla \cdot (\kappa \nabla T(r,t)) + p(r,t) \quad r \in D. \tag{1}$$

B. Boundary Condition

To quickly obtain a thermal profile with reasonable accuracy, a good and reasonable thermal model is necessary to be used. Table II lists the variables used in formulating a thermal model in this section. A flip-chip model in which top and bottom surfaces of die are attached to printed circuit board (PCB) and heat sink is shown in Fig. 2. The model assumes all four sides of the chip are insulated from the ambient environment. The net heat flow on the boundary of the four

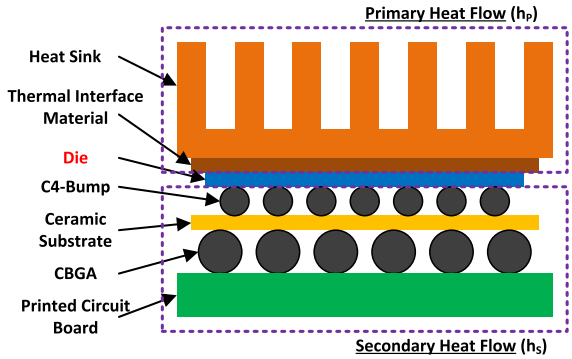

Fig. 2. Schematic representation of cross-sectional view of a VLSI chip with packaging.

side walls (x- and y-direction) is assumed to be zero, which can be expressed in form of homogeneous boundary condition

$$\frac{\partial T(r,t)}{\partial x} |_{x=0,L_x} = \frac{\partial T(r,t)}{\partial y} |_{y=0,L_y} = 0. \tag{2}$$

Heat generated from the chip can be dissipated to two directions, one toward the heat sinks at the top and one toward PCB at the bottom. In Fig. 2, h_p denotes primary heat flow to the heat sink and h_s denotes secondary heat flow to the PCB. Boundary condition of heat flow in z-direction can be expressed in form of inhomogeneous boundary condition

$$\kappa \frac{\partial T(r,t)}{\partial z} |_{z=-L_z} = h_p T(x, y, -L_z, t) \tag{3}$$

$$\kappa \frac{\partial T(r,t)}{\partial z} |_{z=0} = -h_s T(x, y, 0, t). \tag{4}$$

C. Solving Heat Conduction Problem as Homogeneous Equation

Before solving (5), temperature distribution described in (6) is first solved by setting power density in (1) to zero. In (6), $\Theta(x, y, z, \infty)$ denotes temperature distribution without the presence of power density.

$$\nabla^2 T(r) = \frac{-p(r)}{\kappa} \tag{5}$$

Equation (5) is an inhomogeneous equation. The general solution to the inhomogeneous equation in (5) needs to satisfy all of the boundary conditions in (2)–(4). Thus, the given heat conduction problem is first modeled as a homogeneous equation. Solution obtained by solving the homogeneous equation is substituted back to (5) to solve the inhomogeneous equation.

The heat conduction problem is modeled as a form of homogeneous equation by setting the internal power density $p(r,t)$ to zero. Equation (1) can then be rewritten as follows:

$$\sigma \frac{\partial T(r,t)}{\partial t} = \nabla \cdot (\kappa \nabla T(r,t)). \tag{6}$$

Let $\Theta(r, \infty)$ be the homogeneous solution of steady-state temperature distribution. By substituting $\Theta(r, \infty)$ into (6) when time variable t approach to infinity, the fundamental solution can be obtain as follows:

$$\Theta(r, \infty) = \cos(\omega_x x) \cos(\omega_y y) v(z). \tag{7}$$

The variable of ω is an eigenvalue of r coordinate after solving the homogeneous equation in (6), and the fundamental solution $v(z)$ in z dimension that satisfies the inhomogeneous boundary conditions (3) and (4) can be obtained by applying a combination of trigonometric function.

Using a method described in [16], the general form of eigenvector, eigencondition and normalize factor N_{ijk} can be obtained. Equations (8) and (9) correspond to two sets of eigenvector in z direction that satisfies the boundary condition described in (3) and (4). Equation (10) is the eigencondition that satisfies the boundary condition in z-direction for both (3) and (4)

$$v(z) = \kappa \cos(\omega_z (z + L_z)) + \frac{h_p}{\omega_z} \sin(\omega_z (z + L_z)) \quad (8)$$

or

$$v(z) = \kappa \cos(\omega_z z) + \frac{h_s}{\omega_z} \sin(\omega_z z) \quad (9)$$

where ω_z satisfies

$$\frac{\kappa^2 \omega_z^2 - h_p h_s}{\kappa \omega_z (h_p + h_s)} = \cot(\omega_z L_z). \quad (10)$$

If eigencondition in (10) is satisfied, both set of eigenvectors in (8) and (9) can achieve the same final result. In our implementation, only (8) is used as our eigenvector in z-direction.

As cosine is periodic, ωL must be an integer multiple of π. The general solution of homogeneous heat equation at infinite time is expressed as the summation of numerous base solution described as

$$\begin{aligned}\Theta(x, y, z, \infty) &= \sum_{i=0}^{\infty}\sum_{j=0}^{\infty}\sum_{k=0}^{\infty} \frac{v(r)}{\sqrt{N_{ijk}}} \\ &= \sum_{i=0}^{\infty}\sum_{j=0}^{\infty}\sum_{k=0}^{\infty} \frac{\cos\left(\frac{i\pi}{L_x}x\right)\cos\left(\frac{j\pi}{L_y}y\right)v(z)}{\sqrt{N_{ijk}}}.\end{aligned} \quad (11)$$

N_{ijk} is the normalized value equal to $N_{xi}N_{yj}N_{zk}$, N_{xi}, N_{yj}, and N_{zk} are expressed as follows:

$$\begin{aligned} N_{xi} &= \begin{cases} \frac{L_x}{2}, & i \neq 0 \\ L_x, & i = 0 \end{cases} \\ N_{yj} &= \begin{cases} \frac{L_y}{2}, & j \neq 0 \\ L_y, & j = 0 \end{cases} \\ N_{zk} &= \frac{1}{2\omega_z^2}\left\{\left[hp^2 + (\kappa\omega_z)^2\right]\left[\frac{h_s\kappa}{h_s^2 + (\kappa\omega_z)^2} + L_z\right] + h_p\kappa\right\}. \end{aligned} \quad (12)$$

D. Solving Heat Conduction Problem as Inhomogeneous Equation

To solve the temperature distribution problem with the presence of power density, Green function denoted by $G(r, r')$ is applied. In this context, $G(r, r')$ represents the temperature distribution in response to a unit point power source denoted by $\delta(r - r')$. The set of eigenvectors in (11) satisfies the definition of Dirac Delta function and can be used to obtain general solution $T(r, \infty)$ described as

$$T(r, \infty) = \int_D G(r, r')P(r')dr' \quad (13)$$

$$\nabla^2 G(r, r') = -\frac{\delta(r, r')}{\kappa} = -\frac{\Theta(r, r')}{\kappa} \quad (14)$$

subject to boundary conditions

$$\frac{\partial G(r, r')}{\partial x}|_{x=0,a} = \frac{\partial G(r, r')}{\partial y}|_{y=0,b} \quad (15)$$

$$\kappa\frac{\partial G(r, r')}{\partial z}|_{z=-L_z} = h_p G(x, y, -L_z) \quad (16)$$

$$\kappa\frac{\partial G(r, r')}{\partial z}|_{z=0} = -h_s G(x, y, 0) \quad (17)$$

where

$$\delta(r, r') = \begin{cases} 1, & r = r' \\ 0, & r \neq r'. \end{cases} \quad (18)$$

Equation (19) is the temperature distribution in response to a unit power source that can be obtained by applying (14) to the heat equation. Equation (20) corresponds to the temperature distribution for multiple power sources, which is the summation of all temperature distributions in response to each individual unit power source.

$$G(r, r') = \frac{1}{\kappa\omega^2}\Theta(r, r'). \quad (19)$$

$$\begin{aligned} G(r, r') = &\sum_{i=0}^{N_x-1}\sum_{j=0}^{N_y-1}\sum_{k=0}^{N_z-1} \\ &\times\frac{1}{\kappa\omega^2 N_{ijk}} v_{ij}(x, y, x', y')v_k(z, z'). \end{aligned} \quad (20)$$

In our implementation, temperature distribution is approximated by dividing the given chip into M by N bins. More bins imply more detailed temperature distributions that the temperature profile can offer. Equation (21) describes the average temperature T_{mn} in bin (m, n).

$$\begin{aligned} T(r, \infty) &\approx T(m, n) \\ &= \frac{1}{\triangle x \triangle y}\int_{m\triangle x}^{(m+1)\triangle x}\int_{n\triangle y}^{(n+1)\triangle y} T(r, \infty)dxdy \end{aligned} \quad (21)$$

$$\triangle x = \frac{L_x}{M}, \quad \triangle y = \frac{L_y}{N} \quad (22)$$

Solution in z-direction described in (21) is independent to solution in x- and y-directions. The temperature distribution

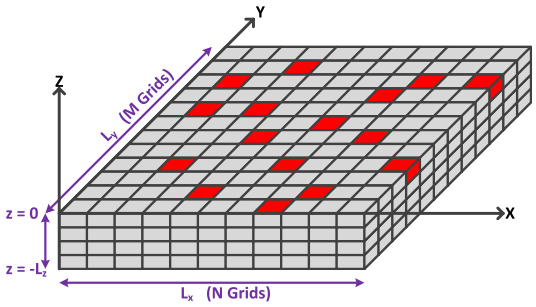

Fig. 3. Illustration of power density on a chip that is partitioned to M by N grids.

in (21) can then be derived as

$$\begin{aligned}
&T(m,n)\\
&= \frac{1}{\triangle x \triangle y}\int_{m\triangle x}^{(m+1)\triangle x}\int_{n\triangle y}^{(n+1)\triangle y}\sum_{i=0}^{N_x-1}\sum_{j=0}^{N_y-1}\sum_{k=0}^{N_z-1}\frac{\upsilon_{ij}(x,y)\upsilon_k(0)}{\kappa\omega^2 N_{ijk}}\\
&\quad *\int_0^{L_x}\int_0^{L_y}\int_{-L_z}^{0}P(x',y')\upsilon_{ij}(x',y')\upsilon_k(z')dx'dy'dz'dxdy\\
&= \frac{1}{\triangle x \triangle y}\int_{m\triangle x}^{(m+1)\triangle x}\int_{n\triangle y}^{(n+1)\triangle y}\sum_{i=0}^{N_x-1}\sum_{j=0}^{N_y-1}\sum_{k=0}^{N_z-1}\frac{\upsilon_{ij}(x,y)\upsilon_k(0)}{\kappa\omega^2 N_{ijk}}\\
&\quad *P_{ij}T_k dxdy\\
&= \sum_{i=0}^{N_x-1}\sum_{j=0}^{N_y-1}\sum_{k=0}^{N_z-1}C_{ij}D_{ij}\hat{P}_{ij}\frac{T_k\upsilon_k(0)}{\kappa\omega^2 N_{ijk}}\cos\left(\frac{i\pi(2m+1)}{2M}\right)\\
&\quad *\cos(\frac{j\pi(2n+1)}{2N})\\
&= \sum_{i=0}^{N_x-1}\sum_{j=0}^{N_y-1}E_{ij}\hat{P}_{ij}Z_{ij}\cos\left(\frac{i\pi(2m+1)}{2M}\right)\cos\left(\frac{j\pi(2n+1)}{2N}\right)\\
&= \mathrm{IDCT}\left[E_{ij}\hat{P}_{ij}Z_{ij}\right]. \qquad (23)
\end{aligned}$$

In Fig. 3, the overall chip power distribution is approximated by dividing the chip into $M \times N$ grids with power density p_{mn} in each grid. The power density in each bin is the summation of power density of cells within that bin. For cells that are placed on the boundary between the two bins, power density of the cell is divided based on proportion of cell area covered in each bin. When solving temperature distribution in (23), power density $P(r,r')$ is transformed to frequency domain, which becomes P_{ij}.

$$P_{ij} = \int_0^{L_x}\int_0^{L_y}P(x',y')\upsilon_{ij}(x',y')dx'dy'. \qquad (24)$$

$$\begin{aligned}
P_{ij} &= \sum_{m=0}^{M-1}\sum_{n=0}^{N-1}p_{mn}\int_{mL_x/M}^{(m+1)\frac{L_x}{M}}\int_{nL_y/N}^{(n+1)\frac{L_y}{N}}\upsilon_{ij}(x',y')dx'dy'\\
&= \frac{4L_xL_y}{ij\pi^2}\sin\left(\frac{i\pi}{2M}\right)\sin\left(\frac{j\pi}{2N}\right)\\
&\quad *\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}p_{mn}\cos\left(\frac{i\pi(2m+1)}{2M}\right)\cos\left(\frac{j\pi(2n+1)}{2N}\right) \qquad (25)
\end{aligned}$$

The second term on the right hand side of (25) is a form of type-I DCT, thus, the formula can be simplified as follows:

$$P_{ij} = C_{ij} * \hat{P}_{ij} \qquad (26)$$

where

$$\hat{P}_{ij} = \mathrm{DCT}\,[p_{mn}] \qquad (27)$$

$$C_{ij} = \frac{4L_xL_y}{ij\pi^2}\sin\left(\frac{i\pi}{2M}\right)\sin\left(\frac{j\pi}{2N}\right) \qquad (28)$$

$$D_{ij} = \frac{4MN}{ij\pi^2}\sin\left(\frac{i\pi}{2M}\right)\sin\left(\frac{j\pi}{2N}\right) \qquad (29)$$

$$E_{ij} = C_{ij} * D_{ij} \qquad (30)$$

$$T_k = \int_{-L_z}^{0}\upsilon_k(z')dz' \qquad (31)$$

$$Z_{ij} = \sum_{k=0}^{N_z-1}\frac{T_k\upsilon_k(0)}{\kappa\omega^2 N_{ijk}}. \qquad (32)$$

Equation (30) cannot be evaluated when $i = 0$ and $j = 0$, l'Hopital's rule is applied to approximate the value of E_{ij} when $i \approx 0$ and $j \approx 0$. E_{ij} can then be expressed as follows:

$$E_{ij} = \begin{cases}
\triangle x \triangle y & i = 0, j = 0\\
\frac{4NL_y\triangle x\sin^2\left(\frac{j\pi}{2N}\right)}{j^2\pi^2} & i = 0, j \neq 0\\
\frac{4ML_x\triangle y\sin^2\left(\frac{i\pi}{2M}\right)}{i^2\pi^2} & i \neq 0, j = 0\\
\frac{16MNL_xL_y\sin^2\left(\frac{i\pi}{2M}\right)\sin^2\left(\frac{j\pi}{2N}\right)}{i^2j^2\pi^4} & i \neq 0, j \neq 0.
\end{cases} \qquad (33)$$

Equation (23) is also a form of type-I inverse DCT (IDCT) of $E_{ij} * \hat{P}_{ij} * Z_{ij}$. Solving DCT and IDCT directly requires complexity of $O(N^4)$. However, time complexity $O(N\log N)$ can be achieved by applying input reordering by realizing DCT using DFT. The runtime can be further be enhanced by calculating E_{ij} and Z_{ij} beforehand as both terms are independent to the geometry of power density. In short, the final temperature profile all comes down to (23).

IV. Maximum Temperature Reduction at Global Placement Stage

In this section, we present a thermal aware placer integrated with the analytical thermal model presented in Section III. The flow diagram of the thermal aware placer is shown in Fig. 4. The proposed algorithm implemented in this paper is implemented under the SimPL framework [2]. An overview is provided to get a brief idea of the SimPL [2] framework, then we present how to integrate an additional thermal constraint to the framework to achieve temperature reduction.

A. Overview of the SimPL Framework

In the SimPL [2] framework, two placement algorithms are implemented. One greedily minimizes the total wirelength and the other spreads out the cells to remove overlap. The two placement algorithms interleave with one another, solution generated by one placement algorithm serves as input to another. The terminating condition is when the difference

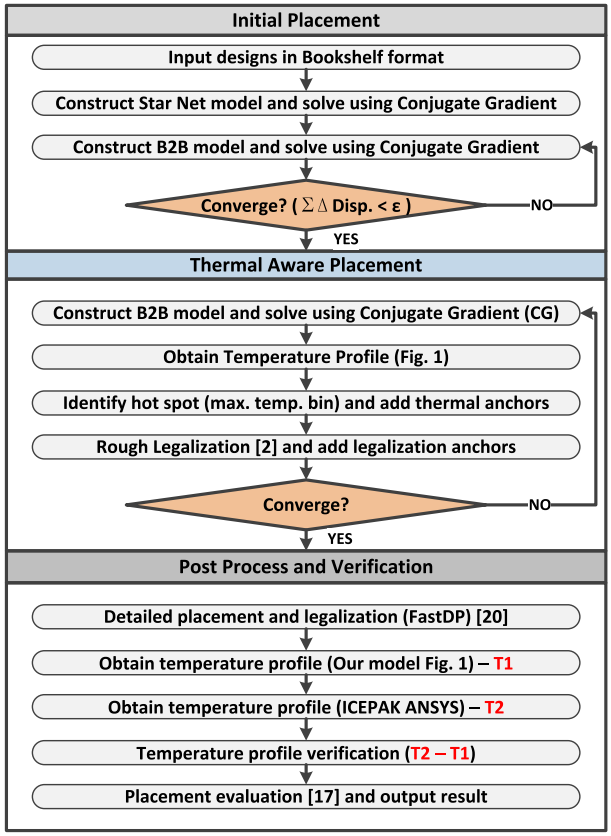

Fig. 4. Flow diagram of the proposed thermal aware placer.

in HPWL generated by two placements is less than a certain threshold. In other words, the entire framework terminates when $|\text{HPW}L_i - \text{HPW}L_{i-1}| \leq \beta$ where β is an empirical value.

Minimization of wirelength is based on a quadratic wirelength model where net weight is defined in (34). Variable (x_i, y_i) and (x_j, y_j) are the coordinate of cell c_i and c_j. The summation of all net weight is defined in (35). The solution on coordinates of cells with a minimum net weight can be obtained by solving $Q_x X = -d_x$ and $Q_y Y = -d_y$. Q_x and Q_y are positive semidefinite matrices that can be solved efficiently through conjugate gradient method

$$E_{ij} = \frac{1}{2} W_{ij} \left[\left(x_i - x_j\right)^2 + \left(y_i - y_j\right)^2 \right] \tag{34}$$

$$\phi(x, y) = \sum_{i,j} E_{ij} = \frac{1}{2} x^T Q_x X + d_x^T X + \frac{1}{2} y^T Q_y Y + d_y^T Y. \tag{35}$$

The cell spreading mechanism relies on a intuitive partition method called rough legalization. The given placement is partitioned into set of bins. For bins where cell density is above a certain threshold, the cells are evenly spread out to a preidentified region. In early iteration of the placement, bin size is set large since result of the legalization does not require to be exact. As iteration number increases, bin size decreases to have more accurate grasp toward congested region. The cell locations obtained in rough legalization then act as anchors by adding an additional constraint to matrices d_x and d_y to spread out cells. To distinguish the anchors to spread out cells and anchors to reduce maximum temperature, we name the anchors obtained in rough legalization as legalization anchors.

Equations (36) and (37) defines the weight of legalization anchors. Variable (x_l, y_l) is the coordinate of the legalization anchor corresponding to cell c_i. Variables (x_i, y_i) denotes the coordinate for cell c_i. The variable α is an empirical variable to accelerate convergence rate

$$W_{X,\text{legal}} = \alpha \cdot \frac{n}{|x_l - x_i|} \tag{36}$$

$$W_{Y,\text{legal}} = \alpha \cdot \frac{n}{|y_l - y_i|}. \tag{37}$$

B. Considering Thermal Effect in the SimPL Framework

A cell in the SimPL framework has two forces act upon. One is a net force that minimizes the wirelength and the other is a move force that removes overlap. Under this framework, we can integrate an additional move force that moves cells away from hot spot. Using the analytical method proposed in Section III, a temperature profile can be quickly obtained with a power density distribution.

In this paper, our goal is to minimize the maximum temperature. Thus, we propose a greedy approach to select a bin with the maximum temperature and reduce the temperature in the selected region on each iteration of the SimPL framework. Recall from Section III that analytical approach based on Green function divides the design to $M \times N$ bins where each bin holds the summation of power density of all cells located in that bin. The temperature profile reports the temperature value for each bin. A maximum temperature bin is selected after each thermal analysis.

Contrary to cell spreading mechanism to reduce the cell density, reducing the maximum temperature cannot be effectively achieved by simply moving all the cells away from one bin to the neighboring bins. The temperature of a bin is contributed by every other power densities from other bins. Simply moving the cells away from the maximum temperature bin, the regional power density still remains the same and the temperature cannot be effectively reduced. To effectively reduce the maximum temperature, it requires movement of cells at larger scale.

After a maximum temperature bin is identified, it clusters neighboring bins to build a hot region. Using identified hot region as center, the move bound of the cells is defined by an imaginary circle with radius R. For each cell within the hot region, a pseudoanchor is created and placed at the perimeter of circle. We define these anchors as thermal anchors, which serve to reduce the maximum temperature by moving cells away from hot region.

Each cell in the hot region is paired with a thermal anchor positioned at perimeter of move bound that directs cell away from the center. The scenario where cells within the hot region is exerted by a move forces from legalization anchor and a move force from thermal anchor is shown in Fig. 5. To obtain the position of thermal anchors, we first calculate the vectors from cell c_i to the center of hot region. Variable (x_i, y_i) is the coordinate of cell c_i and (x_o, y_o) are the coordinate of the

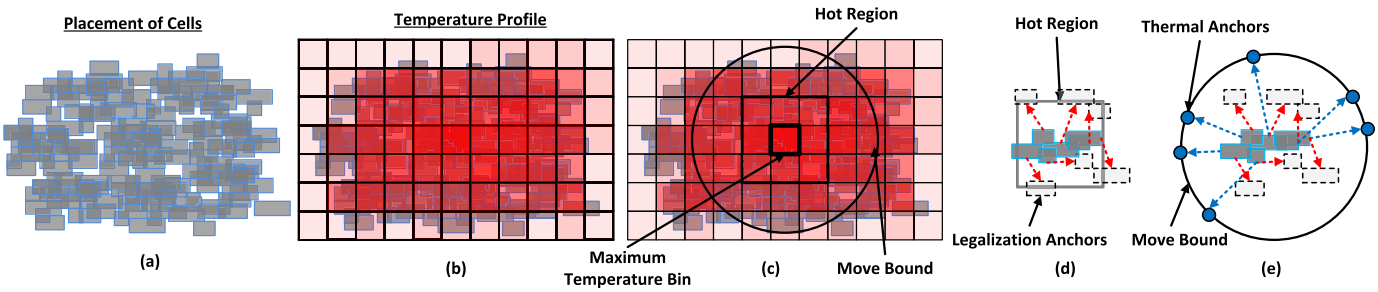

Fig. 5. Illustration of move force exerted on cells within the hot region. (a) Placement of cells after wirelength minimization. (b) Placement is divided to $M \times N$ grid and thermal analysis is conducted. (c) Maximum temperature bin is identified, neighboring bins are clustered to form the hot region, and move bound is defined around the hot region. (d) Move force exerted by legalization anchors. (e) Move force exerted by thermal anchor.

center point. Equation (40) is the coordinate of thermal anchor c_{ti} connecting to cell c_i

$$\vec{x} = x_i - x_o, \quad \vec{y} = y_i - y_o \tag{38}$$

$$\beta = \sqrt[2]{\frac{R^2}{\vec{x}^2 + \vec{y}^2}} \tag{39}$$

$$(x_{ti}, y_{ti}) = (x_o, y_o) + \beta \cdot (\vec{x}, \vec{y}). \tag{40}$$

1) Dynamic Hot Region Size Control: In the SimPL framework, as iteration number increases, the general structure of placement begins to form as cells become less congested. To have a better grasp toward congestion area, the size of bin decreases on each iteration and net weight of legalization anchor increases on each iteration.

In SimPL framework, the size of bin is decreased on each iteration. To cope with this framework, we scale down the size of hot region on each iteration to avoid perturbing too many cells. In our implementation, we initially set the size of hot region to a maximum of 13 bins in width and height and decrease the bin size by average of 2.5% on each iteration. The decrease in hot region size is accompanied by increase in net weight of thermal anchors. In short, larger hot region is accompanied by smaller net weight of thermal anchors and smaller hot region is accompanied by larger net weight of thermal anchors. We found empirically that through balance on size of hot region and net weight of thermal anchors can offer better tradeoff between the maximum temperature reduction and increase in HPWL.

2) Determining Net Weight of Thermal Anchors: Cell within the hot region has a move force exerted by a legalization anchor and a move force exerted by a thermal anchor. We explain how to adjust the net weight for the two types of anchors.

In early iterations, legalization anchors that pulls cells away from congested region also effectively reduces regional power density. This is because at early stage of placement, cells are congested in few clusters. There is not much difference between the move force that removes the cell density and the move force that removes power density. Thus, we let the net weight of legalization anchors dominate over thermal anchors at early stage and then gradually increase the proportion of thermal anchors as iteration number increases. The net weight of the thermal anchors is set proportional to n^2/N where n is the iteration number and N is the total iteration number in the

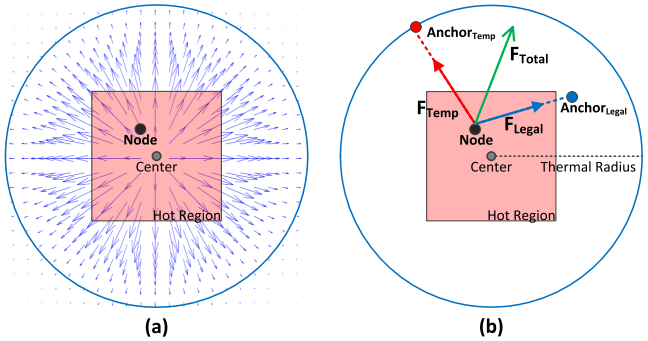

Fig. 6. Illustrations of adding move force from thermal anchor. (a) Illustration of 2D Gaussian model over the hot region. (b) Illustration of move force from legalization anchor and thermal anchor exerted on a node in the hot region.

SimPL framework. Thus, at early stage, the proportion on net weight of thermal anchor is negligible. As iteration number approaches to N, the net weight of legalization anchors and thermal have equal proportion.

To accelerate the convergence rate, the net weight of legalization anchors is adjusted by constant variable α. The same variable is applied on thermal anchor such that without any other net weight adjustment, the net weight of thermal anchor and legalization anchor are the same. We found by applying the same adjustment to thermal anchors results in rapid increase in HPWL. Thus, instead of applying a constant variable, the adjustment variable is determined through 2-D Gaussian distribution. The 2-D Gaussian distribution adjusts the cells that are at the center of the hot region with a greater net weight. This approach seeks to minimize increase in HPWL while effectively reduce the maximum temperature. Fig. 6 is an illustration of applying Gaussian distribution over an identified hot region.

The 2-D Gaussian distribution is defined in (41) where variable A defines the peak value of Gaussian distribution. Combined with a quadratic net weight adjustment (n^2/N), the net weight of thermal anchor in X- and Y-direction is defined in (42) and (43), respectively. In (42) and (43), (x_i, y_i) is the coordinate for cell c_i and (x_{ti}, y_{ti}) is the coordinate of thermal anchor c_{ti} connecting to cell c_i. Variable σ_x and σ_y stands for standard deviation in x and y direction of the cells within the hot region. The change in HPWL and reduction in maximum temperature for test case *adaptec1* for different settings is

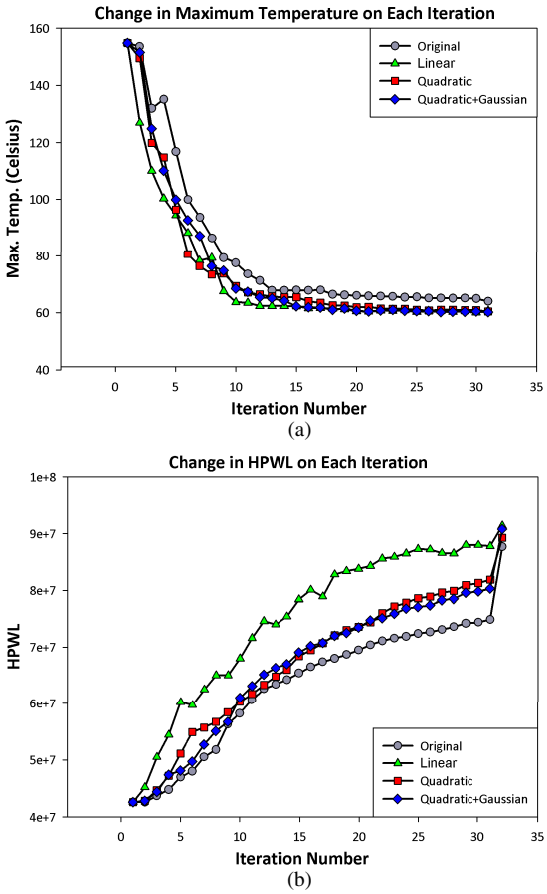

Fig. 7. Illustration on change in maximum temperature and HPWL for different weight adjustment scheme of thermal anchor. This experiment is performed on testcase adaptec1. (a) Change in maximum temperature on each iteration. (b) Change in HPWL on each iteration.

shown in Fig 7. It can be observed that using quadratic weight combined with Gaussian adjustment, the increase in HPWL on each iteration is less aggressive but just as effective in a maximum temperature reduction compared with a linear weight setting. In the experiment shown in Fig. 7, each setting has different initial value. The weight on linear setting of thermal anchor is set equal to the weight of legalization anchor such that proportion between legalization anchor and thermal anchor is equal throughout the iterative process. The settings on quadratic and Gaussian adjustment show that by adjusting the weight of thermal anchor to a negligible proportion in the beginning and gradually increases its proportion at latter stage are more efficient in reducing maximum temperature

$$g(x,y) = Ae^{-\left(\frac{(x_i-x_o)^2}{2\sigma_x^2}+\frac{(y_i-y_o)^2}{2\sigma_y^2}\right)} \tag{41}$$

$$W_{X,\text{thermal}} = g(x,y)\cdot\alpha\frac{(n)^2}{N}\cdot\frac{1}{|x_{ti}-x_i|} \tag{42}$$

$$W_{Y,\text{thermal}} = g(x,y)\cdot\alpha\frac{(n)^2}{N}\cdot\frac{1}{|y_{ti}-y_i|}. \tag{43}$$

V. Experimental Results

In this section, experimental results are presented in two subsections. First subsection presents the accuracy of the thermal model comparing to Icepak. In second subsection, we compare temperature distribution and total HPWL with and without considering the thermal effect.

TABLE III
PARAMETERS USED IN THERMAL MODEL

Parameters	Value
Chip W, H	Case dependent, given in ISPD benchmark
Chip thickness	0.5mm
Thermal conductivity κ	148 $W/(m\cdot^{\circ}C)$
Heat transfer rate h_p	8700 $W/(m^2\cdot C)$
Heat transfer rate h_s	2017 $W/(m^2\cdot C)$
Power density for each cell	Random value from 0 to $2*10^6$ W/m^2
Ambient temperature	22.02°C
Bin number M,N	128
Number of eigenvectors N_x, N_y	128
Grid dimension used in Icepak	64*64

The entire thermal aware placer is written in standard C++ language and compiled using g++ 4.1.2. Our placer is performed using Intel Xeon E5530 Quad Core machine operating at 2.4 GHz with 8-GB memory. ISPD 2005 placement benchmark [26] is used for input benchmark. Final legalization and detail placement are delegated to an external binary FastDP [27]. An open-source C-code-based FFT solver [28] is used in computation to generate temperature profile. All of the test cases are performed using same parameter without tuning for a specific test case. The total HPWL is evaluated using open source GSRC bookshelf evaluator [17] and every temperature profile is evaluated with ANSYS Icepak [29] after legalization.

A. Verification of Thermal Model

To examine the accuracy of our thermal model, we compare the temperature profile generated by our thermal analysis model to ANSYS ICEPAK [29]. ANSYS ICEPAK is a computational fluid dynamic engine for high accurate temperature profiling. It is constructed based on ANSYS FLUENT solver [30]. Parameters used in [7] was used in our thermal analysis. Table III lists the value of parameters used in our thermal analysis. Grid number used in ANSYS ICEPAK is set to 64.[1]

Fig. 8 compares the temperature profile of our thermal analysis with ANSYS ICEPAK. High resemblance can be observed between our temperature profiles with ANSYS ICEPAK. The numerical results for all of the eight test cases are shown in Table IV. Maximum and average temperature with and without considering the thermal effect is presented. Deviation of temperature distribution for each test case is calculated by taking the average of the temperature difference for each grid between temperature calculated in our thermal model and temperature obtained from ICEPAK. Execution time is the time required to generate a thermal profile for one given placement. On average, our thermal model achieves an accuracy within 3.0% deviation compared with ANSYS Icepak with 242 times speedup.[2]

[1]Setting higher grid number results entire program to crash in our environment.

[2]ANSYS ICEPAK are built for commercial use which have its specific data structure and interface. It is designed for thermal analysis that requires high accuracy. The comparison with ANSYS ICEPAK only serves to demonstrate that a standalone and efficient thermal aware framework can be implemented based on an analytical thermal analysis with minimal loss of accuracy.

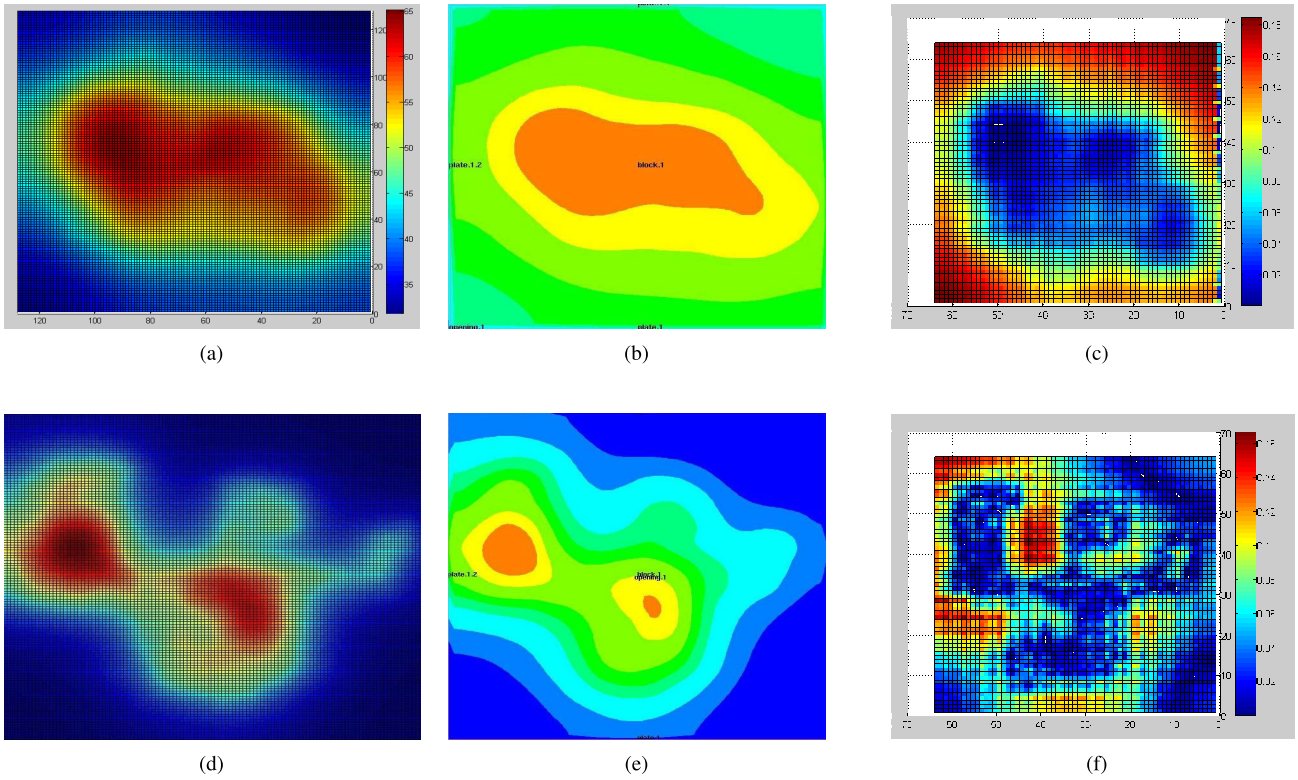

Fig. 8. (a) Temperature distribution for test case adaptec1 using our thermal model. (b) Temperature distribution for test case adaptec1 using Icepak. (c) Relative error for test case adaptec1 by comparing temperature value in each grid using our thermal model with Icepak. (d) Temperature distribution for test case bigblue3 using our thermal model. (e) Temperature distribution for test case bigblue3 using Icepak. (f) Relative error for test case bigblue3 by comparing temperature value in each grid using our thermal model with Icepak. It should be noted that all of the analyses are performed after legalization.

TABLE IV

COMPARISON OF TEMPERATURE PROFILE AFTER LEGALIZATION WITH AND WITHOUT CONSIDERING THERMAL EFFECT USING OUR THERMAL MODEL WITH ICEPAK

	Without Thermal					**With Thermal**					**Max Temp.**	
	Our		**Icepak**			**Our**		**Icepak**			**Red. (%)**	
#	Max.(°C)	Time(s.)	Max.(°C)	Time(s)	Dev.(%)	Max.(°C)	Time(s)	Max.(°C)	Time(s.)	Dev.(%)	Our	IcePak
adaptec1	63.95	0.74	63.78	219.71	2.66	60.21	0.51	61.62	247.54	2.29	5.85	3.39
adaptec2	50.44	0.64	48.02	235.02	5.03	50.45	0.43	48.38	235.82	4.28	-0.02	-0.75
adaptec3	46.14	0.68	45.20	236.67	3.69	44.01	0.67	42.22	240.66	4.24	6.10	6.60
adaptec4	46.57	0.71	46.82	242.68	5.33	45.18	0.71	45.86	250.83	1.48	2.98	2.05
bigblue1	73.54	0.51	73.41	225.46	1.77	70.77	0.52	71.36	234.69	0.83	3.77	2.79
bigblue2	52.09	0.75	53.56	209.26	2.74	51.03	0.75	53.25	247.39	4.17	2.03	0.58
bigblue3	73.79	1.24	71.52	218.39	3.17	65.46	1.35	64.61	231.09	1.32	11.29	9.66
bigblue4	75.35	2.19	77.67	222.37	2.99	72.37	2.42	75.49	234.55	4.13	3.95	2.81
Avg.	-	**0.93**	-	**226.20**	**2.32**	-	**0.92**	-	**240.32**	**2.84**	**4.50**	**3.39**

TABLE V

REDUCTION OF MAXIMUM ON CHIP TEMPERATURE BY ADJUSTING WEIGHT OF THERMAL ANCHOR USING LINEAR, QUADRATIC, AND QUADRATIC + GAUSSIAN MODEL (IN THIS PAPER, $\alpha = 0.08$ AND $N = 30$)

		Original		**Lin. Wt.** $W = \alpha n$			**Quad. Wt.** $W = \alpha n^2/N$			**Quad. Wt. + Gaus.** $W = g(x,y)\alpha(n)^2/N$		
Benchmarks	**Cell#**	**HPWL**	**Temp.**	**HPWL**	**Temp.**	**Red.(%)**	**HPWL**	**Temp.**	**Red.(%)**	**HPWL**	**Temp.**	**Red.(%)**
adaptec1	211K	87.69	63.95	91.40	60.72	5.05	89.33	60.43	5.50	90.76	60.21	5.85
adaptec2	255K	98.22	50.44	115.86	49.25	2.36	109.94	52.96	-5.00	105.76	50.45	-0.02
adaptec3	452K	242.49	46.14	282.51	49.68	-6.00	274.06	45.02	3.94	258.81	44.01	6.10
adaptec4	496K	212.09	46.57	219.20	44.43	4.59	228.01	45.33	2.66	219.12	45.18	2.98
bigblue1	278K	107.46	73.54	126.37	71.39	2.92	123.76	71.25	3.11	118.61	70.77	3.77
bigblue2	558K	155.53	52.09	160.73	53.22	-2.17	166.15	51.46	1.21	163.46	51.03	2.03
bigblue3	1110K	378.09	73.79	524.75	67.42	8.63	474.70	62.28	15.60	439.27	65.46	11.29
bigblue4	2180K	897.69	75.35	935.53	66.55	2.05	947.73	66.88	11.24	909.50	72.37	3.95
Norm.	-	**1.00**	**1.00**	**1.15**	**0.98**	**2.18**	**1.11**	**0.95**	**4.79**	**1.07**	**0.95**	**4.50**

B. Thermal Aware Placer

Table V lists the different settings on net weight of thermal anchors. The first setting sets net weight of thermal anchor equal to the net weight of legalization anchor, which linearly increases with iteration number n. The second setting sets the net weight of thermal anchor to n/N and third setting configures the adjustment variable to $G(x, y)$, which stands for Gaussian distribution. The first setting has maximum temperature reduction by 2.2% at the expense of 15% increase in

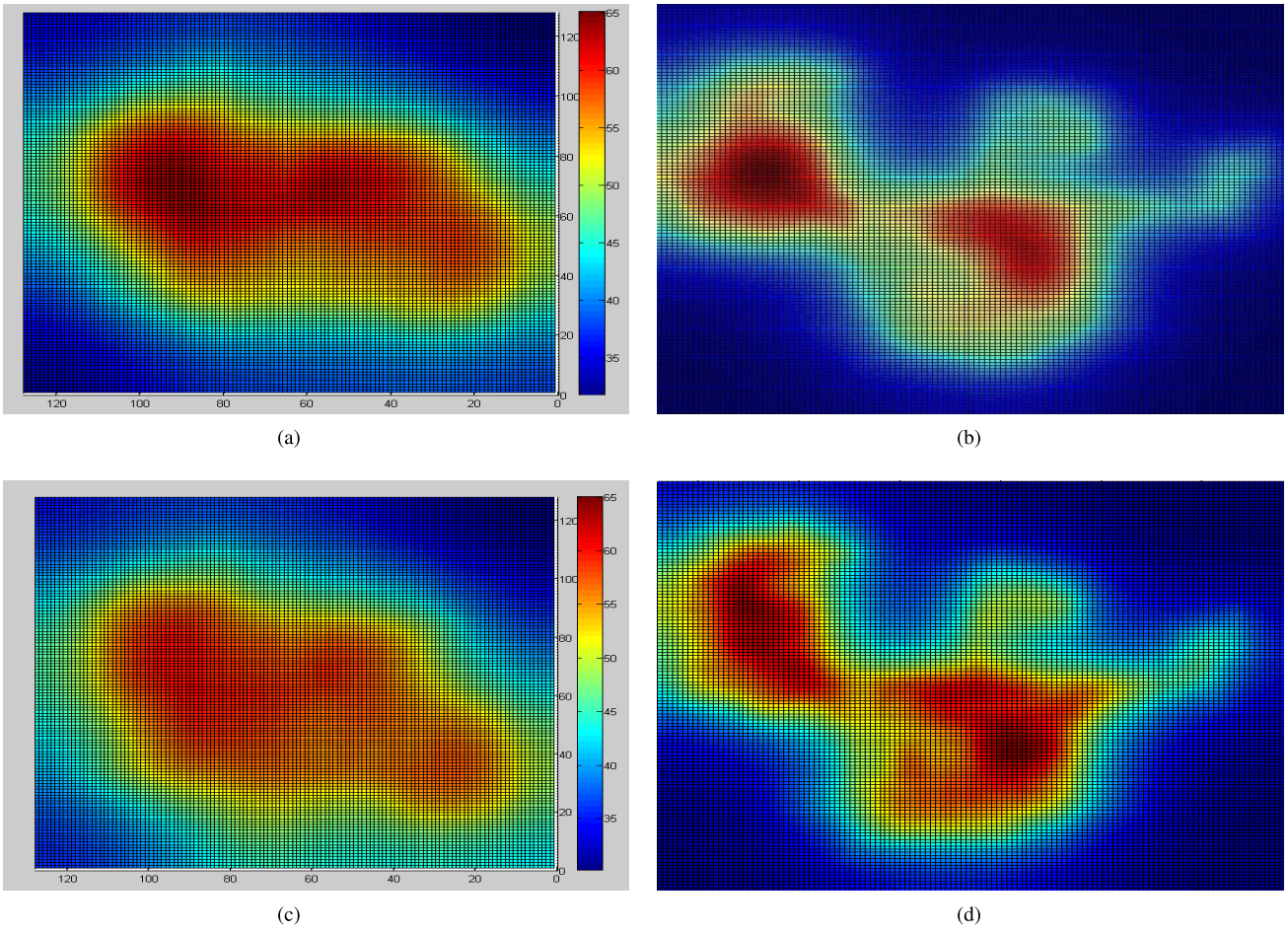

Fig. 9. Temperature distribution with and without consideration of thermal effect for test case adaptec1 and bigblue3. It can be observed that hot region is removed and temperature distribution is smoother when thermal effect is considered during placement stage. (a) Temperature distribution of adaptec1 without consideration thermal effect. (b) Temperature distribution of bigblue3 without consideration thermal effect. (c) Temperature distribution of adaptec1 with consideration thermal effect. (d) Temperature distribution of bigblue3 with consideration thermal effect.

TABLE VI

COMPARISON WITH PRIOR WORKS [24], [25] ON TEMPERATURE MITIGATION TECHNIQUES ON MAXIMUM TEMPERATURE T_{max} AND HPWL (GP: ALGORITHM TOOK PLACE DURING GLOBAL PLACEMENT STAGE. PP: TECHNIQUE TOOK PLACE DURING POSTPLACEMENT STAGE)

		Original		**Chu et. al. [24]**		**Liu et. al. [25]**		**Our**	
GP/PP		**-**		**PP**		**PP**		**GP**	
Benchmarks	**Cell#**	T_{max}	**HPWL**	T_{max}	**HPWL**	T_{max}	**HPWL**	T_{max}	**HPWL**
adaptec1	211K	63.95	87.69	47.79	LG Fail	61.23	108.21	60.21	90.76
adaptec2	255K	50.44	98.22	35.92	LG Fail	50.28	108.68	50.45	105.76
adaptec3	452K	46.14	248.00	33.11	LG Fail	45.52	290.60	44.01	258.81
adaptec4	496K	46.57	212.09	33.91	LG Fail	45.32	291.92	45.18	219.12
bigblue1	278K	73.54	107.46	51.23	LG Fail	70.56	121.31	70.77	118.61
bigblue2	558K	52.09	155.53	41.04	LG Fail	50.82	178.86	51.03	163.46
bigblue3	1110K	73.79	378.09	39.98	LG Fail	69.56	472.95	65.46	439.27
bigblue4	2180K	75.35	897.69	45.41	LG Fail	72.34	1093.94	72.37	909.50
Norm.	**-**	**1.042**	**0.941**	**0.719**	**-**	**1.013**	**1.131**	**1.000**	**1.000**

HPWL. The second and third setting demonstrates by properly adjusting the proportion on net weight of thermal anchors, better tradeoff between HPWL and temperature can be obtained. In the third setting, we can achieve 4.5% reduction in maximum temperature with 7% increase in total HPWL. Detailed placer in general is local optimization of cells, which does not significantly change the regional power density. According to our observation, the temperature difference before and after the detailed placer has a mean deviation less than 0.6%. We have noticed in test case adaptec2, the maximum temperature actually increases after the thermal aware optimization, this may be due to the higher percentage of macro blocks in adaptec2, which creates barrier to move cells away from hot spot.

The temperature distribution of adaptec1 and bigblue3 with and without consideration of thermal effect is shown in Fig. 9. Maximum temperature for Fig. 9(c) is 5.85% less than Fig. 9(a) with 3.5% increase in total HPWL. It can be observed

that a smoother temperature distribution can be obtained by considering the thermal effect.

We reimplemented this paper done in [24] and empty row insertion proposed in [25]. In comparison with [25], our proposed technique achieves additional 1.3% maximum temperature reduction with 13.1% less HPWL. In implementation of [24], t is set to two and total bin number is set to 128×128. In implementation of [25], row insertion is achieved by shifting cells upward/downward since proposed technique does not consider presence of hard macros.

In Table VI, our proposed force model method can significantly decrease maximum temperature by 4.2% compared with original placement. Techniques proposed in [24] achieves best temperature reduction by redistributing power across entire chip, however, such greedy approach also significantly increase HPWL and leads to failure during legalization on all eight test cases.[3] Nevertheless, result from [24] offers an indication to the upper bound of temperature reduction.

VI. Conclusion

In this paper, we proposed a thermal aware placer using an analytical thermal model integrated with an analytical placer-based quadratic wirelength model. The analytical thermal model was implemented using Green function and temperature profile was solved using DCT with input reordering to enhance speed. Analytical thermal model can offer closed form thermal representation with a negligible run time. Although analytical thermal model was less accurate compared to numerical approach, it can obtain the temperature profile much faster within reasonable accuracy. Such characteristic was very suitable for thermal analysis during the placement or floorplanning stage where thermal analysis does not required to be very exact.

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