A 160-GHz Frequency-Translation Phase-Locked Loop With RSSI Assisted Frequency Acquisition

Wei-Zen Chen, Tai-You Lu, Yan-Ting Wang, Jhong-Ting Jian, Yi-Hung Yang, and Kai-Ting Chang

***Abstract*—A 160-GHz frequency-translation PLL with tuning range from 156.4 GHz to 159.2 GHz is presented. Sub-THz 1/9 prescaler is replaced by a 3rd harmonic mixer incorporating a frequency tripler for frequency down conversion. A transformer-based VCO is utilized to alleviate capacitive and resistive load associated with varactor and succeeding buffer stages. Frequency acquisition is assisted by received signal strength indicator (RSSI) for automatic frequency sweeping and fast locking. Fabricated in 65 nm CMOS technology, the chip size is 0.92 mm^2. The PLL locking time is less than 3 μs. This chip drains 24 mW from a 1.2 V power supply.**

***Index Terms*—Harmonic mixer, PLL, RSSI, tripler.**

I. Introduction

CMOS Terahertz (THz) systems are considered as emerging technology for advanced imaging and spectroscopy for sensing and detection applications, and have drawn tremendous research efforts recently [1], [2]. As limited by the unity maximum available power gain frequency of transistor ($\mathrm{f_{max}}$), CMOS THz signal generators rely on the harmonic generation of a sub-THz reference using phase combination or push-push techniques [3], [4]. To implement a high speed phase-locked loop, multi-stage cascaded injection-locked frequency dividers (ILFD) [5]–[7] are commonly used in the feedback path to down covert the VCO output frequency for phase comparison. For the oscillation frequency close to hundreds of GHz range, the frequency tuning ranges of both VCO and ILFD become very limited, which are highly susceptible to parasitic effects associated with the buffer stage and interconnects. As the ILFD is prone to self-oscillation without properly injection locked, frequency misalignments in feedback chain are susceptible to PVT variations and may cause the loop fail to lock. To circumvent the critical issue, this paper proposes a novel frequency-translation PLL (FT-PLL) for over 100 GHz operations.

In the proposed FT-PLL, high speed prescalers are replaced by a harmonic mixer incorporating frequency tripler to down convert VCO frequency from sub-THz to around 1 GHz, which can be easily scaled down by digital divider. Besides, a received signal strength indicator (RSSI) is used for automatic frequency sweeping to overcome PVT variations and extend locking range.

This paper is organized as follows. Section II describes the proposed FT-PLL architecture and operation principle. The system behavior is discussed in Section III. Section IV describes the detailed circuit schematic. Experimental results are shown in Section V, and Section VI concludes this paper.

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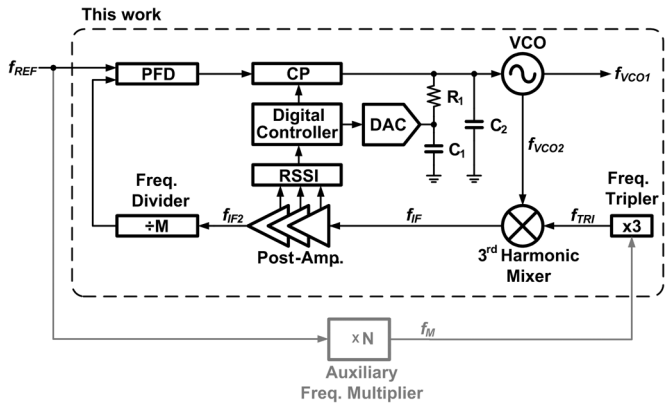


Fig. 1. FT-PLL architecture.

II. Architecture

Fig. 1 depicts the proposed FT-PLL architecture. The sub-THz output frequency (f_{VCO}) is generated from an on-chip LC oscillator. To down convert f_{VCO} for phase comparison, an auxiliary frequency multiplier generates f_M ($\mathrm{N}f_{REF}$), whose output frequency is then tripled (f_{TRI}) by an on chip frequency tripler to drive a 3rd harmonic mixer. Through harmonic mixing with f_{TRI}, f_{VCO} is translated to a much lower frequency band (f_{IF}) [8], and then enlarged by a post amplifier to drive a digital frequency divider (1/M). When the loop is locked, we have

$$f_{TRI} = 3f_M = 3Nf_{REF} \tag{1}$$

$$f_{VCO} - 3f_{TRI} = M_{REF} \tag{2}$$

$$f_{VCO} = (9N + M)f_{REF}. \tag{3}$$

It can be seen that the frequency tripler incorporating with 3rd harmonic mixer performs the same function as a 1/9 prescaler, and f_{VCO} can be adjusted by programming the divide ratio M or the frequency multiplication factor N. To alleviate bandwidth requirement of frequency tripler, f_M is fixed in this design. It also facilitates the optimization of frequency tripler and harmonic mixer. Besides, the bandwidth of post amplifier is designed to cover the frequency tuning range of $\mathrm{M}f_{REF}$. It en-

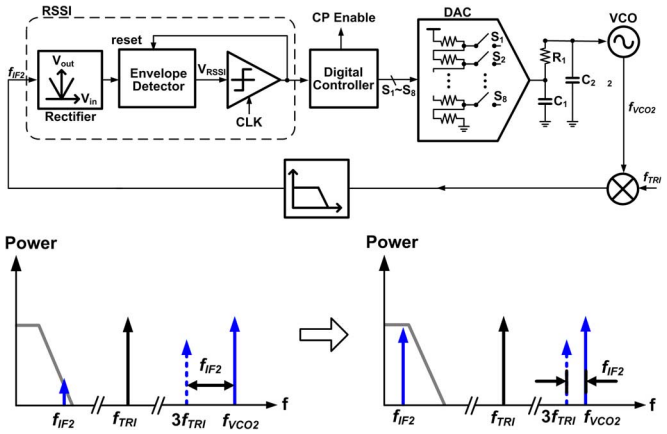


Fig. 2. PLL with RSSI assisted frequency tracking scheme.

larges the signal swing of f_{IF} to logic level for a proper operation of digital divider.

Using a mixer for frequency down conversion, the alternative solution of f_{IF} is at $3f_{TRI} - f_{VCO}$. To avoid this ambiguity, the oscillator free running frequency is preset to its highest frequency at the onset of frequency switching, which is higher than $3f_{TRI}$ to guarantee a single mode operation.

The procedure for phase and frequency locking is described as follows. When the channel switching command is issued, the VCO is preset to its highest frequency controlled by a 3 bits resistor ladder DAC, and the PLL is opened loop by disabling the charge pump current. Meanwhile, the received signal strength indicator (RSSI) continues monitoring the power level at f_{IF2}. Fig. 2 illustrates the frequency acquisition scheme incorporating RSSI. The harmonic mixer output is fed into a post voltage amplifier, and the RSSI is composed of a rectifier followed by an envelope detector and a comparator. The comparator output is stored in a digital controller to adjust the resistor ladder DAC. Once the DAC output is renewed, the envelope detector will be reset to track the new signal amplitude at f_{IF2}. Meanwhile, the VCO frequency f_{VCO} is adjusted by charging the loop filter capacitor C_1 through DAC. By the low-pass nature of the post voltage amplifier, for $f_{VCO} \gg 3f_{TRI}$, a higher f_{IF} leads to a smaller received signal amplitude. According to RSSI, the digital controller then updates the DAC contents in a descending way to reduce f_{VCO}, pulling in the frequency gradually to approach $3f_{TRI}$. As the f_{IF} falls into the bandwidth of post amplifier, its signal amplitude would become sufficiently larger to toggle the post frequency divider properly, as is illustrated in Fig. 2.

Moderated by the RSSI and level detector, this pull-in process will be finished when the signal amplitude at f_{IF2} exceeds the threshold level to drive the succeeding frequency divider. In this design, the input sensitivity of the post divider is around 150 mV, thus the threshold voltage of comparator is set to 180 mV to tolerate 20% PVT variation. The 3 bits DAC provides voltage tuning range of 0.9 V and corresponding frequency tuning range of 3 GHz. As the DAC is updated at 4 MHz, the frequency sweeping time is less than 2 μs. After the pull-in process monitored by RSSI, the digital controller then resumes the close loop operation by enabling the charge pump current, and keeps f_{VCO} phase tracking f_{REF}. The proposed frequency sweeping scheme brings f_{VCO} into its target frequency automatically, alleviating bandwidth requirement of the feedback path of PLL without sacrificing its locking range.

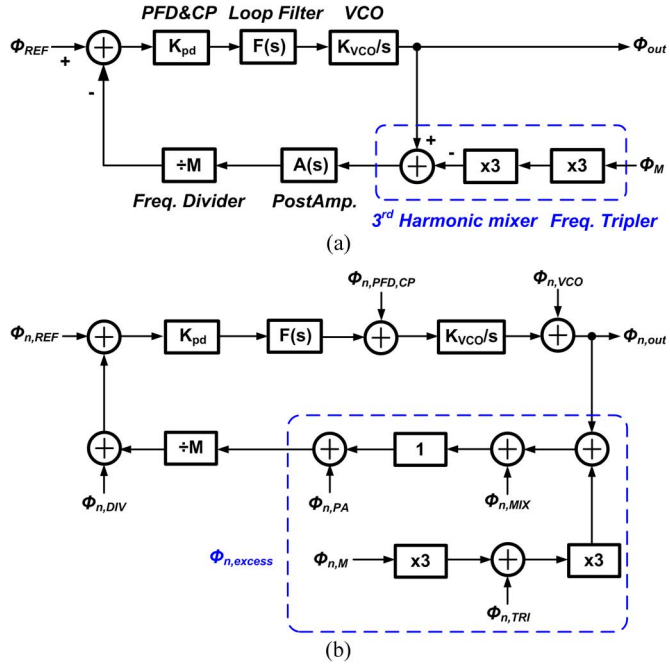


Fig. 3. (a) Frequency-translation PLL behavioral model (b) noise model.

III. Behavioral Model

To investigate behavior and phase noise performance of the proposed FT-PLL, its linear model is illustrated in Fig. 3(a). Here K_{pd} represents the gain of phase frequency detector (PFD) and charge pump (CP), K_{VCO} denotes VCO gain, $F(s)$ and $A(s)$ respectively represent the transfer function of loop filter and post amplifier. The linear model of 3rd harmonic mixer and frequency tripler is illustrated in the dashed box, which provides phase offset of $9\phi_M$ ($\mathrm{N}\phi_{REF}$) in the feedback path. The phase transfer function of ϕ_{REF} to ϕ_{out} can be derived as

$$\frac{\phi_{out}}{\phi_{REF}} = \frac{\left[1 + \frac{9NA(s)}{M}\right] G(s)}{1 + \frac{A(s)G(s)}{M}} \tag{4}$$

where $G(s) = K_{pd}K_{VCO}F(s)/s$. When the PLL is operating in phase tracking mode, f_{IF} falls within the post amplifier's -3 dB bandwidth, and the phase shift caused by $A(s)$ is negligible ($A(s) \approx 1$). Thus the system transfer function can be simplified as

$$\frac{\phi_{out}}{\phi_{REF}} = \left.\frac{\left[1 + \frac{9NA(s)}{M}\right] G(s)}{1 + \frac{A(s)G(s)}{M}}\right|_{G(s)\to\infty} = 9N + M \tag{5}$$

which is the same as that of a conventional PLL with frequency multiplication factor of $9N + M$. Fig. 3(b) illustrates the phase noise contribution from individual building blocks, where, $\phi_{n,REF}$, $\phi_{n,PFD,CP}$, $\phi_{n,VCO}$ and $\phi_{n,DIV}$ respectively represent the noise source from reference input, loop filter, VCO, and frequency divider in a typical charge-pump based PLL. Their impacts on the VCO phase noise ($\phi_{n,outi}$) can be respectively represented as

$$H_1(s) \equiv \frac{\phi_{n,out1}}{\phi_{n,REF}} = \frac{G(s)}{1 + \frac{G(s)}{M}} \tag{6}$$

$$H_2(s) \equiv \frac{\phi_{n,out2}}{\phi_{n,PFD,CP}} = \frac{\frac{1}{s}K_{VCO}}{1+\frac{G(s)}{M}} \tag{7}$$

$$H_3(s) \equiv \frac{\phi_{n,out3}}{\phi_{n,VCO}} = \frac{1}{1+\frac{G(s)}{M}} \tag{8}$$

$$H_4(s) \equiv \frac{\phi_{n,out4}}{\phi_{n,DIV}} = \frac{G(s)}{1+\frac{G(s)}{M}} \tag{9}$$

Assuming that the frequency multiplier output f_M is generated from an auxiliary PLL, its phase noise $(\phi_{n,M})$ can be described as

$$\phi_{n,M} \equiv H_a(s)\phi_{n,REF} + \phi_{n,AuxPLL} \tag{10}$$

where $H_a(s)$ represents the reference phase noise transfer function (low pass filtering) of the auxiliary PLL, whose DC gain equals to N (frequency multiplying factor), and $\phi_{n,AuxPLL}$ denotes other noise sources coming from the auxiliary PLL. Defining the excess noise source in the frequency-translation PLL (FT-PLL) as $\phi_{n,excess}$, where

$$\begin{aligned}\phi_{n,excess} &= 9\phi_{n,M} + 3\phi_{n,TRI} + \phi_{n,MIX} + \phi_{n,PA} \\ &= 9H_a(s)\phi_{n,REF} + 9\phi_{n,AuxPLL} + 3\phi_{n,TRI} \\ &\quad + \phi_{n,MIX} + \phi_{n,PA}.\end{aligned} \tag{11}$$

We have

$$H_5(s) \equiv \frac{\phi_{n,out5}}{\phi_{n,access}} = \frac{\frac{G(s)}{M}}{1+\frac{G(s)}{M}}. \tag{12}$$

Combing (6) and (12), it reveals that the reference phase noise transfer function $H_{REF}(s)$ can be described as

$$H_{REF}(s) = 9H_a(s)H_5(s) + H_1(s) \tag{13}$$

whose DC gain equals to $(9N + M)$. The 1st term corresponding to $9N$ is noise shaped by the cascaded loop filter $H_a(s)H_5(s)$, which facilitates optimization compared to a single loop architecture [9]. Meanwhile, the other terms in $\phi_{n,excess}$ $(9\phi_{n,AuxPLL} + 3\phi_{n,TRI+}\phi_{n,MIX+}\phi_{n,PA})$ are translated to VCO output as in-band noise without amplification. According to (7)–(9), the noise contribution from $\phi_{n,CP}$ and $\phi_{n,DIV}$ in the main loop is reduced from $(9N + M)$ to (M) in contrast to a single loop PLL. Additionally, in-band noise from VCO is suppressed by increasing the loop gain (feedback factor increases by $(9\mathrm{N} + \mathrm{M})/\mathrm{M}$ compared to single loop PLL). It provides some design margin to accommodate noise degradation caused by $\phi_{n,excess}$.

To sum up, the FT-PLL output phase noise $\phi_{n,out}$, can be expressed as

$$\overline{\phi^2_{n,out}} = \overline{\phi^2_{n,out1}} + \overline{\phi^2_{n,out2}} + \overline{\phi^2_{n,out3}} + \overline{\phi^2_{n,out4}} + \overline{\phi^2_{n,out5}} \tag{14}$$

Provided that the reference noise floor is -150 dBc/Hz at 1 MHz offset, $\mathrm{M} = 8$ and $\mathrm{N} = 134$, the loop bandwidth is chosen where the out-of-band noise and the loop noise contribute equally to the output jitter, the simulated in band phase noise is about -89 dBc/Hz.

IV. Building Blocks

Design considerations of the individual building blocks are described as follows.

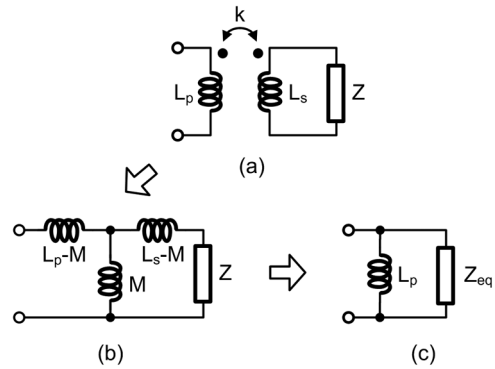


Fig. 4. The equivalent model of transformer.

A. Voltage Controlled Oscillator

As f_{VCO} approaches devices' $\mathrm{f_{max}}$, the parasitic resistance introduced by the LC tank and its succeeding buffer stages becomes a critical issue to maintain stable oscillation. Meanwhile, the parasitic capacitance severely limits the oscillation frequency of VCO. To overcome the design challenges, a transformer-based VCO is adopted.

To demonstrate the advantage of capacitive degeneration through magnetic coupling, Fig. 4(a) exemplifies a two-coil model for simplicity [10]. For a two-coil transformer with primary coil inductance of L_p, secondary coil inductance of L_s, mutual inductance of M, and coupling factor of k, its equivalent T-model can be depicted as shown in Fig. 4(b). When the secondary port is loaded with impedance (Z), the equivalent impedance (Z_{eq}) seen from the primary port and paralleled with $\mathrm{L_p}$, as shown in Fig. 4(c), becomes

$$Z_{eq} = \frac{1}{k^2}\left[\frac{L_p}{L_s}Z + j\omega L_p(1-k^2)\right]. \tag{15}$$

By choosing $(L_p/k^2L_s > 1)$, the loading effect associated with the secondary port can be reduced accordingly.

Fig. 5 illustrates the detail circuit schematic. The VCO core is composed of negative impedance converter $(M_1 - M_2)$ and the primary coil (L_p) of the transformer, while the varactors, buffer stage, and harmonic mixer are coupled to the resonator through an outer coil (L_{s1}) and inner coil (L_{s2}) respectively. As

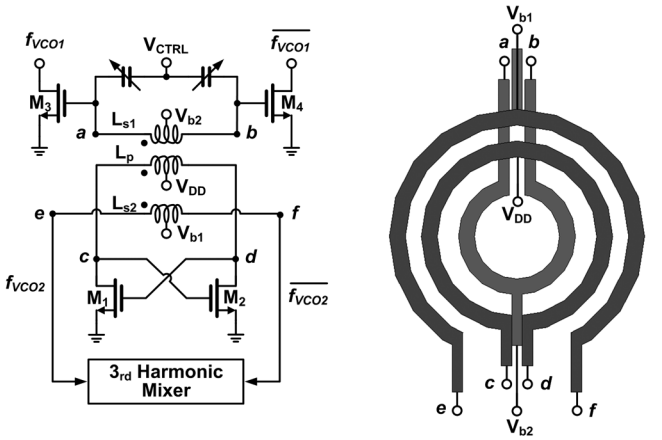
$$L_{s1} < L_p < L_{s2} \tag{16}$$

it also degenerates the tuning sensitivity of the varactor to maintain a high frequency oscillation. Meanwhile, the transformer coupling also provides voltage gain between the primary and secondary ports, where

$$\frac{v_o}{v_i} = k\sqrt{\frac{L_s}{L_p}}. \tag{17}$$

It provides the advantage to generate a higher voltage swing at the input of 3rd harmonic mixer. The detail layout of the triple-coil transformer and its parameters are also summarized in Fig. 5.

The transformer is laid out as micro strip lines using top metal, providing inductance of about 27.5 pH and self-resonant frequency of about 372 GHz. The coupling coefficients from the primary coil to the secondary and the third coil are about 0.103



	Width(μm)	Inductance(pH)	$f_{self\text{-}resonant}$ (GHz)
L_p	3	27.49	372.4
L_{s1}	3	22.32	399.3
L_{s2}	3	42.57	375.6

	Coupling factor
k_{ps1}	0.103
k_{ps2}	0.335

Fig. 5. VCO schematic.

and 0.335 respectively. By impedance transformation, the parasitic capacitance and resistance seen at the resonator are about 13 fF and 243 Ω as referred to the primary coil. For a varactor tuning range from 6.7 fF to 16.6 fF, the measured tuning range of the VCO is from 156.4 GHz to 159.2 GHz.

B. Frequency Tripler

Fig. 6 illustrates the circuit schematic of frequency tripler. The frequency tripler [11] is configured as a synchronous lock oscillator composing of M_3, M_4, and LC tank, whose output frequency (f_{TRI}) is tuned at $3Nf_{REF}$. The excitation signal (f_M) provided by the auxiliary frequency multiplier is injected differentially at $\mathrm{M_1}$ and $\mathrm{M_2}$ to generate the third harmonic tone of f_M, which is provided to synchronize the injection locked oscillator. Since both the f_M and f_{TRI} frequencies are fixed, it facilitates the optimization of the tripler design with maximum power gain by properly choosing the resonant frequency of the tank. As the locking range of the frequency tripler can be described as [12]

$$\omega_L = \frac{\omega_0}{2Q}\frac{I_3}{I_{osc}} \tag{18}$$

where ω_0 and Q represent the center frequency and quality factor of the LC tank, I_3 represents the third harmonic drain current of $\mathrm{M_1}$ and $\mathrm{M_2}$, and I_{osc} represents the DC current of the injection locked oscillator. The 3rd harmonic of the transconductance of $\mathrm{M_1}$ and $\mathrm{M_2}$ can be maximized to enhance the injection efficiency by properly choosing their conduction angle (ϕ) [13]. The strength of the third harmonic component under different conduction angle can be evaluated by normalizing its amplitude I_3 to that of the overall drain current I_{max}, where

$$\frac{I_3}{I_{\max}} = \frac{\sin\left(\frac{3\phi}{2}\right)\cos\left(\frac{\phi}{2}\right) - 3\cos\left(\frac{3\phi}{2}\right)\sin\left(\frac{\phi}{2}\right)}{12\pi\left(1-\cos\frac{\phi}{2}\right)}. \tag{19}$$

As shown in Fig. 7, the frequency tripler has the highest injection efficiency at the conduction angle of about 80°. Under this

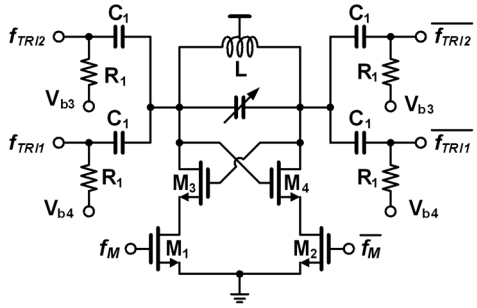


Fig. 6. Frequency tripler schematic.

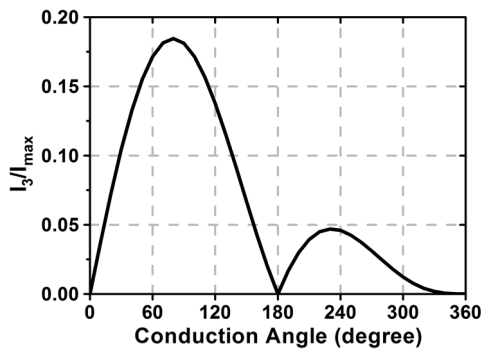


Fig. 7. Injection efficiency of frequency tripler under different conduction angle.

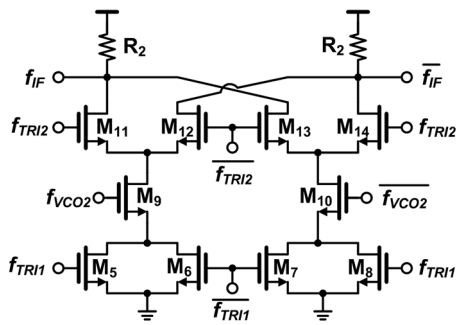


Fig. 8. 3rd harmonic mixer schematic.

circumstance, $\mathrm{M_1}$ and $\mathrm{M_2}$ are biased at sub-threshold region, which may cause the oscillator fail to start oscillation due to limited DC current. To overcome this issue, a conduction angle of about 240° is chosen in this design for a higher injection efficiency while meeting the oscillation criterion.

C. 3rd Harmonic Mixer

Fig. 8 illustrates the circuit schematic of 3rd harmonic mixer. It is composed of frequency doubler $(M_5 - M_8)$, a single transistor mixer $(M_9 - M_{10})$, and a double-balanced Gilbert switches $(M_{11} - M_{14})$ in cascode to reduce power consumption. f_{TRI} is injected differentially to the transistor $(M_5 - M_8)$ and $(M_{11} - M_{14})$, and the VCO output is applied to $(M_9 - M_{10})$ as f_{VCO2}.

Let

$$f_{TRI} = A_{TRI}(\cos\omega_{TRI}t) \tag{20}$$

and

$$f_{VCO2} = A_{VCO}(\cos\omega_{VCO}t). \tag{21}$$

The drain current of $M_5 - M_8$ can be expressed as [14]

$$i_{D5-8} \approx \left(\mu_n C_{ox} \frac{W}{L}\right)_{5-8} \left(V_{OV5-8}^2 + f_{TRI}^2 \pm 2V_{OV5-8} f_{TRI}\right) \tag{22}$$

where V_{OV5-8} are the overdrive voltages of $M_5 - M_8$.

By connecting the output currents of M_5, M_6, and M_7, M_8, the source voltage of M_9 and M_{10} can be approximated as

$$\begin{aligned} v_{s9} = v_{s10} &\approx (i_{D5} + i_{D6}) R_L \\ &\approx \frac{1}{2}\left(\mu_n C_{ox} \frac{W}{L}\right)_{5-8} A_{TRI}^2 R_L \cos 2\omega_{TRI} t + V_{DC} \end{aligned} \tag{23}$$

where R_L represents the effective impedance at the source node of M_9 and M_{10}, and V_{DC} denotes the DC voltage.

From (23), it can be seen that the odd order harmonics of f_{TRI} are cancelled out at the source of M_9 and M_{10}, while its even order harmonics remain. To maximize the second order harmonic tone of the frequency doubler, M_5 to M_8 are biased at subthreshold region to perform as ideal switches and boost the harmonic tones.

As the overdrive voltage of M_9 and M_{10} are modulated by the second order harmonic of f_{TRI} and f_{VCO2}, they perform as single transistor mixers through the nonlinearity of MOSFET I-V characteristic. Their output currents become

$$\begin{aligned} i_{d9,10} \approx{}& \frac{A_1}{2}\cos(2\omega_{TRI} - \omega_{VCO2})t + A_2 \cos \omega_{VCO2} t + \\ & A_3 \cos 2\omega_{TRI} t + \frac{A_1}{2}\cos(2\omega_{TRI} + \omega_{VCO2})t + \cdots \end{aligned} \tag{24}$$

where

$$A_1 = \left(\frac{\mu_n C_{ox}}{2}\frac{W}{L}\right)_{5-8} \left(\mu_n C_{ox} \frac{W}{L}\right)_{9-10} A_{VCO} A_{TRI}^2 R_L. \tag{25}$$

The other high frequency terms due to leakage (A_2, A_3) and harmonic tones are low pass filtered at the input of Gilbert switches. Thus the drain currents of M_9 and M_{10} are translated to $(f_{VCO} - 2f_{TRI})$ and flow through the commutating stages $M_{11} - M_{14}$ driven by f_{TRI} again.

The resulting down converted signal f_{IF} is at $(f_{VCO2} - 3f_{TRI})$, and the unwanted spurs at $(f_{VCO2} - f_{TRI})$ and $(f_{VCO2} + 3f_{TRI})$ are also filtered out by the RC low pass filter. If $\mathrm{M}_{11} - \mathrm{M}_{14}$ is modeled as ideal switches, the conversion gain (G_{Mixer}) of the third harmonic mixer can be derived as

$$\begin{aligned} G_{Mixer} &\approx \frac{2}{\pi}\frac{A_1}{A_{VCO}} R_2 \\ &= \frac{1}{\pi}\left(\mu_n C_{ox}\frac{W}{L}\right)_{5-8} \left(\mu_n C_{ox}\frac{W}{L}\right)_{9-10} A_{TRI}^2 R_L R_2. \end{aligned} \tag{26}$$

If

$$R_L \approx \frac{1}{g_{m9-10}} = \frac{1}{V_{ov9-10}\left(\mu_n C_{ox}\frac{W}{L}\right)_{9-10}}. \tag{27}$$

Combing (26) and (27), we have

$$G_{mixer} \propto \left(\mu_n C_{ox}\frac{W}{L}\right)_{5-8} \frac{1}{V_{ov,9-10}} A_{TRI}^2 R_2. \tag{28}$$

According to (28), G_{Mixer} can be enhanced by increasing A_{TRI} and decreasing the overdrive voltage of M_9 and M_{10}, which leads to a higher nonlinearity of the single transistor mixer. With on chip VCO amplitude of about 100 mV and tripler output amplitude of about 250 mV, the simulated conversion gain of the third harmonic mixer is about -28 dB.

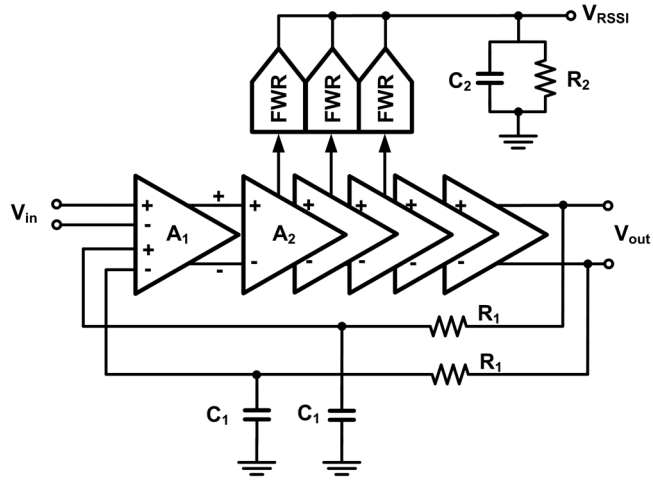


Fig. 9. Post-amplifier schematic.

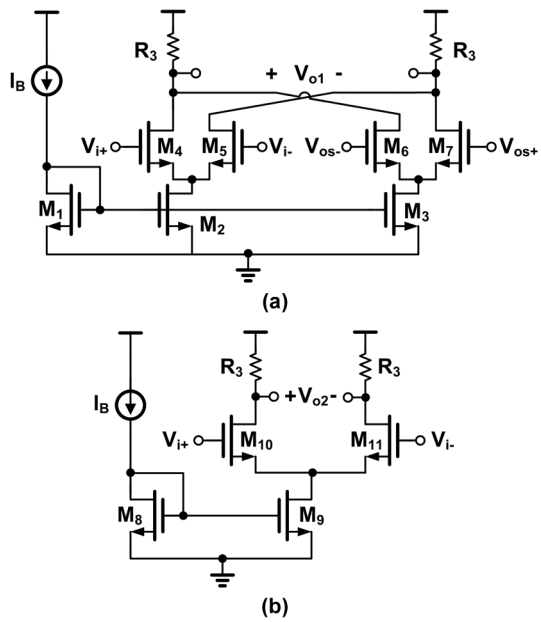


Fig. 10. (a) Offset-cancellation amplifier (b) gain cell.

D. Post-Amplifier and RSSI

Fig. 9 shows the post-amplifier architecture. It is composed of an offset cancellation input stage (A_1) followed by five identical gain cells (A_2) and an $(\mathrm{R}_1, \mathrm{C}_1)$ low pass filter for offset extraction. The offset cancellation stage and the gain cells are basically common source amplifiers, as are shown in Fig. 10(a) and Fig. 10(b) respectively. The post amplifier provides a DC gain of 60 dB, and -3 dB bandwidth of about 1 GHz $(\sim\ Mf_{REF})$. If f_{IF} falls within the -3 dB bandwidth of the post amplifier, it would be enlarged to be higher than 324 mVpp to drive the divider for phase and frequency comparison.

The post amplifier output is connected to a full wave rectifier to perform as received signal strength indicator (RSSI). Fig. 11 shows the detailed circuit schematic. The output voltage is con-

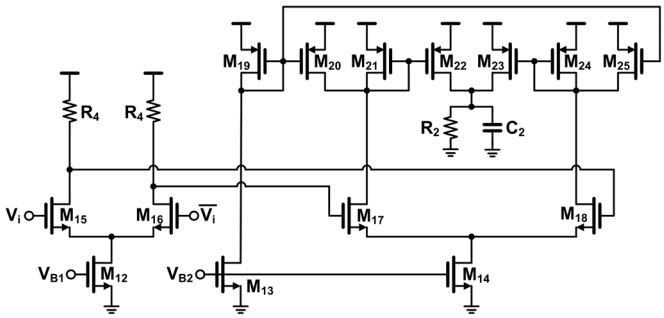


Fig. 11. Full wave rectifier for RSSI.

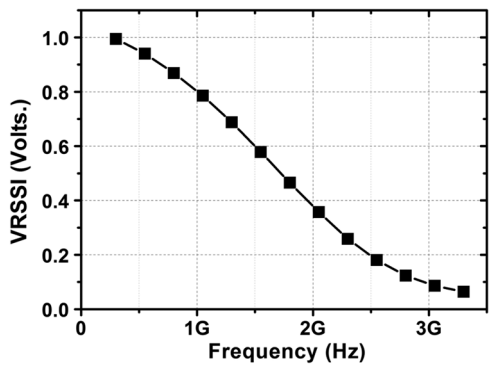


Fig. 12. Simulated frequency dependent output voltage characteristic of RSSI.

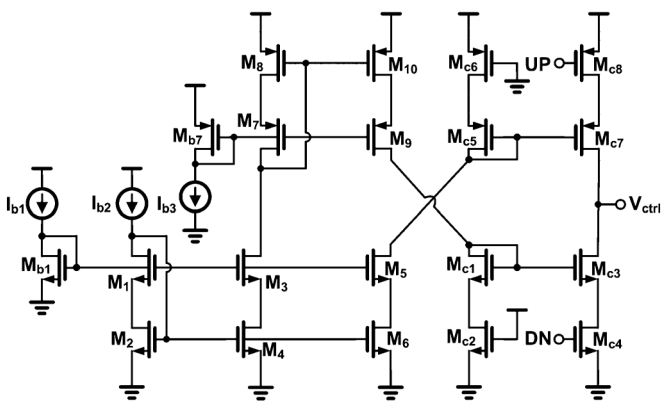


Fig. 13. Charge pump schematic.

verted to current form by M_{17} and M_{18}, and rectified through current mirrors $(\mathrm{M}_{21}-\mathrm{M}_{22})$ and $(\mathrm{M}_{23}-\mathrm{M}_{24})$. The RSSI manifests pseudo linear frequency dependent transfer characteristic, as is shown in Fig. 12. It fully covers the tuning range of the VCO to assist frequency pull-in process.

At the onset of frequency lock-in process, the VCO is preset to its highest frequency, leading to a smaller output at the RSSI. The VCO frequency is then pulled down gradually by a resistor-ladder DAC, which is controlled by the RSSI. As RSSI exceeds the threshold level, the post amplifier output is large enough to make the succeeding dividers function properly. The PLL will resume its close loop operation for frequency locked and phase tracking.

E. Charge Pump

Fig. 13 shows the charge pump circuit. To alleviate reference spurs induced by current mismatch, wide swing cascode current

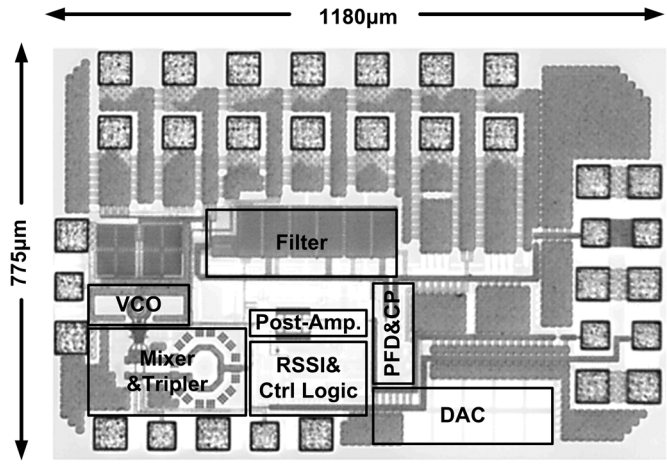


Fig. 14. Chip photograph.

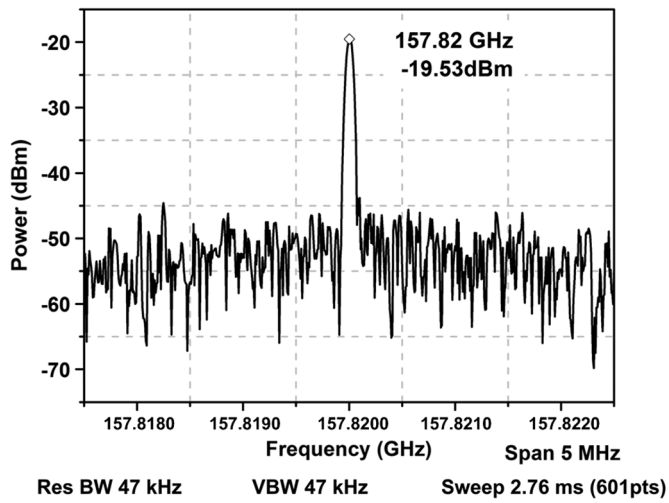


Fig. 15. Measured PLL output spectrum at 157.82 GHz with $f_{REF} = 130$ MHz.

mirrors are adopted to copy the up and down currents. Here M_{c2} and M_{c6} are replicas of M_{c4} and M_{c8}.

V. Experimeantal Results

A 160 GHz frequency-translation PLL has been fabricated using TSMC 65 nm CMOS process, and is powered under a 1.2 V supply. The total power dissipation is about 24 mW and the chip size is about 775 μm $\times$ 1180 μm, excluding the frequency multiplier. The chip photo is shown in Fig. 14. The chip performance is measured using probe station. The VCO output frequency is down converted by an external harmonic mixer (OML M05HWD) and measured by frequency spectrum analyzer (Agilent E4448A). With a reference frequency (f_{REF}) of 130 MHz, f_M at 17.42 GHz $(\mathrm{N} = 134)$, and $\mathrm{M} = 8$, the measured output spectrum is shown in Fig. 15. By taking the insertion loss (~ -55 dB) of external mixer and cable into account, the output power of VCO is -19 dBm. The measured locking time using signal source analyzer (Agilent E5052A) is less than 3 μs by the proposed frequency acquisition scheme, as is shown in Fig. 16.

Due to the limitation of in house instruments, the VCO phase noise performance is indirectly measured at the post amplifier

TABLE I
PERFORMANCE BENCHMARK

Reference	[7]	[16]	[17]	This work
Technology	65nm CMOS	0.13μm SiGe BiCMOS	InP HBT	65nm CMOS
f_{out}(GHz)	104	95	300	158
Locking Range (GHz)	1.5	7.5	0.36	2.8
Prescaler	ILFD	Miller Divider	Miller Divider	Harmonic Mixer + RSSI Frequency Sweeping
P_{out} (dBm)	-23	3	-23	-19
Phase noise	-80.4 dBc/Hz @ 1MHz offset	-102 dBc/Hz @1MHz offset	-85 dBc/Hz @ 1 MHz offset	-85 dBc/Hz @ 1MHz offset
Power Dissipation	63 mW	570 mW	301.6 mW	24 mW (w/o frequency multiplier)
Chip size	1.1x0.76 mm^2	1.1x1.1 mm^2	0.84 mm^2	1.2x0.8 mm^2 (w/o frequency multiplier)

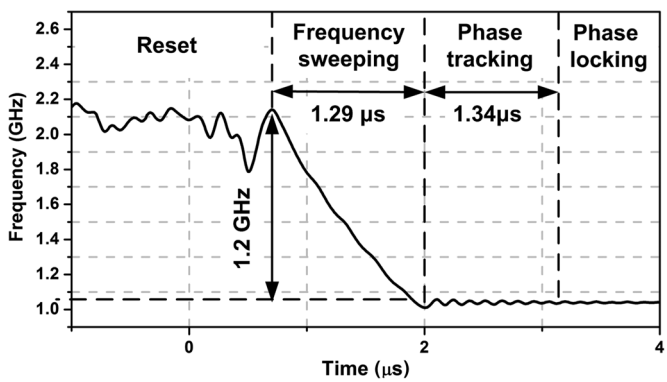


Fig. 16. Measured PLL settling behavior at f_{IF2} (For f_{VCO} hopping from 158.92 GHz to 157.82 GHz, f_{IF2} changes from 2.14 GHz to 1.04 GHz).

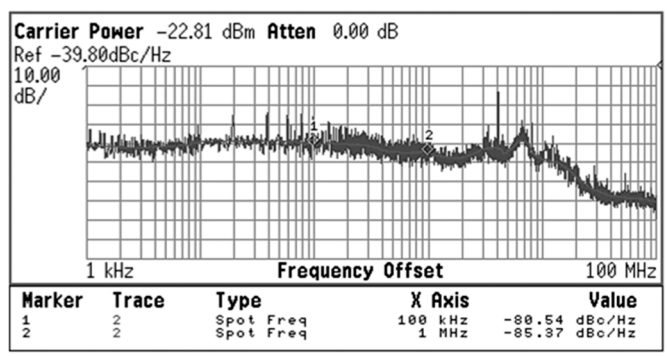


Fig. 17. Measured phase noise performance at f_{IF2}.

output (f_{IF2}). Fig. 17 shows the measured phase noise performance. According to the previous discussions in Section III, the phase noise performance at amplifier output $(\phi_{n,IF2})$ can be modeled as

$$\overline{\phi^2_{n,IF2}} = \overline{\phi^2_{n,VCO}} + \overline{\phi^2_{n,excess}}. \quad (29)$$

By taking the noise contribution of $\phi_{n,excess}$ into account, the VCO phase noise is expected to be better than -85 dBc/Hz at 1 MHz offset.

Table I summaries the performance benchmark. It can be seen that the resonator based divider (ILFD/Miller) are facing severe design challenges as operating frequency beyond 100 GHz. Taking the estimated power of auxiliary PLL into account [15], the proposed FT-PLL architecture still manifests superiority in low power consumption by circumventing 1/9 millimeter wave prescaler. Additionally, by RSSI assisted automatic frequency sweeping, it can achieve reliable operation without external tuning.

VI. CONCLUSION

This paper proposes a novel frequency-translation PLL for sub-THz systems. High frequency prescaler in the PLL is replaced by a 3rd harmonic mixer for frequency down conversion. In contrast to conventional PLL with cascaded ILFDs as prescaler, it is free of frequency misalignment problems with the aid of RSSI for automatic frequency sweeping. Finally, a 160 GHz fundamental mode PLL with agile locking speed is demonstrated using TSMC 65 nm CMOS process.

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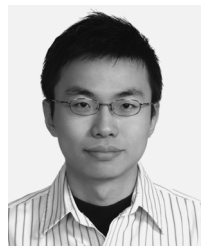

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