Ambipolar $MoTe_2$ Transistors and Their Applications in Logic Circuits

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The advent of graphene, a two-dimensional (2D) material, extracted from graphite using scotch tape-based mechanical cleavage, has triggered much attention because of its peculiar electrical, optical, and mechanical properties in nature, opening up a new area for both fundamental science and technological communities.[1] However, the absence of an intrinsic bandgap in graphene has hindered its development for use in logic circuits in the modern semiconductor industry, stimulating scientific and engineering progress on its derivatives and other 2D layered nanomaterials.[2–7] Transition-metal dichalcogenides (TMDs) with the common formula MX_2, where M stands for a transition metal from group IV-VII (M = Mo, W, Nb, Re, and so on) and X is a chalcogen element (S, Se, Te), form a well-known class of layered composite materials. In these layered materials, a hexagonally packed layer of M atoms is sandwiched between two layers of X atoms, and the triple layers stack together via weak van der Waals forces, which facilitate cleavage of the bulk crystals to form individual 2D flakes along each triplet of layered structures. The lack of covalent bonds between adjacent triple layers renders these 2D TMD flakes free of dangling bonds, thus creating chemical stability and low carrier scattering on their surfaces. These layered TMD structures lead to high anisotropy in their electrical properties.[8] The earliest use of TMDs in field-effect transistors was reported in 2004, where bulk WSe_2 crystals exhibited ambipolar behavior with mobilities as high as 500 $cm^2\ V^{-1}\ s^{-1}$ and a current modulation of up to 10^4.[9] The electrical properties of several TMDs with ultra-thin layers have been studied including those of MoS_2, $MoSe_2$, WS_2, and WSe_2 flakes, revealing superior transistor performance in comparison to those made of graphene.[10–14] As a result, 2D TMDs are regarded as promising materials for the development of non-graphene optoelectronics.

2H-type molybdenum ditelluride ($MoTe_2$) is a TMD layered compound. In its bulk form, $MoTe_2$ is a semiconductor with an indirect bandgap of 1.0 eV[3] and has been exploited as an electrode material in photovoltaic cells because of its strong absorption properties throughout the solar spectrum.[15] Other distinctive properties have also been addressed in bulk $MoTe_2$. Its mobility at room temperature (RT), for example, can theoretically reach up to 200 $cm^2\ V^{-1}\ s^{-1}$.[16] Both p- and n-type materials were synthesized through controlling the growth conditions in $MoTe_2$ crystals, leading to their use in light-emitting transistors (p–n junctions).[17] In addition, a phase transition was observed between the semiconducting α-$MoTe_2$ and the metallic β-$MoTe_2$ because of distortion of the octahedral coordinates.[18] Moreover, calculations have shown that $MoTe_2$ exhibits a direct bandgap of 1.07 eV because of the induced quantum confinement when the layer is thinned to a monolayer.[19] Recently, semiconducting $MoTe_2$ nanorods were fabricated by annealing $MoTe_2$ particles in solution.[20] The mechanical properties of the single-walled $MoTe_2$ nanotubes were found to strongly depend on the diameter and chirality of the tubes.[21] Although the electrical properties of bulk $MoTe_2$ have been studied,[8,16,22–25] layered $MoTe_2$ flake structures have not been investigated thus far and are still puzzling.

In order for digital and analog applications to be realized, silicon-based complementary metal-oxide-semiconductor (CMOS) electronics, where unipolar n- and p-type transistors are predetermined through deliberate stoichiometric variations during the fabrication process and are integrated together to build logic circuits, have been part of the most efficient strategy until now. However, as the number of transistors per circuit increases, the transistor channels have to be spatially separated to prevent leakage currents. Thus, the fabrication of circuits becomes more complex and the cost of mass production is more expensive as a result. In contrast, the use of ambipolar-based transistors, characterized by a superposition of electrons and holes, might be used as an alternative scenario in simplifying circuit

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design. Transistors that display charge-carrier ambipolarity can easily be switched because of the simultaneous or selective transport of electrons and holes in the conducting channel by applying an electric field.[26] Very recently, with the use of an electrolyte gate, ambipolar charge transport has been shown in 2D TMD flakes, providing an opportunity for future applicability in both the digital and analog domains.[12,27–29]

In this communication, we determine, for the first time, the electrical characteristics in layered flakes (2–4 layers) of α-$MoTe_2$ that were mechanically exfoliated onto Si/SiO_2 substrates. The $MoTe_2$ transistors unambiguously displayed ambipolar charge-transport behavior. The performance of the ambipolar-transistor operation under a drain-source voltage (V_{ds}) of 10 V at RT was characterized with a current on/off ratio of 5×10^2 and 2×10^3 for the electron and hole accumulation regimes, respectively. Through extensive analysis of the temperature dependence of the current–voltage (I_{ds}–V_{ds}) curves in the layered $MoTe_2$ transistors, the ambipolar charge transport can be exactly described on the basis of charge transport across a Schottky barrier at the metal–$MoTe_2$ contact. The existence of a Schottky barrier at the contact can be modulated by the addition of an electrostatic field from the back-gate voltage (V_{bg}) and the drain-source voltage (V_{ds}), allowing the $MoTe_2$ flakes to exhibit ambipolar charge transport with a low contact resistance for both n- and p-type conduction. Comprehensive mapping of the effective Schottky barrier heights as a function of V_{bg} and V_{ds} is further unveiled and offers insight into understanding the carrier-injection mechanism, as well as the controlling current on/off ratio in $MoTe_2$ flakes. More excitingly, these ambipolar layered $MoTe_2$ transistors enabled us to achieve complementary inverters and output polarity controllable (OPC) amplifiers based on a single active material.

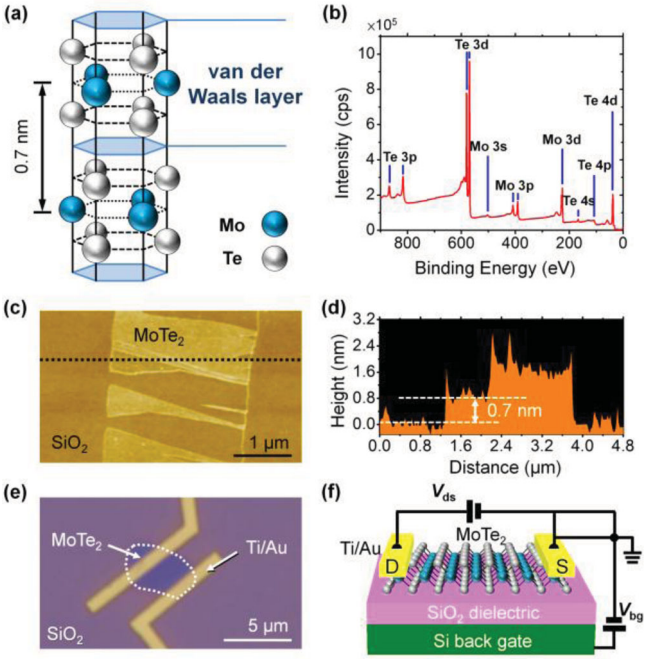

Figure 1. a) The crystal structure of 2H-type α-$MoTe_2$. Each layer has a thickness of 0.7 nm. b) XPS spectrum of as-synthesized $MoTe_2$ crystals. c) AFM image of a $MoTe_2$ flake deposited on top of a silicon substrate with a 285-nm thick SiO_2 layer. d) The cross-sectional profile along the dotted line of the AFM image shown in (c). e) Optical image of a pair of Ti/Au electrodes deposited on a layered $MoTe_2$ flake. f) Scheme of a $MoTe_2$ transistor used for this study, with the circuit diagram overlaid. The heavily doped Si substrate was used as the back gate. The electrode on one side served as the drain (D), whereas the other was the source (S).

The crystal structure of the 2H-type α-$MoTe_2$ layer compound is shown in **Figure 1**a, where the stacking layers follow the sequence of Te-Mo-Te, Te-Mo-Te. Each layer has a thickness of 0.7 nm, in which the Mo atom is covalently bound to six neighboring Te atoms in a trigonal prismatic coordination.[30] The XPS spectrum for the as-synthesized bulk crystals used in the study is displayed in Figure 1b. Only Mo and Te core electron peaks are observed, indicating that the growth of $MoTe_2$ crystals was successful. Figure 1c shows an AFM image of a $MoTe_2$ flake transferred onto a Si/SiO_2 substrate. From the line profile of the AFM image the thickness of the flake could be estimated to be about 0.7 nm, which is in conformity with the height of a monolayer of $MoTe_2$ (see Figure 1d). *This result is the first experimental evidence proving that a monolayer of $MoTe_2$ can be stable at RT in air.* The flakes that we obtained were triangular, with most of them showing irregularities (Figure S3, Supporting Information). In this study, we used $MoTe_2$ flakes with thicknesses ranging from 2 to 4 layers rather than monolayer $MoTe_2$ flakes, because we were unable to cleave the $MoTe_2$ crystals down to atomic flakes with a large enough lateral size for device fabrication. It should be noted that within the investigated thickness range of the $MoTe_2$ flakes, the transistor characteristics were not found to be remarkably thickness dependent. An optical image of a typical $MoTe_2$ transistor (bilayer) is displayed in Figure 1e. For all of the layered $MoTe_2$ transistors, the channel length-to-width ratio was purposely kept constant at around 1 to reduce device–device variations. Figure 1f illustrates a sketch of the $MoTe_2$ transistor configuration along with the circuit measurements used.

The room-temperature (RT) transfer characteristics of a trilayered $MoTe_2$ transistor under different V_{ds} values are shown on the linear scale in **Figure 2**a and on the logarithmic scale in Figure 2b. An abrupt increase in I_{ds} is clearly observed with increasing V_{bg} for both positive (n-channel) and negative (p-channel) polarities, which demonstrates the ambipolar operation in the $MoTe_2$ flake transistors. Moreover, no significant hysteresis is observed in the transfer characteristics of the $MoTe_2$ flake transistors when the back-gate voltage is scanned at the fixed speed of 4 V s^{-1} used in our study (Figure S4, Supporting Information), implying that defect and trap contributions can be ignored. Under modulation of V_{bg} the current on/off ratio at V_{ds} = 10 V reaches 5×10^2 and 2×10^3 for the n- and p-type regimes, respectively, fulfilling the requirements for use as a switch.[31] For simplicity, the contribution of the contact resistance was ignored when estimating the mobilities. According to the conventional equation $\mu = (L/W)(d/\varepsilon_0\varepsilon_r V_{ds})(\Delta I_{ds}/\Delta V_{bg})$, where μ is the field-effect mobility, L/W is the channel length-to-width ratio and is 1 for this study, ε_0 is the permittivity in vacuum, ε_r is 3.9 for SiO_2, and d is the thickness of the dielectric layer (285 nm),[32] we obtained mobilities of 0.03 and 0.30 cm^2 V^{-1} s^{-1}, extracted at V_{ds} = 10 V in the high V_{bg} region, for electrons and holes, respectively. Both mobilities were much lower than the theoretical prediction in the literature,[16] implying the existence of a large contact resistance in the layered $MoTe_2$ transistors.

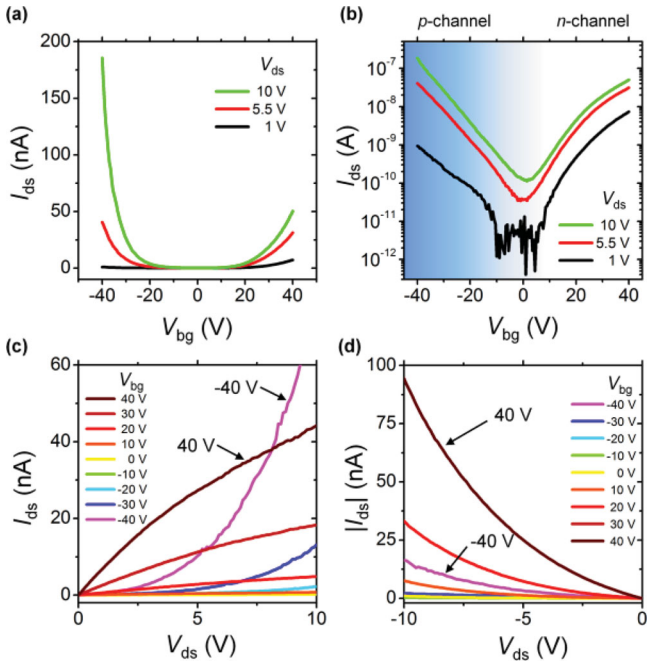

Figure 2. RT transfer characteristics of a tri-layered $MoTe_2$ transistor under different V_{ds} values on a linear scale (a) and on a logarithmic scale (b). RT output characteristics of the $MoTe_2$ transistor under different V_{bg} values in the positive V_{ds} regime (c) and in the negative V_{ds} regime (d).

Figure 2c and d reveal the RT output characteristics of the $MoTe_2$ transistor at different V_{bg} values in the positive and negative V_{ds} regimes, respectively. When sweeping V_{ds} from 0 to 10 V, a saturation of the current is detected at V_{bg} = 40 V, as shown in Figure 2c. This is caused by the occurrence of pinch-off in the channel. With a decreasing V_{bg} from 40 to 0 V at a given V_{ds}, the magnitude of I_{ds} decreases. This demonstrates that electrons are the majority of the charge carriers in the positive V_{bg} regime. However, when varying V_{bg} from 0 to –40 V, the I_{ds} shows typical behavior, namely it increases at a given V_{ds}. Such a unique increase, which is not present in unipolar transistors, can be attributed to the accumulation of holes in the conducting channel and is a typical ambipolar feature. When V_{ds} is scanned from 0 to –10 V, we observe a nonlinear increase in $|I_{ds}|$ (Figure 2d), suggesting that there is a significant contact resistance suppressing the carrier injection as well as the transistor appearance in the channel. With a decrease in the negative V_{bg} the $|I_{ds}|$ value gradually decreases, which means that holes are dominant in the negative V_{bg} regime. The electron current (ca. 95 nA at V_{bg} = 40 V and V_{ds} = –10 V) was twice as large as the hole current (ca. 45 nA at V_{bg} = –40 V and V_{ds} = –10 V), confirming that the type of carrier that formed the majority in the inversion layer was not as obvious as seen in Figure 2c. Unlike graphene transistors, evidence of both a high current on/off ratio and current saturation over a wide V_{ds} window points to the presence of a bandgap in the $MoTe_2$ flakes, showing that these flakes can contribute to broadening the scope of logic design.

To verify our conjecture on the existence of contact barriers and to elucidate the charge-transport mechanism for the ambipolar operation in $MoTe_2$ transistors, temperature-dependent measurements were carried out. **Figure 3**a and b unveil the temperature dependence of the transfer and output characteristics, respectively, for the $MoTe_2$ transistor shown in Figure 2. In Figure 3a, it can be seen that the minimum voltage required to achieve the on-current state (threshold voltage, V_{th}) shifts toward the more positive or negative V_{bg} region, when the temperature decreases from 300 down to 100 K. The blue dashed lines in Figure 3a are a guide to the eye for the shift in V_{th}. This behavior is can be explained by the decreasing number of charge carriers in the conducting channel. The current on/off ratio was derived as 5×10^2 (2×10^3) at 300 K, approaching a saturation value of 10^4 (10^5) at 220 K at V_{ds} = 10 V for the n- (p-) channel region (Figure S5, Supporting Information). In Figure 3b, the I_{ds} increases for a fixed temperature with increasing V_{ds}, revealing a downward (upward) bending characteristic in the positive (negative) V_{ds} region. Such asymmetric I_{ds}–V_{ds} behavior is strongly associated with the contact resistance, which arises from contact barriers with different potential heights, taking place at the source/$MoTe_2$ and drain/$MoTe_2$ interfaces. With decreasing temperature, the value of I_{ds} gradually drops for a given V_{ds}.

If we consider the semiconducting nature of $MoTe_2$, the circuit configuration of the $MoTe_2$ transistors can be treated as a metal–semiconductor–metal (M–S–M) structure, where the Schottky barriers are constructed at both metal/semiconductor contacts. To verify the relationship between the experimental data and the model of thermionic emission for the Schottky contacts,[33] an Arrhenius plot of the $MoTe_2$ transistor as a function of V_{bg} (p-channel) is shown in Figure 3c. From this figure, the contribution of both the thermionic emission and tunneling components can be clearly differentiated. Similar results are obtained for an n-channel as well. This manifests that Schottky barriers are formed at both the source/$MoTe_2$ and drain/$MoTe_2$ interfaces, giving rise to the contact resistance. Through analysis of the slopes of the linear fits in the $\ln(I_{ds})$–$1/T$ plot at high temperatures, the effective Schottky barrier, ϕ_{eff}, could be obtained (see Section V of the Supporting Information for more details). The extracted ϕ_{eff} at V_{ds} = 10 V shows a strong dependence on V_{bg}, as it shrinks from 0.13 to 0.08 eV as V_{bg} is increased from –10 to –40 V.

To gain further insight into the underlying mechanism of the ambipolar behavior in the layered $MoTe_2$ transistors, the magnitudes of the effective Schottky barrier heights were mapped as a function of V_{ds} and V_{bg} and are presented in Figure 3d. The dotted and dashed white lines refer to the positions of V_{ds} = 0 V and V_{bg} = 0 V, respectively, which equally divide Figure 3d into four quadrants so as to highlight the energy-band bending in the $MoTe_2$ transistors under different electrostatic fields. Taking into account the M–S–M structure, the band model of two back-to-back Schottky barriers was adopted,[34] as shown in Figure 3d. As V_{bg} is swept between –40 to 40 V, the transistor undergoes a transition from the p- to the n-type regime. With a positive V_{bg}, the conduction and valence bands are bent downward, making it easier to inject electrons from the source (drain) to the drain (source) at a given positive (negative) V_{ds}, thus establishing n-type conduction. Parts (I) and (IV) in Figure 3d show a concept of the energy-band diagram. With a negative V_{bg}, the conduction and valence bands are bent upward driving holes from the drain (source) to the source (drain) at a given

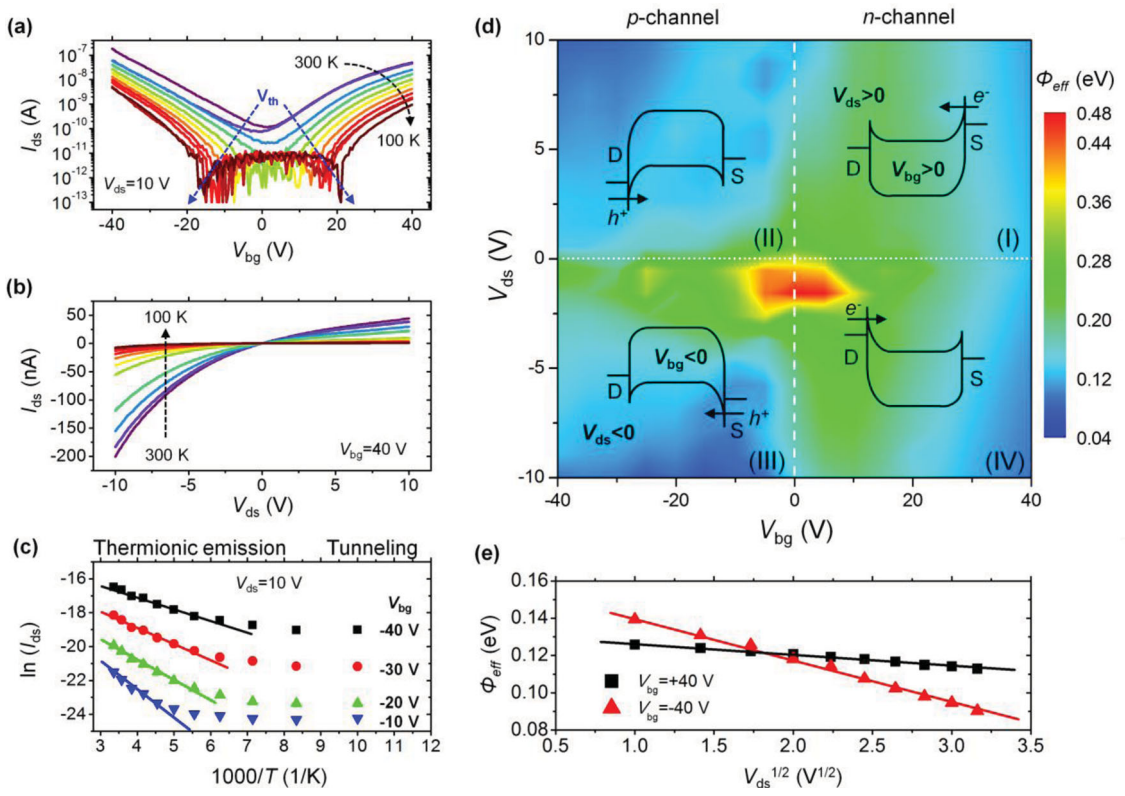

Figure 3. a) Transfer characteristics of the $MoTe_2$ transistor at V_{ds} = 10 V as a function of temperature. b) Output characteristics of the $MoTe_2$ transistor at V_{bg} = 40 V as a function of temperature. c) Arrhenius plot at V_{ds} = 10 V with V_{bg} varying from –40 to –10 V (p-channel). d) Maps of effective Schottky barrier heights, ϕ_{eff}, as a function of V_{ds} and V_{bg} for the $MoTe_2$ transistors. The dotted and dashed white lines denote the positions of V_{ds} = 0 V and V_{bg} = 0 V, respectively. Energy-band bending diagrams for the $MoTe_2$ transistor operated under V_{ds}> 0 and V_{bg} > 0 (I), V_{ds} > 0 and V_{bg} < 0 (II), V_{ds} < 0 and V_{bg} < 0 (III), and V_{ds} < 0 and V_{bg} > 0 (IV) are drawn to illustrate the electron and hole injections and the ambipolar charge-transport behavior. d) ϕ_{eff} as a function of the square root of V_{ds} at V_{bg} = 40 V (n-channel) and –40 V (p-channel).

positive (negative) V_{ds}. This idea is shown in parts (II) and (III) in the p-channel regime. Close inspection of the effective barrier heights shows that a small ϕ_{eff} can be gained at a high V_{ds} or V_{bg}. In other words, when both V_{ds} and V_{bg} gradually approach 0 V, a maximum ϕ_{eff} of 0.48 eV occurs, as depicted in Figure 3d. As the variations in I_{ds} are roughly symmetric with respect to V_{bg} (see Figure 2b), the maximum effective barrier height is expected to be half that of the $MoTe_2$ bandgap ($\phi_{max} \sim E_g / 2$).[35] Hence an experimental value for E_g of 0.96 eV can be obtained, which is in excellent agreement with the previously published value of 1.0 eV.[3] In addition, the fact that the deduced mobility for electrons is lower than that for holes can also be explained by the existence of a higher ϕ_{eff} in the n-type regime. Interestingly, the ϕ_{eff} obeys a linear dependence on the square root of V_{ds} (see Figure 3e), which signifies a large electrostatic field from the V_{ds} at the contacts, leading to an image force lowering of the Schottky barrier.[33]

From these above-mentioned results, we can summarize that the thermionic emission of the Schottky contacts dominates the charge transport in the layered $MoTe_2$ transistors and the ambipolar characteristics are responsible for the tunability of the Schottky barrier heights and the contact resistance, rather than the channel conductance. We speculate that the formation of two back-to-back Schottky barriers possibly stems from the energy difference between the metal work function and the $MoTe_2$ electron affinity energy.[36] For transistors with Ti contacts (Ti work function is ca. 4.33 eV), relatively equal barrier heights for electrons and holes are established, allowing ambipolar charge transport. The conjecture suggests that using a metal with a lower (or higher) work function for the contacts may *engineer* $MoTe_2$ transistors to behave in a unipolar n- (p-) type manner. This type of unipolar transistor has been preliminarily realized and is shown in Figure S6 in the Supporting Information. Further discussion about charge injection via different contact metals is still needed in the near future. An unusual two-Schottky-barrier-type transistor has been demonstrated in the layered $MoTe_2$ flakes. Complete mapping of the effective barrier heights will pave a way to develop new electronic functions in 2D TMD electronics.

Despite the fact that transistors with two back-to-back Schottky barriers arising from the contacts are considered to be undesirable because they cause additional energy to dissipate, leading to poor device performance and low mobilities, in the following discussion we demonstrate that the ambipolarity caused by these Schottky barriers in the $MoTe_2$ transistors should not be seen as a drawback but can be beneficial in realizing logic applications.

As proof of concept, we fabricated a complementary inverter, which is the basic building block in logic architectures, by assembling two layered $MoTe_2$ transistors (bilayer) with a

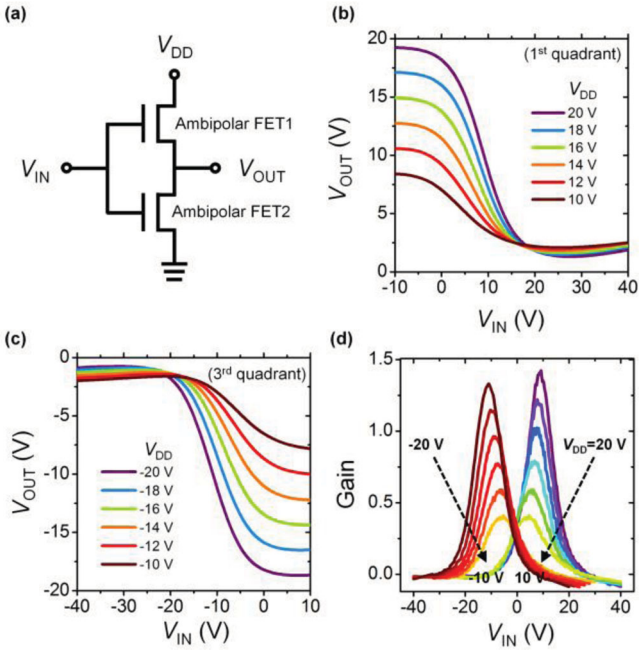

Figure 4. a) Scheme of a complementary inverter circuit comprising two ambipolar transistors, one of which operated as an n-type channel transistor whereas the other was conducted as a p-type channel transistor. b) Inverter characteristics where V_{IN} and V_{DD} were both positively biased (1st quadrant). c) Inverter characteristics where V_{IN} and V_{DD} were both negatively biased (3rd quadrant). d) The corresponding voltage gain of the complementary inverter ($-\Delta V_{OUT}/\Delta V_{IN}$).

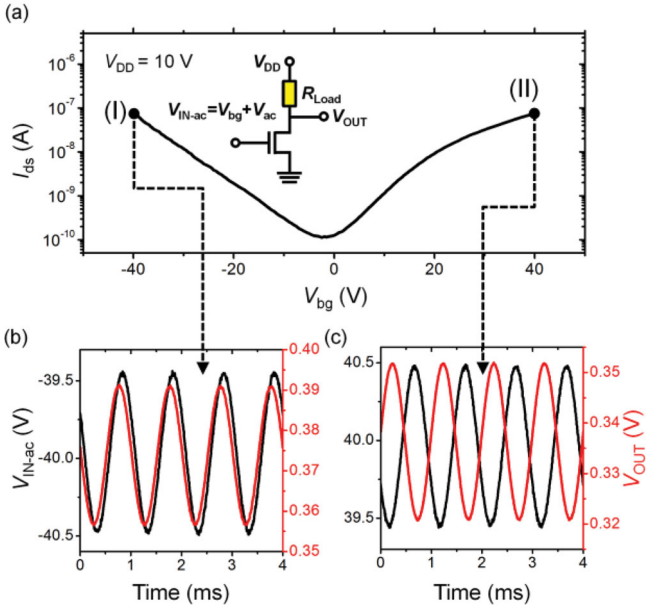

Figure 5. a) RT transfer characteristics of a layered $MoTe_2$ transistor. The inset depicts the scheme of an OPC amplifier circuit equipped with an off-chip resistor R_{Load}. The two dots represent the difference in the operation modes. From the left side to the right side, the OPC amplifier is manipulated in the common-drain mode (I) and the common-source mode (II). b) In the common-drain mode, the output signal shows the same phase as the input signal. c) In the common-source mode, the output signal displays a 180° phase shift when compared to the input signal.

common gate as the input voltage, V_{IN}. The circuit diagram for the inverter is depicted in **Figure 4**a, where the supply voltage and output voltage are labeled as V_{DD} and V_{OUT}, respectively. When a positive V_{DD} and V_{IN} are applied, the inverter works in the positive V_{OUT} regime (1st quadrant), as shown in Figure 4b. Under these circumstances, the ambipolar transistor, FET1 in Figure 4a, operates as a p-type channel, whereas the FET2 conducts as an n-type channel. As V_{DD} and V_{IN} are applied negatively *without any alternation of the circuit formation*, the inverter works in the negative V_{OUT} regime (3rd quadrant), as shown in Figure 4c. Here, the ambipolar transistors, FET1 and FET2, are functioned to the n- and p-type regimes, respectively. Depending on the polarities of V_{DD} and V_{IN}, the inverter can work in either the 1st or 3rd quadrant, which is a unique characteristic of ambipolar-based inverters. The corresponding voltage gains, defined as $-\Delta V_{OUT}/\Delta V_{IN}$, at various V_{DD} are displayed in Figure 4d as a function of V_{IN}. With decreasing $|V_{DD}|$ the voltage gain is reduced. It is worth noting that the peak position of the gain (inverting voltage) is close to $V_{DD}/2$, which reflects that there is no significant difference between the electron and hole contributions in the two ambipolar transistors used in the inverter demonstration.

Transistors displaying ambipolar behavior have flexibilities for use in communication applications over conventional routines. Ambipolar transistors could much simplify circuit designs and improve signal processing performance. Here we use another layered $MoTe_2$ transistor (bilayer) with balanced electron and hole characteristics to demonstrate the two basic functions of analog circuits. The RT transfer curve for this $MoTe_2$ transistor is displayed in **Figure 5**a. The inset shows the scheme of an OPC amplifier circuit equipped with an off-chip resistor R_{Load}. The V_{DD} and R_{Load} were set to 10 V and 25 MΩ, respectively. A small sinusoidal signal V_{ac} was superimposed at a given constant V_{bg} and then applied to the back gate as a dynamic input signal ($V_{IN\text{-}ac} = V_{bg} + V_{ac}$). When a negative V_{bg} is applied to the OPC amplifier, in the positive phase of V_{ac}, I_{ds} increases/decreases as $V_{IN\text{-}ac}$ decreases/increases; and, as a consequence, the corresponding V_{OUT} also increases/decreases in an oscillatory manner. This situation is called the common-drain mode and is illustrated in Figure 5b. In this mode, V_{OUT} shows the same phase as $V_{IN\text{-}ac}$. Similarly, when V_{bg} is applied in the n-type regime, the corresponding V_{OUT} oscillates synchronously with a phase difference of 180° with respect to $V_{IN\text{-}ac}$, as shown in Figure 5c (the common-source mode). This demonstration of two fundamental modes in a *single*-layered $MoTe_2$ transistor has encouraged us to develop other complicated analog circuits such as phase-shift keying, frequency-shift keying, and RF mixers.

In conclusion, a layered compound structure of a semiconducting α-$MoTe_2$ crystal has been thinned down to atomic flakes and placed on Si/SiO_2 substrates by means of mechanical exfoliation before fabricating them into ambipolar transistors. Through deliberate analysis of the temperature dependence of the electrical properties, the ambipolarity of the charge transport in the layered $MoTe_2$ flakes was seen to occur because of the formation of two back-to-back Schottky barriers rather than through the channel conductance. An *in-depth* understanding

of the underlying mechanism of the carrier injection was uncovered by mapping the effective Schottky barrier heights as a function of V_{bg} and V_{ds}. By precisely controlling the electrostatic fields of V_{bg} and V_{ds}, the effective barrier height dramatically varied, and the current on/off ratio reached 5×10^2 and 2×10^3 for the electron and hole accumulation regimes, respectively. In addition, through extrapolation of the effective barrier height (at $V_{bg} = 0$ V and $V_{ds} = 0$ V), the bandgap of $MoTe_2$ was found to be 0.96 eV, which is consistent with the literature value, confirming the validity of this study. The tunability of these $MoTe_2$-based ambipolar transistors is suitable for use in logic and analog applications. Our findings provide an important avenue toward future fundamental studies as well as for the production of new atomic electronics with simpler and higher integration densities.

Experimental Section

Flakes made of a few layers of $MoTe_2$ were obtained by mechanical exfoliation of a semiconducting α-$MoTe_2$ bulk crystal grown by chemical vapor transport and then deposited on a heavily doped Si substrate covered with a 285-nm-thick SiO_2 dielectric layer. As-synthesized $MoTe_2$ bulk crystals were examined by X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (see Section I and Figure S2 of the Supporting Information for more details). Here the specific thickness of the SiO_2 layer was chosen to be able to optically visualize the contrast between the layers in the $MoTe_2$.[37] Flakes suitable for electrical characterization were identified by an optical microscope and the corresponding thicknesses were accurately inspected by atomic force microscopy (AFM). After characterization, a pair of electrical contacts was patterned on top of the selected flakes using standard electron-beam lithography, followed by thermal evaporation of a Ti/Au film (5/50 nm thick). To acquire the temperature-dependent evolution, the as-fabricated $MoTe_2$ transistors were mounted into an insert cryostat. The temperature was set using a temperature controller (Cryogenic Control Systems model 32) in the range of 300 to 100 K. The quasi-static measurements of the layered $MoTe_2$ transistors were carried out using an Agilent 4156C semiconductor parameter analyzer, whereas the dynamic characterizations were performed by combining a Hewlett-Packard 3245A signal generator and a Keithley 2400 power supply. The radio-frequency (RF) response was monitored using an Agilent 54830B digital oscilloscope.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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