Practical Routability-Driven Design Flow for Multilayer Power Networks Using Aluminum-Pad Layer

Wen-Hsiang Chang, Mango C.-T. Chao, and Shi-Hao Chen

***Abstract*— This paper presents a novel framework to efficiently and effectively build a robust but routing-friendly multilayer power network under the IR-drop and electro-migration (EM) constraints. The proposed framework first considers the impact of the aluminum-pad layer and provides a conservative analytical model to determine the total metal width for each power layer that can meet the IR-drop and EM constraints. Then the proposed framework can identify an optimal irredundant stripe width by considering the number of occupied routing tracks and the potential routing detour caused by the power stripes without the information of cell placement. Next, after the cell placement is done, the proposed framework applies a dynamic-programming approach to further reduce the potential routing detour by relocating the power stripes. A series of experiments are conducted based on a 40 nm, 1.1 V, and 900-MHz microprocessor to validate the effectiveness and efficiency of the proposed framework.**

***Index Terms*— Electro-migration (EM), IR drop, power network, routing-driven.**

I. Introduction

In ADVANCED process technologies, the supply voltage is aggressively decreased to reduce the overall power consumption, which greatly reduces the noise margin of a chip's power supply [1]. Simultaneously, the current density of a same chip area significantly increases along with the scaling of the technology node and the faster switching frequency [2]. Therefore, more switching current flows in the power network, which may degrade the performance through the IR drop of the power network and the reliability through the metal wear-out caused by electro-migration (EM). To meet the IR-drop and EM constraints, significant routing resources need to be spent on the power networks, which directly impacts the routability of the underneath circuits and in turn delay the time of achieving the design closure. Thus, building a robust but routing-friendly power network under the IR-drop and EM constraints becomes a crucial task for advanced high-performance integrated circuits (ICs).

To explicitly analyze or simulate the worst case IR drop (or the current density) by considering a nonideal power network and all nonlinear devices, essentially, is computationally infeasible because of the huge number of the supplying devices and the power-grid size. In addition, the IR drop of the power network and the current load of devices are mutually interacted, which makes the convergence of the IR-drop analysis even slower. Therefore, a common practice to perform the IR-drop (or EM) analysis is firstly to estimate the current load of all devices under an assumed fixed IR drop and then simulate the IR-drop map for the power network based on that current estimation. Such an approximation can work reasonably accurate when the IR drop of the power network is only a small portion of the supply voltage, which is usually the case in practice.

By separating the estimation of the devices' current load from the power network's IR drop, the IR drop analysis can be successfully formulated as a linear system with a conductance matrix of the power grids along with a vector of voltage sources and a vector of current loads. This problem formulation is straightforward and simple, but finding an exact solution to this linear system is still much more complicated than this formulation looks as the size of the conductance matrix is N^4 for a $N \times N$ power mesh. Thus, several previous works applied different techniques, such as random walk [3]–[6] and hybrid solver [7], to perform the IR drop analysis without directly solving the entire conductance matrix, or attempted to reduce the problem size by finding the locality of the power network (for flip chips) [8], [9].

If the current loads are assumed to be uniform, several methods, such as mathematical programming [1], incomplete Cholesky conjugate gradient simulation-based methods [10], and wire sizing with closed-form IR-drop analysis [11], [12], can be applied to minimize the worst case IR drop based on a given total metal width and an approximate IR-drop estimation for uniform [11] or nonuniform [1], [10], [12] power networks. [13] further considers the impact of both resistive and inductive impedance while minimizing the worst case IR drop for a nonuniform power network. If the current load can be obtained after the placement, a sequential linear programming method [14] or incomplete Cholesky decomposition conjugate gradient method [15] can be applied to minimize the total metal width used in the power network. However, the worst-cast IR drop of a power network is often a design constraint in practice, rather than a factor to be optimized. In addition, all the above IR-drop minimization works relied on an approximate IR-drop estimation, and hence the resulting power network may still need to be further manually refined and verified by a more accurate

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IR-drop analyzer, which may result in multiple extra design iterations.

Instead of minimizing the IR drop under a given total metal width, the industrial practice tackles the IR-drop problem by properly setting a sufficient total metal width for the power network at the early design stage [16], which has to be conservative enough to limit the IR drop under a predefined constraint (usually less than 5% of the supply voltage) for a reasonably wide range of the current-load distribution. With such a design margin, the power-network design needs not be iteratively modified throughout the entire design flow and can achieve faster design closure. In addition, the IR-drop problem can be eased by utilizing a higher aluminum-pad (AP) layer with much lower sheet resistance to build the power network, which can greatly reduce the amount of the power network's metal required at the lower regular metal layers and save more routing resources for the routing of the underneath circuits.

References [2], [17], and [18] have discussed how to determine a sufficient total metal width for guaranteeing the IR drop of a power network. However, none of these have considered the impact of the AP layer in use, which can actually make the analysis easier. In addition, none have discussed how many percentages of the total metal should be allocated for each metal layer in a multilayer power network, which is usually the case in practice, and how this metal allocation as well as the layout configuration of the power stripes may affect the EM and the overall routability.

In this paper, we propose an efficient and effective framework to automatically build a routing-friendly multilayer power network for flip-chip designs. The proposed framework first uses an analytical model to determine the sufficient total metal width of each power metal layer for meeting the IR-drop and EM constraints while considering the impact of the AP layer. Second, based on the determined total metal width, the proposed framework can identify an optimal layout configuration for the power stripes by considering the total number of occupied routing tracks and the potential routing detour caused by the power stripes. Next, the proposed framework applies a dynamic-programming (DP) approach to relocate the power stripes based on the cell placement such that the routing detour can be further minimized. The reported experiments are conducted based on a 1.1 V, 900-MHz microprocessor implemented by a Taiwan Semiconductor Manufacturing Company (TSMC) 40-nm technology, and demonstrate that the power network generated by the proposed framework can effectively reduce the total wire length and the timing violations after detail routing. In addition, the worst case IR drop and EM of the resulting power network can both satisfy the predefined constraints, which are verified by a commercial power analysis tool, RedHawk [19]. The proposed framework is applied to several successful products in practice.

II. Background of Multilevel Power-Network Design

A. Overview of a Multilevel Power Network

Fig. 1 shows an exemplary multilevel power network based on a 8-metal-layer process, where VDD and GND are alternately placed and colored by the dark and light background, respectively. In this example, each of the VDD and GND networks is composed of four metal layers, including AP, M8, M7, and M2 layers. For conventional power-network designs, the power stripes on M8 and M7 (or the top two regular metal layers) are mutually crossed (the M8 stripes along the X-direction and the M7 stripes along the Y-direction) and often with the same total metal width. The power stripes on M7 connect to the power rails on M2 through vias. The power rails are placed on the same direction as the M8 power stripes (X-direction) and are actually the power lines of the standard cells. The vias are inserted within the overlapping area between each M7 power stripe and M2 power rail (as well as each M8 power stripe and M7 power stripe). Last, the metal on AP are added on the top and placed along the opposite direction of the M8 power stripes to reduce the overall IR drop with its low sheet resistance. In practice, most of the AP metal is used for the power network with the maximum metal width allowed by the design rule.

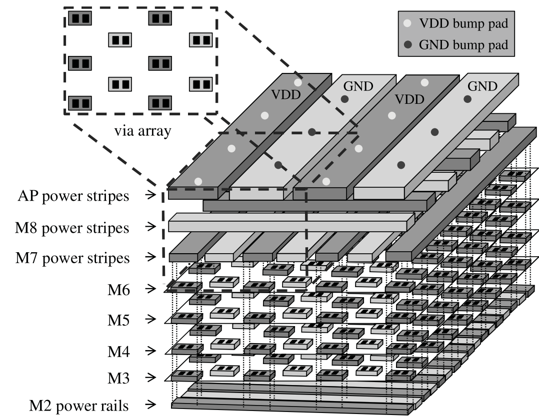

Fig. 1. Illustration of a multilayer power network.

Note that AP layer is originally designed for redistribution layer (RDL) routing in flip chips, where the pads (solder bumps) of power/ground and IO signals are directly attached to [20]–[22]. By using the AP layer and the top metal layer, the IO-signal pads are connected to the IO cell along the chip boundaries. Such RDL routing only consumes a small portion of the AP layer and hence the rest of the AP layer can also be used for the power-network routing. Because of its low sheet resistance, the AP layer can effectively reduce the IR drop of the power network, and thus even the wire-bond chips also use the AP layer for building the power networks [22].

B. IR-Drop Map After Using AP Layer

We first use the commercial tool, RedHawk [19], to perform an IR-drop analysis on a 1.1 V, 900-MHz microprocessor implemented by a TSMC 40-nm 8-metal technology, which contains a similar multilevel power network using the same four metal layers as shown in Fig. 1 (AP, M8, M7, and M2). Fig. 2 shows the corresponding IR-drop map of the VDD power network, i.e., the IR drop directly connecting to a cell on M2. As the result shows, the IR-drop difference along the X-direction of the VDD power network can be up to 8 mV

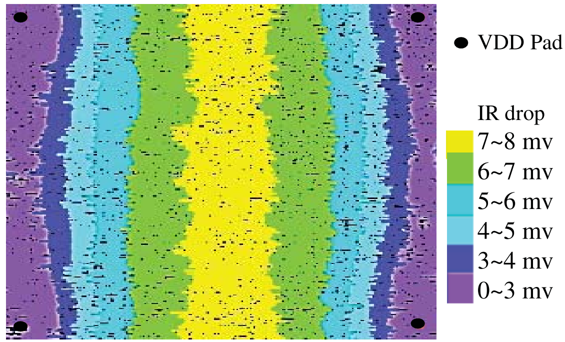

Fig. 2. IR-drop map for a power network with the AP layer.

while the IR-drop difference along the Y-direction is much more limited (less than 1 mV).

This phenomenon on IR drop results from the fact that once the AP layer is used to build the power network, the resistance on the Y-direction of the power network can be greatly reduced. Therefore, when targeting the worst case IR drop, we should focus on the total metal width along the X-direction, such as the M8 power stripes and the M2 power rails. The total metal width of M7 power stripes (also along the Y-direction) has almost no impact on the worst-case IR drop due to the use of the AP layer, which demonstrates that the conventional way of using the same metal width for M8 and M7 power stripes is not an efficient allocation of the routing resource. Note that a similar trend can be observed for the GND power network in this example, and hence the worst-case IR drop of the overall power network is around 16 mV.

C. Impact of Stripe Configuration on Routing

In most previous works about power-network designs, the total metal width used in each power layer is viewed as the index of the routing overhead of a power network. However, this index is only a rough approximation. In fact, the number of routing tracks occupied by the power stripes may vary significantly with respect to different layout configurations of the power stripes, even though the total metal width for each configuration is the same. Fig. 3 shows two layout configuration of power stripes, where a power stripe and a general interconnect wire are colored by red and green backgrounds, respectively, and a routing track is represented by a dashed line. w_{ps} denotes the width of a power stripe and $S(w_{\text{ps}})$ denotes the minimum spacing between the power stripe and its adjacent wire allowed by the design rules, which is actually a function of the stripe's width. RW denotes the width of an interconnect wire, which is a fixed value for a metal layer set in the APR tool and usually assigned to the minimum allowed width. P_{track} denotes the pitch between two routing tracks.

As Fig. 3 shows, both configurations occupy four routing tracks while the metal width shown in Fig. 3(a) is significantly smaller than that in Fig. 3(b), where the spacing between the power stripe and its adjacent wire is exactly the minimum allowed spacing and hence no space is wasted. In other words, the configuration in Fig. 3(a) consumes more routing tracks per unit width of power stripes' metal and in turn leaves

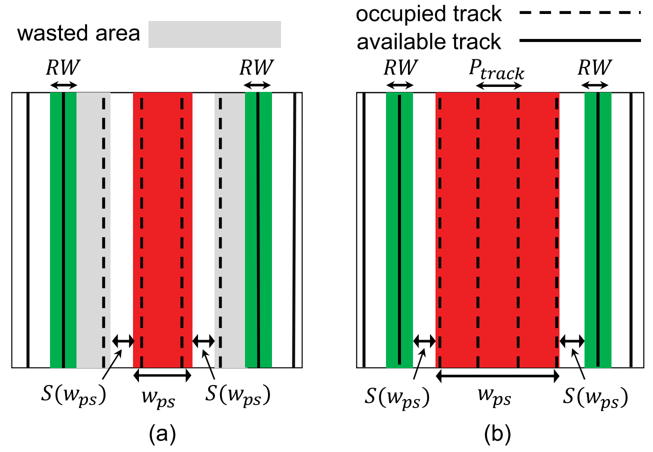

Fig. 3. Example of a redundant and an irredundant stripe width that occupies the same number of routing tracks.

less routing tracks for general interconnect wires when the total metal width for power stripes is fixed. The stripe width shown in Fig. 3(b) is called an irredundant stripe width. In our framework, we always use an irredundant stripe width in the power network to preserve maximal routing tracks for the routing of the underneath circuit.

In addition the number of occupied tracks of a power network, the routing of the underneath circuit can also be affected by the via walls between the M7 power stripes and the M2 power rails. A via wall is formed under the overlapping area between each M7 power stripe and M2 power rail as shown in Fig. 1, and may potentially result in routing detour if the APR tool attempts to connect two pins underneath a power stripe. Therefore, how to estimate the routing impact of the via walls and further minimize it is another crucial task when designing a routing-driven power network.

III. Proposed Power-Network Framework

A. Overall Flow

Fig. 4 shows the overall flow of the proposed framework for building a robust routing-driven power network, where the stripe width is the same for all the power stripes on each metal layer. The proposed framework consists of three major stages. The first stage is to calculate a sufficient total metal width for the top two regular metal layers (i.e., M8 and M7) of the power network, such that the IR and EM constraints can be both satisfied with extra design margin. The inputs of the first stage include the: 1) supply voltage; 2) power consumption of the underneath circuit; 3) pitch between power pads; 4) IR and EM constraints; 5) sheet resistance of each metal specified in library exchange format (LEF); and 6) overall layout area. As we only target the flip-chip designs, our IR and EM analysis can be restricted within a local region of the power network, as shown in Fig. 5, based on the power-pad pitch and the overall layout area [8], [9].

Note that most metal on the AP layer is used for building the power network and its stripe width is the maximum width allowed by the design rules. The metal width on a M2 power rail is predefined in the cell library and the number of power rails is a fixed ratio to the cell height. Therefore, the total

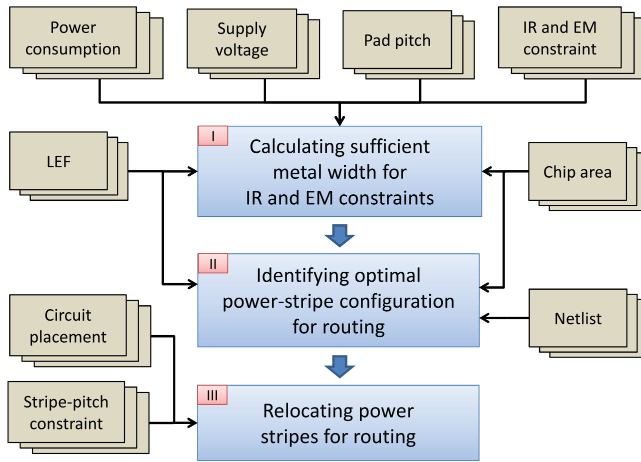

Fig. 4. Overall flow of the proposed framework.

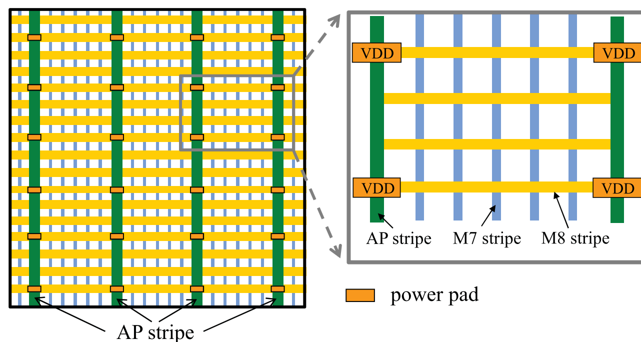

Fig. 5. Minimal local region to be analyzed in a flip-chip design.

metal width on the AP and M2 layers of the power network is almost fixed and not a factor to be considered in our proposed framework.

The second stage of the proposed framework is to identify an optimal routing-driven configuration for the power-stripe layout by considering the number of occupied routing tracks and the potential routing detour as shown in Section II-C. The inputs of the second stage include the: 1) spacing rules specified in LEF; 2) overall layout area; and 3) circuit netlist. This stage uses the concept of the irredundant stripe width to minimize the number of occupied tracks per unit stripe width, and defines a detour cost to estimate the potential routing detour without any information about the cell placement.

The third stage is to relocate the M7 power stripes after the placement such that the routing detour of the cells' follow pins can be further minimized. The inputs of this stage include the: 1) cell placement of the underneath circuit and 2) pitch (or spacing) constraint between two adjacent power stripes. This minimization of the routing detour can be achieved by a dynamic programming approach, which can be scalable for large industrial designs.

Note that during both the second and the third stages, only the impact of routing is considered. The impact of different power-stripe configurations on IR drop and EM is limited and can be well covered by the design margin given in the first stage. Table III shows an example, where the biggest differences on the worst-case IR drop and EM are 0.6 mV and 10.1%, respectively, for different stripe widths in use. In addition, each of the three stages of the proposed framework can be utilized independently and hence can be integrated with other existing power-network design flows. In addition, most of the following discussion focuses on the VDD power network only. The same ideas will be applied to build the GND power network as well.

B. Metal-Scheme Notations in Proposed Framework

In this paper, we use a 8-metal process technology, seven regular metal layers (from M2 to M8) plus one AP layer, as an example to explain the ideas of our power-network framework (the same metal scheme shown in Fig. 1). M8 and M7 represent the metal layers used for placing X-direction stripes and Y-direction stripes of the power network, respectively, which are usually the top two metal layers right below the AP layer. The power stripes on AP layer are Y-directional. When a different metal schemes is used, M8 and M7 may not be the two layer placing X-direction stripes and Y-direction stripes. However, the same ideas of this paper can still be applied as long as we replace M8 and M7 with the corresponding metal layers used for placing X-direction stripes and Y-direction stripes, respectively.

IV. Total Metal Width for Each Power Layer

A. Sufficient Total Metal Width of M8 Power Stripes

In our analysis for IR drop and EM, we use the following three assumptions. First, the resistance along the Y-direction (an AP power stripe) is close to zero due to the low sheet resistance and the large amount of total metal width of AP stripes. Second, the connection between different metal layers is ideal as the via resistance is small enough to be ignored. The minimum resistance along an unit X-direction grid, i.e., an unit grid M8 power stripe with the maximum allowed width, is about 1 ohm while the via resistance is about 0.014 ohm in the adopted 40-nm technology. Third, each intersection between a M7 stripe and a M8 stripe sinks the same amount of current. Note that these three assumptions can reflect the actual design trend on our created power networks. However, they are not 100% true. We just tried to use these simplified assumptions to derive a conservative approximation of the worst-case IR drop at the early design stage.

The current load on each intersection between a M7 stripe and a M8 stripe is denoted as I_{node}. I_{node} can be calculated by (1), where Pow is the overall power consumption in the area, N_{M7} is the number of the M7 power stripes, and N_{M8} is the number of the M8 power stripes

$$I_{\text{node}} = \frac{Pow}{N_{M7} \times N_{M8} \times \text{Vdd}}. \quad (1)$$

The total metal width of M8 power stripes, MW_{M8}, is the maximum value of W_IR_{M8} and W_EM_{M8}, where W_IR_{M8} and W_EM_{M8} represent the sufficient metal width for meeting the IR-drop and EM constraints, respectively. The details of estimating W_IR_{M8} and W_EM_{M8} will be shown in Section IV-A1 and Section IV-A2. Fig. 6 shows the minimum local region of a multilayer power network that needs to be analyzed for a flip-chip design and some corresponding notations used in the analysis.

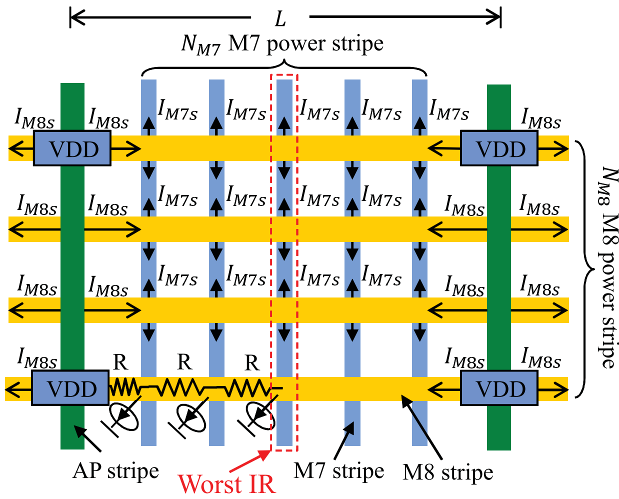

Fig. 6. Illustration and notations for the IR and EM analysis in a multilayer power network.

1) Considering IR Drop on M8: Based on our assumption, the current from an AP stripe to each M8 stripe is the same. The worst-case IR drop of a M8 stripe is right in the middle between the two VDD AP stripes. Therefore, the worst-case IR drop, ΔV, can be estimated by considering only one single M8 stripe as shown in Fig. 7.

Equation (2) list the calculation of ΔV, which should be limited under a predefined IR-drop constraint, $\mathrm{IR_{cons}}$

$$\Delta V = I_{\mathrm{node}} \times R \times \left(1 + 2 + \cdots + \frac{N_{M7}}{2}\right) \leq \mathrm{IR_{cons}}. \quad (2)$$

In (2), R is the grid resistance on a M8 stripe and can be calculated by (3), where R_{oe} and L are the sheet resistance of M8 and the X-direction distance between two VDD pads, respectively

$$R = R_{\mathrm{oe}} \times \frac{\frac{L}{N_{M7}}}{\frac{W_\mathrm{IR_{M8}}}{N_{M8}}}. \quad (3)$$

Combining (1)–(3), we can obtain the lower bound of $W_\mathrm{IR_{M8}}$

$$W_\mathrm{IR_{M8}} \geq \frac{Pow \times R_{\mathrm{oe}} \times L \times \frac{N_{M7}+2}{N_{M7}}}{8 \times \mathrm{Vdd} \times \mathrm{IR_{cons}}} \approx \frac{Pow \times R_{\mathrm{oe}} \times L}{8 \times \mathrm{Vdd} \times \mathrm{IR_{cons}}}. \quad (4)$$

Note that such a minimum $W_\mathrm{IR_{M8}}$ is a conservative estimation since we did not consider the impact of M2 power rails on the IR drop. The M2 power rails are parallel connected to M8 power stripes, and hence can help to further reduce the X-direction IR drop. The reason is that a power network is considered as a media to send current from the power sources to each standard cell. On a power network, there are multiple paths from the current sources to one single cell. If we add extra stripes on a metal layer, such as M2, with the same X-direction as M8, it can create more extra paths from the power sources to the cell. In this case, some current originally flowing on M8 stripes can now go to M2 through the vias first and then go to the end cell. The IR drop on M8 will become less. Simultaneously, M2 rail can also create some IR drop, but the overall IR drop will still be less than the original one. In other words, the M2 rails can share the X-direction current originally flowing on M8 and hence result in smaller effective resistance. Therefore, the extra help from M2 power rails can be viewed as an extra design margin for the IR drop.

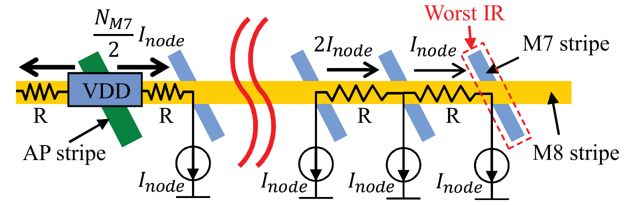

Fig. 7. Illustration of the worst IR drop for M8 power stripes.

2) Considering EM on M8: The EM constraint for M8, $EM_{\mathrm{cons},M8}$, defines the maximum current per metal unit width for a M8 power stripe. The width of a M8 stripe, $W_\mathrm{EM_{M8}}/N_{\mathrm{M8}}$, can be limited by (5), where I_{M8S} is the maximum current on a power stripe as shown in Fig. 6

$$I_{M8S} \times N_{M8}/W_\mathrm{EM_{M8}} \leq \mathrm{EM_{cons,M8}}. \quad (5)$$

The current of each power stripe is the same and the total current load of the analyzed L-wide fragment of a power stripe is supplied by two I_{M8S}: one from the left VDD AP stripe and the other from the right VDD AP stripe. Thus, I_{M8S} can be calculated by (6)

$$I_{M8s} = \frac{Pow}{2 \times N_{M8} \times \mathrm{Vdd}}. \quad (6)$$

Combining (5) and (6), we can obtain the lower bound of $W_\mathrm{EM_{M8}}$

$$W_\mathrm{EM_{M8}} \geq \frac{Pow}{2 \times \mathrm{EM_{cons,M8}} \times \mathrm{Vdd}}. \quad (7)$$

The $W_\mathrm{EM_{M8}}$ obtained by (7) is actually the same as suggested by TSMC's application note [16]. However, this equation is derived under the assumption of the uniform current loads. Note that the distribution of current loads affects the worst-case current density more significantly than the worst-case IR drop in practice. Therefore, our framework uses a highly conservative bound for $W_\mathrm{EM_{M8}}$, which is twice of the value calculated by (7), to avoid EM violations.

B. Sufficient Total Metal Width of M7 Power Stripes

As shown in Fig. 2, the IR drop along the Y-direction is low due to the use of the AP layer. Therefore, IR drop is not a concern when determining the sufficient total metal width of M7 power stripes, denoted as MW_{M7}, as the M7 power stripes are placed along the Y-direction as well. MW_{M7} needs to be large enough to cover the EM constraint for both M2 power rails and M7 power stripes.

1) Considering EM on M2: We first show how the EM constraint for M2 power rails can affect the total metal width of M7 power stripes. The current sinks through the intersection of each M2 and M7 stripe equals the maximum current on a M2 stripe. Based on the uniform current loads, the maximum

current on a M2 stripe, I_{M2S}, can be calculated by (8), where N_{M2} and N_{M7} are the number of M2 and M7 stripes, respectively

$$I_{M2S} = \frac{Pow}{N_{M2} \times N_{M7} \times \text{Vdd}}. \tag{8}$$

I_{M2S} is also limited by the EM constraint for M2, $EM_{\text{cons},M2}$, as shown in (9), where W_{M2S} is the width of a M2 power rail

$$I_{M2S}/W_{M2S} \leq EM_{\text{cons},M2}. \tag{9}$$

Combining (8) and (9), we can obtain the lower bound of the number of the M7 power stripes, N_{M7}, with (10). Note that W_{M2S} and N_{M2} are both a fixed value defined in the library

$$N_{M7} \geq \frac{Pow}{EM_{\text{cons},M2} \times W_{M2S} \times N_{M2} \times \text{Vdd}}. \tag{10}$$

To give a conservative bound of the total metal width of M7 power stripes, we set MW_{M7} as the lower bound of N_{M7} times the largest width allowed for a M7 stripe. Under this setting of MW_{M7}, no matter which M7 stripe width is used, the resulting N_{M7} can exceed the lower bound.

2) Considering EM on M7: Following shows how to calculate MW_{M7} based on the EM constraint on M7. Similar to the calculation above, the width of a M7 stripe, $W_\text{EM}_{\text{M7}}/N_{\text{M7}}$, can be limited by the EM constraint for M7, $\text{EM}_{\text{cons},M7}$, as shown as follows:

$$I_{M7S} \times N_{M7}/W_\text{EM}_{\text{M7}} \leq \text{EM}_{\text{cons,M7}}. \tag{11}$$

In (11), I_{M7S} is the maximum current on a M7 power stripe as shown in Fig. 6. Based on the uniform current load, I_{M7S} can be replaced by $(P\text{ow})/(2 \times N_{M7} \times N_{M8} \times \text{Vdd})$. Then the lower bound of W_EM_{M7} based on the EM constraint on M7 is as follows:

$$W_\text{EM}_{\text{M7}} \geq \frac{Pow}{2 \times N_{\text{M8}} \times \text{EM}_{\text{cons,M8}} \times \text{Vdd}}. \tag{12}$$

Based on our experience, the MW_{M7} calculated based on the EM constraint on M2 (10) can usually exceed the MW_{M7} calculated based on the EM constraint on M7 (12).

C. Experimental Results

In the following experiment, we first use the above proposed method to determine the total width for each layer and build the corresponding power network. Then we compare the resulting power network with one built based on the conventional metal allocation, i.e., the same total width for both M8 and M7 power stripes. Note that the combining total width of M8 and M7 is almost the same for the proposed and the conventional methods (due to some not dividable width). The stripe width used in each layer is an irredundant width and both methods use the same stripe widths. The underneath circuit is still the same 40 nm, 1.1 V, and 900-MHz microprocessor used in Section II-B. The tool, Encounter [23], is used to perform the placement and routing. The IR drop constraint is set to 5% of the supply voltage, i.e., 55 mV. The EM constraint for each metal layer is defined in LEF. The IR-drop analysis is performed by RedHawk [19] based on the actual power density consumed by the microprocessor.

Table I shows the comparison between the two methods after the detail route with respect to different M7 stripe widths in use. To highlight the routing impact caused by a power network, we report the increased wire length defined as the total wire length routed with the power network minus the total wire length routed without any power network, i.e., the wire length purely used for the underneath circuit when there is no power network in the design. As the result shows, the metal allocation of our proposed method can always lead to at least 36.2% smaller increased wire length compared with to the conventional 5050 metal allocation. This is because the proposed method uses less M7 metal layer and hence the potential detour caused by the via walls between each M7 power stripe and M2 power rail can be less. In addition, the total negative slack (TNS), worst negative slack (WNS), and the number of violation paths caused by the proposed metal allocation are all smaller, which is a byproduct of the less total wire length in use and can implicitly lead to faster design closure.

The worst-case IR drop caused by the proposed method always meets the IR-drop constraint with a quite large margin. This is because the sufficient metal width for EM (W_EM_{M8}) is much larger than the sufficient metal width for IR drop (W_IR_{M8}). Using the analytical model shown in Section IV-A1, the estimated worst-case IR drop for this total M8 metal width in use is 15.8 mV, which is still larger than all the reported IR drop caused by the proposed method. This margin results from the total metal width of the M2 power rails, which is almost the same as the total metal width of the M8 power stripes. This result demonstrates that the proposed IR-drop model is indeed a conservative bound. Similarly, the worst-case EM caused by the proposed method ranges from 50.9% to 64.1% of the maximum allowed current density and is also well bounded by the proposed method. The variation of the worst-case EM results from the distribution of the physical current loads. In addition, the worst-case IR drop and EM resulting from the proposed method are both smaller than that from the conventional 50–50 method for all three irredundant M7 widths used in the power network. This is because the worst-case IR drop and EM are mainly determined by the total metal width of the M8 power stripes, which is placed along the opposite direction of the AP power stripes. The above results again show the importance of considering the impact of AP layer when determining the total metal widths for all power layers.

V. Layout Configuration of Power Stripes

A. Irredundant Stripe Width With Minimum Occupied Tracks

As shown in Section II-C, different stripe widths may result in different occupied tracks per metal unit width of the power stripes. When determining the layout configuration of power stripes (including the width, pitch, and offset), we should always use an irredundant stripe width to minimize the number of tracks occupied by power stripes and leave more tracks available for cell routing. Once an irredundant stripe width is used, its spacing to the next possible adjacent wire is exactly the minimum spacing defined in the library as shown in Fig. 3(b).

TABLE I

DETAIL-ROUTE RESULTS OF USING THE POWER NETWORKS GENERATED BY THE PROPOSED METAL ALLOCATION AND THE CONVENTIONAL ONE

Method	Total M8+M7 Width (μm)	M8			M7			Increased Wire Length (μm)	reg2reg			Static Worst IR Drop (mV)	Worst EM
		# of Stripes	w_{ps} (μm)	Occupied Track %	# of Stripes	w_{ps} (μm)	Occupied Track %		TNS (ns)	WNS (ns)	Violation Paths		
Convention (a)	1023.42	346	1.47	43.53	1560	0.33	42.88	238175	39.146	0.076	3516	12.2	79.3%
Proposed (b)	1024.41	544	1.47	68.45	681	0.33	18.72	151949	36.674	0.054	3189	8.3	56.7%
(a−b)/a	-	-	-	-	-	-	-	36.20%	6.31%	28.95%	9.3%	-	-
Convention (a)	1023.12	346	1.47	43.53	350	1.47	31.27	221241	48.847	0.090	3660	12.2	95.8%
Proposed (b)	1024.59	544	1.47	68.45	153	1.47	13.67	117486	40.971	0.055	3572	8.6	50.9%
(a−b)/a	-	-	-	-	-	-	-	46.90%	16.12%	38.89%	2.40%	-	-
Convention (a)	1023.78	346	1.47	43.53	212	2.43	34.96	263138	51.697	0.069	3998	12.4	85.0%
Proposed (b)	1025.67	544	1.47	68.45	93	2.43	15.34	129798	45.957	0.064	3731	8.8	64.1%
(a−b)/a	-	-	-	-	-	-	-	50.67%	11.10%	7.25%	6.68%	-	-

TABLE II

IRREDUNDANT STRIPE WIDTH WITH RESPECT TO EACH T_{ps}

Tps	Wps (μm)	Tps/Wps (1/μm)	Tps	Wps (μm)	Tps/Wps (1/μm)
1	N.A.	N.A.	12	1.33	9.02
2	N.A.	N.A.	13	1.47	8.84
3	N.A.	N.A.	14	N.A.	N.A.
4	0.33	12.12	15	N.A.	N.A.
5	0.47	10.64	16	N.A.	N.A.
6	0.61	9.84	17	N.A.	N.A.
7	N.A.	N.A.	18	1.59	11.32
8	0.77	10.39	19	1.73	10.98
9	0.91	9.89	⋮	⋮	⋮
10	1.05	9.52			
11	1.19	9.24			

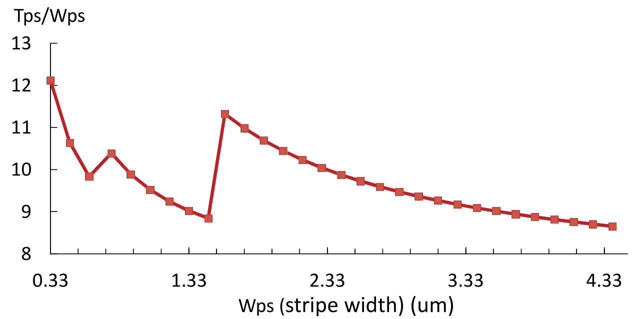

Fig. 8. Number of the occupied routing tracks per metal unit length with respect to different irredundant widths.

Based on Fig. 3, we can list the condition that a stripe w_{ps} can satisfy the minimum spacing rule in (13), where $S(w_{ps})$ is the minimum spacing between the power stripe and its adjacent wire, RW is the wire width, P_{track} is the track pitch, and T_{ps} is the number of tracks occupied by the stripe. In both Fig. 3(a) and (b), T_{ps} is equal to 4

$$w_{ps} + 2S(w_{ps}) \le (T_{ps} + 1) \times P_{track} - RW. \quad (13)$$

An irredundant stripe width is a value of w_{ps} when the equality holds. We will get different irredundant stripe widths if different values of T_{ps} are used. As the minimum spacing $S(w_{ps})$ is a function of w_{ps}, which is not a continual function and represented as a table in the LEF file, the irredundant stripe widths cannot be directly solved. Therefore, we have enumerated each number of T_{ps} and tried to solve its corresponding w_{ps} by searching the boundary values of $S(w_{ps})$ in the library. Table II lists the irredundant stripe width with respect to each T_{ps}.

As Table II shows, not every T_{ps} can map to a valid irredundant stripe width. This is due to the noncontinual nature of the minimum spacing function $S(w_{ps})$, which may (13) unsolvable under certain T_{ps}. In addition, a valid irredundant stripe width needs to meet the lower bound and upper bound of a power stripe. The lower bound of a valid stripe width is the width that can legally put at least two vias on, i.e., the minimum via pitch plus twice of the via enclosure. That is why no valid irredundant stripe width can be obtained from $T_{ps} = 1$ to $T_{ps} = 3$. The upper bound of a valid stripe width is the maximum metal width for a layer defined in LEF.

Note that Table II also reports the number of the occupied routing tracks per metal unit length of a power stripe, i.e., T_{ps}/w_{ps}. A higher value of T_{ps}/w_{ps} means that the more routing tracks need to be spent to build the power stripes with the same total metal width. Therefore, the irredundant stripe width with a lower T_{ps}/w_{ps} is more preferred when the number of the available tracks is the only concern. Fig. 8 plots the value of T_{ps}/w_{ps} for each valid irredundant stripe width, where three local minimal points can be obtained.

Fig. 9 shows the number of occupied tracks after using an irredundant and redundant stripe width to build the power network for the above microprocessor. As the result shows, the three minimal points all result from irredundant stripe widths and are significantly larger than those resulting from the nearby redundant stripe widths. This result again demonstrates the advantage of using an irredundant stripe width.

Once the stripe width is determined for the Mi layer, the corresponding stripe pitch, P_{ps}, and offset, X_{off}, can be calculated by evenly distributing the stripes as shown in Fig. 10. Equations (14) and (15) show the calculation of P_{ps} and X_{off}, respectively, where N_{Mi} denotes the number of the power stripes on the Mi layer and AT_p denotes the number

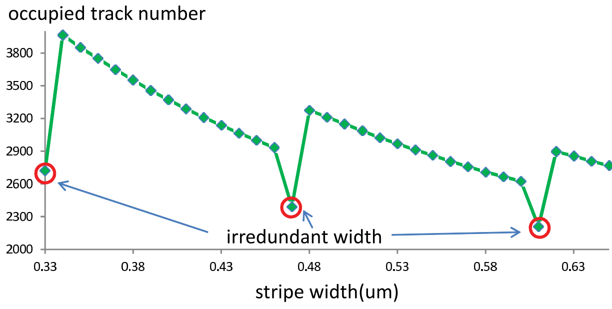

Fig. 9. Number of occupied tracks resulting from redundant and irredundant stripe widths.

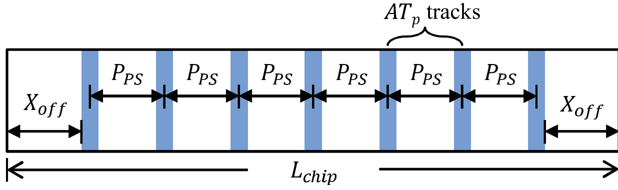

Fig. 10. Layout of evenly distributed power stripes.

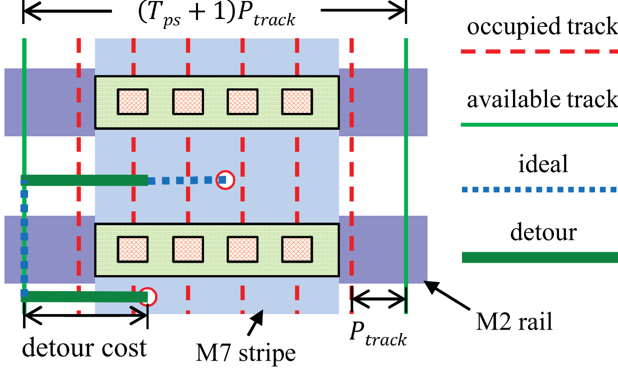

Fig. 11. Illustration of the routing detour caused by the via walls and the defined detour cost.

of available tracks within the stripe pitch

$$P_{ps} = (AT_p - 1) \times P_{track} + 2S(W_{ps}) + R_W + W_{ps} \quad (14)$$

$$X_{off} = (AT_p - 1) \times P_{track} + S(W_{ps}) + \frac{R_W}{2} \quad (15)$$

$$AT_p = \left\lfloor \frac{\left\lfloor \frac{L_{chip}}{P_{track}} \right\rfloor + 1 - N_{Mi} \times T_{ps}}{(N_{Mi}+1)} \right\rfloor. \quad (16)$$

B. Routing Detour Caused by Power Stripes

As discussed in Section II-C, a power network may affect the result of routing by not only the number of the tracks it occupied but also the potential routing detour its via walls may cause. Fig. 11 shows an example of this routing detour when connecting two pins right underneath a power stripe. In this situation, the detour length would depend on how close a pin is placed toward an edge of the via wall, which is usually the width of a power stripe. In other words, if the pin is placed closer to the stripe's center, the detour length would likely be more. If the pin is placed closer to the stripe's edge, the detour length would likely be less.

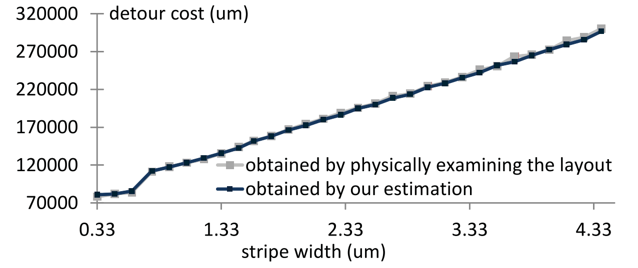

Fig. 12. Detour cost estimated by (17) and physical examination.

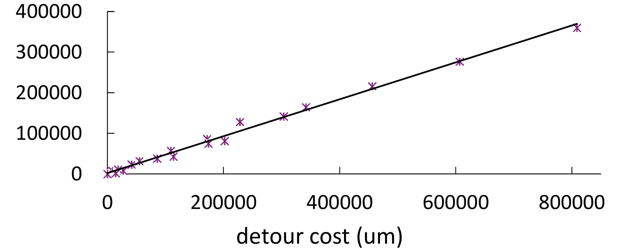

Fig. 13. Actual increased wire length versus its detour cost.

In our framework, we define the detour cost of a pin underneath a stripe as the shortest distance between the pin and its closest not-occupied track. As the cell placement is not done yet at this stage, we can only estimate the expected value of the overall detour cost of all the pins underneath the power stripes, denoted as RD_{tot}. The calculation of RD_{tot} is shown in 17, where N_{pin} is the total number of pins, $N_{Mi} \times (T_{ps}+1) \times P_{track}/L_{chip}$ is the probability that a pin is underneath a power stripe, and $(T_{ps}+1) \times P_{track}/4$ is the average detour cost for a pin randomly locating within a stripe

$$RD_{tot} = N_{pin} \times \frac{N_{Mi} \times (T_{ps}+1) \times P_{track}}{L_{chip}} \times \frac{(T_{ps}+1) \times P_{track}}{4}. \quad (17)$$

Fig. 12 compares the estimated overall detour cost calculated by (17) (label by the blue line) with the actual detour cost obtained by examining each pin underneath the stripes in the layout (label by the gray line) based on the power networks with different irredundant widths. As the result shows, the estimation of (17) can closely match the actual detour cost without using any information of the layout.

Next, Fig. 13 shows the increased wire length with respect to the corresponding detour cost based on the power networks with the same number of the occupied tracks. As the result shows, the detour cost caused by a power network has a high linear correlation with the increased wire length when the number of the tracks occupied the power network is the same, and hence can be good index for measuring the routing impact of M7 power stripes.

C. Experiment of Finding Optimal Stripe Width

As discussed above, when determining the M7 stripe width, we need to consider the two factors: 1) the number of its occupied tracks and 2) the resulting detour cost. Fig. 14

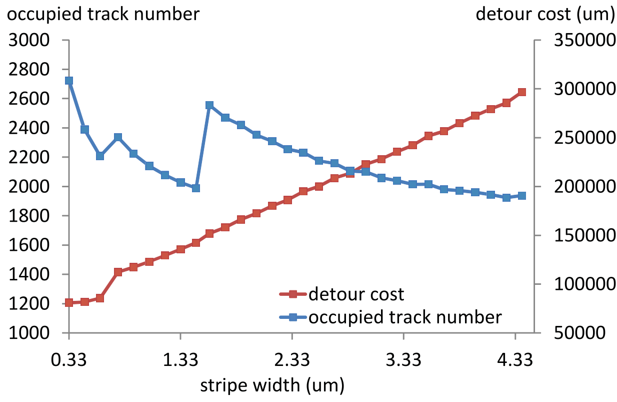

Fig. 14. Occupied tracks and detour cost for each irredundant width.

shows these two factors for each irredundant stripe width when building the M7 power stripes for the microprocessor. By observing the result, the optimal stripe width should fall on the valid candidates around the first and the second minimal points of the number of occupied tracks. A valid candidate is a stripe width that has at least one factor better than the other stripe widths. The valid stripe widths around the third minimal point of the number of occupied tracks all have a detour cost much higher than the valid stripe widths around the first minimal point, but their number of occupied tracks only a little less. Therefore, if the schedule allows, we can try all the valid candidates between the first and second minimal points of the number of occupied tracks, which are around five candidates. If the schedule is tight, we could directly use the stripe width at the first (0.61 μm) or the second (1.47 μm) minimal point.

Table III lists the actual increased wire length of the microprocessor by using the stripe-width candidates between the first and the second minimal points of the number of occupied tracks as the M7 stripe width. As the result shows, the minimum increased wire length falls on the stripe width of 1.19 μm. Note that solution space of the stripe width can be any continual number from its lower bound to its upper bound. With the help of the proposed framework, we can significantly limit the search to only a couple of candidates. In addition, the resulting worst-case IR drop and EM both satisfy the constraints with a significant margin, and the difference of worst-case IR drop among different used stripe widths is also limited. This result again demonstrates the effectiveness of using the total metal width calculated in the previous stage to bound the IR drop and EM.

Note that the optimal stripe width for M8 power stripes is the stripe width with the minimum number of occupied tracks per unit stripe width, T_{ps}/w_{ps}. The M8 stripe width will not induce any routing detour.

VI. Relocating Power Stripes for Routing

A. Problem Formulation and Notations

After the second stage (Section V), we can obtain the first version of the power network with an optimal stripe width and evenly distributed stripes. With this power network, we can perform the placement and routing. Next, based on the placement result, we can further shift the location of the M7

TABLE III
DETAIL-ROUTE RESULT FOR USING DIFFERENT VALID STRIPE-WIDTH CANDIDATES

w_{ps} (μm)	Increased Wire Length (μm)	Worst IR (mV)	Worst EM
033	151949	8.3	56.7%
0.47	125406	8.0	55.7%
0.61	120684	8.2	54.2%
1.05	116702	8.2	53.2%
1.19	110305	8.3	55.0%
1.33	111376	8.5	61.0%
1.47	117486	8.6	50.9%

power stripes to minimize the detour cost for the follow-up pins of all the placed cells. To do so, we first need to examine the cell placement and calculate the detour cost of placing a power stripe at each routing track i, denoted as RD[i]. Following are the notations used in this section.

T	the total number of tracks;
$S_{\min}$	the minimum spacing between two stripes in terms of the number of tracks;
$S_{\max}$	the maximum spacing between two stripes in terms of the number of tracks;
N_{ps}	the total number of M7 power stripes;
RD[i]	the detour cost of placing a stripe at the ith track;
Cost[i][n]	the minimum cost of placing the nth stripe at the ith track;
Low_$b(i)$	the minimum number of placed stripes between the first and ith tracks;
High_$b(i)$	the maximum number of placed stripes between the first and ith track.

Note that we use $S_{\min}$ and $S_{\max}$ to guarantee that the resulting distribution of the M7 power stripes will not be too unbalanced. If two stripes are too close, the via walls caused by the two (or multiple) stripes may virtually merge into one. Under this situation, the actual routing detour would be significantly more than our estimation (17). In addition, if two stripes are too far away, the IR drop at the M2 power rails may be increased, even though its difference is still well bounded by our design margin as shown in the later experiments. In our framework, we usually set $S_{\min}$ and $S_{\max}$ to 0.5 and 2 times of the spacing between two evenly distributed stripes, i.e., $\lfloor T/N_{ps} \rfloor$, respectively.

B. Proposed Dynamic Programming Approach

In our framework, we propose a DP approach to determine stripes' location for minimizing the overall detour cost (the summation of RD[i] for the N_{ps} stripes). The proposed DP approach utilizes the cost function, cost[i][n], to represent the minimum detour cost of placing the nth stripe at the ith track. Then we can calculate cost[i][n] by finding the minimum cost[j][$n-1$], i.e., the minimum detour cost of placing the (n-1)th stripe at the jth track, plus RD[i]. Note that we only need to check the number of j between $i - S_{\max}$ and $i - S_{\min}$ since the ($n-1$)th stripe must be placed at

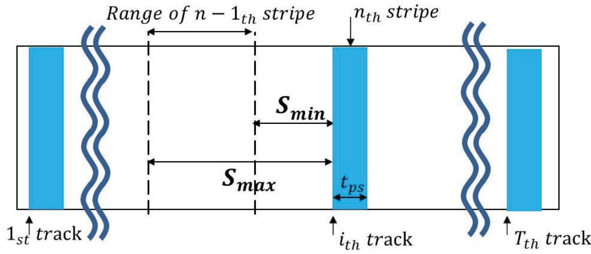

Fig. 15. Illustration of the notations used in the DP-based approach.

```
1 begin
2   for(i=1+S_min; i <=T; i++)
3     for(n=low_b(i); n <=high_b(i); n++)
4       for(j=i-S_max; j <=i-S_min; j++)
5         if(cost[i][n] > cost[j][n − 1]+RD[i])
6           cost[i][n]=cost[j][n − 1]+RD[i]
7 end
```

Fig. 16. Algorithm of the proposed DP-based stripe relocation.

most $S_{\max}$ and at least $S_{\min}$ away from the nth stripe, as shown in Fig. 15. Next, we calculate cost[i][n] starting from $i = 1$ to $i = T$ and from $n = 1$ to $n = N_{\text{ps}}$. The initial condition is cost[1][1]=RD[1] and the final cost function is cost[T][N_{ps}]. Fig. 16 shows the algorithm of the proposed DP approach.

Note that the number of n which needs be calculated for each i is bounded by low_$b(i)$ and high_$b(i)$ calculated in (18) and (19), respectively. low_$b(i)$ is determined by the least number of stripes allowed before the ith track, $\lfloor i-1/S_{\max}\rfloor - 1$, and the most number of stripes allowed after the ith track, $N_{\text{ps}} - \lceil T-i/S_{\min}\rceil$. Similarly, high_$b(i)$ is determined by the most number of stripes allowed before the ith track, $\lfloor i-1/S_{\min}\rfloor - 1$, and the least number of stripes allowed after the ith track, $N_{\text{ps}} - \lceil T-i/S_{\max}\rceil$

$$\text{low_b}(i) = \max\left(\left\lfloor \frac{i-1}{S_{\max}} \right\rfloor - 1, N_{\text{ps}} - \left\lceil \frac{T-i}{S_{\min}} \right\rceil\right) \quad (18)$$

$$\text{high_b}(i) = \min\left(\left\lfloor \frac{i-1}{S_{\min}} \right\rfloor - 1, N_{\text{ps}} - \left\lceil \frac{T-i}{S_{\max}} \right\rceil\right). \quad (19)$$

C. Experimental Results

Table IV compares the routing result of the original evenly-distributed power network with those after applying the proposed DP-based stripe relocation with $S_{\max}$ assigned as 1.25, 1.5, 2.0, and 3.0 times of the original stripe spacing. The $S_{\min}$ is set to 0.5 times of the original stripe spacing and the M7 stripe width is set to 1.47 μm. As the result shows, our proposed DP-based approach can effectively reduce the actual wire length after detail route. In addition, with a larger $S_{\max}$ in use, the increased wire length, violation paths, total negative slack, and WNS will all become smaller in general. However, when $S_{\max}$ is set to 3.0 times of the original stripe spacing, its violation paths and TNS starts to increase even though the increased wire length decreases. Therefore, we usually set $S_{\max}$ to only two times of the original stripe spacing or less. The runtime is less than 5 min for all cases, showing that

TABLE IV
RESULT AFTER APPLYING THE STRIPE RELOCATION WITH DIFFERENT $S_{\max}$

$S_{\max}$	Increased Wire Length (μm)	reg2reg Violation Paths	reg2reg TNS (ns)	reg2reg WNS (ns)	Worst IR Drop (mV)	Worst EM	Run Time (Sec)
original	117486	3572	40.97	0.055	8.6	50.9%	-
1.25X	104535	3415	39.20	0.049	8.7	53.2%	284
1.5X	102808	3404	38.35	0.047	9.1	57.8%	285
2.0X	92179	3382	37.78	0.050	9.0	47.0%	285
3.0X	91364	3418	40.08	0.048	9.3	63.9%	286

TABLE V
RESULT AFTER APPLYING THE STRIPE RELOCATION TO THE POWER NETWORKS WITH DIFFERENT STRIPE WIDTHS

w_{ps} (μm)	Detour Cost (μm) Original (a)	Detour Cost DP (b)	Detour Cost (a−b)/a	Increased Length (μm) Original (c)	Increased Length DP (d)	Increased Length (c−d)/c
0.33	80895	63433	21.6%	151949	121826	19.8%
0.47	81764	65257	20.2%	125406	112029	10.7%
0.61	85679	65777	23.2%	120684	98050	18.8%
1.05	123036	94684	23.0%	116702	97249	16.7%
1.19	129317	100851	22.0%	110305	99050	10.2%
1.33	135708	106760	21.3%	111376	100760	9.5%
1.47	142488	111506	21.7%	117486	92179	21.5%
avg.	-	-	21.9%	-	-	15.3%

the proposed DP-based stripe relocation can be scalable for large industrial designs. Most runtime of the proposed stripe relocation is on collecting each RD[i] based on the placement, not the dynamic programming part.

Table V further reports result of applying the proposed DP-based stripe relocation to the power networks with different M7 stripe widths. The $S_{\max}$ and $S_{\min}$ are set to 0.5× and 2.0×. As the result shows, the proposed DP-based approach can effectively reduce the detour cost by an average 21.9% and in turn reduce the actual wire length after detail route by an average 15.3%. This result again demonstrates that the detour cost is an important index for building a routability-driven power network.

VII. ADDITIONAL EXPERIMENTS

A. Complete Framework Comparison

In this subsection, we would like to show the result of the whole proposed framework (combining all three stages) and compare it to the conventional 50–50 method for the top two metal (M8−M7) distribution, which is the same method shown in Table I and was suggested by several previous works [11], [17]. Both the proposed framework and the conventional method utilize the same amount of the total metal width. We also randomly select 4 different metal widths for the conventional 50–50 method and use the best result among them to compare with the proposed framework. The $S_{\max}$ and $S_{\min}$ are set to 0.5 and 2.0× in the third stage of the proposed framework. The design in this experiment is the same as all of the above experiments in this paper, which is a 1.1 V, 900-MHz

TABLE VI
COMPARISON BETWEEN THE WHOLE PROPOSED FRAMEWORK AND THE CONVENTIONAL METAL-DISTRIBUTION METHOD

Method	M7 w_{ps} (μm)	M8 w_{ps} (μm)	Increased Wire Length (μm)	reg2reg TNS (ns)	reg2reg WNS (ns)	reg2reg Violation Paths	Static Worst IR Drop (mV)	Worst EM	Global Route Congestion Analysis: Total Over-Congestion Gcell	Gcell Overflow Tracks Distribution (1–7)	(8–15)	(16–22)	(23–32)
Convention	0.35	2.30	363388	52.20	0.107	4191	8.7	80.9	17851	17834	13	2	2
	1.60	4.00	223338	48.25	0.065	3810	8.8	72.5	16631	16617	8	4	2
	3.00	1.60	280540	55.79	0.086	4166	8.8	96.7	42125	42090	28	5	2
	4.40	3.84	349722	60.58	0.061	4525	9.4	98.1	45710	45700	8	0	2
Best of convention (a)	1.60	4.00	223338	48.25	0065	3810	8.8	72.5	16631	16617	8	4	2
Proposed (b)	0.61	1.47	88170	36.10	0.048	3260	8.6	66.0	10440	10430	7	1	2
(a−b)/a	-	-	60.5%	25.2%	26.2%	14.4%	-	-	37.2%	-	-	-	-

microprocessor with 3 026 751 gates. The layout dimension is 2037.28 $\times$1446.48 μm.

Table VI first lists the comparison result of the detailed route, where the increased wire length, the TNS, the WNS, and the number of timing violation paths of the proposed framework are 60.5%, 25.2%, 26.2%, and 14.4% less than that of the conventional methods, respectively. Table VI also lists the result of the congestion analysis performed in the global route, including the number of over-congestion Gcells and the distribution of the number of overflow tracks within each over-congestion Gcell, where a Gcell is the routing unit defined in [23]. As the result shows, the number of over-congestion Gcells resulting from the proposed framework is also significantly less (37.2%) than that resulting from the conventional method, demonstrating that the routing resources saved by the proposed framework can not only result in less total wire length but also help to resolve potential routing congestion. Table VI further lists the result of the IR-drop analysis, where the worst IR drop and the worst EM of the proposed framework are both less than that of the conventional method.

Table VII further lists the runtime distribution of the proposed framework, including the runtime of parsing the LEF file to obtain the process parameters and design rules and the runtime of each stage of the proposed framework. As the result shows, most of the runtime of the proposed framework spends on the third stage, i.e., relocating the power stripes. The overall runtime of the proposed framework is less than 5 min. If we try different stripe widths w_{ps} for the power network, run the detail route, and choose the best w_{ps} just like what conventional method does in Table VI, it may take several days (each round of detail route takes more than 12 h). Note that computing the whole table of irredundant stripe widths corresponding to each T_{ps} in the second stage (such as Table II) only takes 1 s, which is highly efficient. In addition, the produced power network in Table VI contains 1.7 million nodes and 2.2 million resistors, which again demonstrates the effectiveness and efficiency of our proposed framework on large industrial cases.

B. IR Drop on Different Metal Layers and vias

In this subsection, we try to validate the first two assumptions used in Section IV by reporting the IR drop on different metal layers and vias. We first build a power network by using the first stage and second stage of the proposed framework. Next, we run a power analysis and report the grid location with the lowest voltage at the VDD network. Then we define the target region as the minimal rectangle covering the lowest-voltage location and its closest VDD power source, as shown in Fig. 17.

TABLE VII
RUNTIME OF EACH STEP OF THE PROPOSED FRAMEWORK

Runtime (Sec): Read in LEF	Stage1	Stage2	Stage3: Read in Placement	Stage3: DP	Total
2	1	1	283	2	289

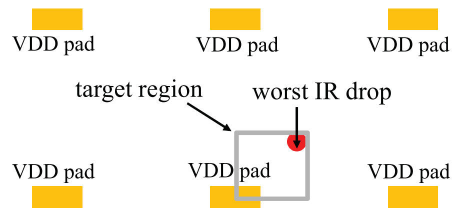

Fig. 17. Illustration of the target region used in the experiment.

Table VIII lists the average IR drop on each M8 power stripe (denoted by M8), each M7 power stripe (M7), each M8-to-M7 via (via87), and each M7-to-M2 via (via72), respectively. As there is only one M2 power rail directly connecting to the lowest-voltage location, the reported IR drop on M2 is the IR drop on that particular M2 power rail. As the result shows, the IR drop on M7 stripes, M2 stripes, M8-to-M7 vias, and M7-to-M2 vias are 14.9%, 3.3%, 1.9%, and 14.5% of that on M8 stripes, respectively, showing that the IR drop of our generated power networks is mainly determined by the M8 stripes.

Note that the total metal width on M8 in the above power network is constrained by the EM constraint, not the IR-drop constraint, meaning that the total metal width on M8 is larger than its minimum sufficient width for meeting the IR-drop constraint and hence the IR drop on M8 is smaller than we expect. Table IX lists the IR-drop distribution if only the IR-drop constraint is used to determine the total metal width on M8. As the result shows, the IR-drop on M7 stripes,

TABLE VIII
AVERAGE IR DROP ON POWER STRIPES AND VIAS WHEN CONSIDERING BOTH EM AND IR CONSTRAINTS

IR Drop (mV)					Ratio			
M8	M7	M2	via87	via72	$\frac{M7}{M8}$	$\frac{M2}{M8}$	$\frac{via87}{M8}$	$\frac{via72}{M8}$
2.994	0.447	0.100	0.058	0.434	14.9%	3.3%	1.9%	14.5%

TABLE IX
AVERAGE IR DROP ON POWER STRIPES AND VIAS WHEN CONSIDERING IR CONSTRAINT ONLY

IR Drop (mV)					Ratio			
M8	M7	M2	via87	via72	$\frac{M7}{M8}$	$\frac{M2}{M8}$	$\frac{via87}{M8}$	$\frac{via72}{M8}$
6.722	0.463	0.044	0.160	0.277	6.9%	0.7%	2.4%	4.1%

M2 stripes, M8-to-M7 vias, and M7-to-M2 vias are 6.9%, 0.7%, 2.4%, and 4.1% of that on M8 stripes. This result is more close to the situation described in the first and second assumptions used in Section IV, that is: 1) the Y-direction resistance is much smaller than the X-direction resistance and 2) the resistance of a vias has limited impact on the overall IR drop.

In summary, if we only consider IR drop constraint, then the assumptions made in Section IV can hold very well. If we consider EM constraint, the assumptions may not hold as strong as it states, but the IR drop can only become better. Either way our assumptions will not hurt the effectiveness of our estimation in Section IV.

C. Reminder of the Experiment Setup

In our analysis, the overall power consumption of the targeted domain is determined by giving a specified voltage, a specified frequency, an estimated total capacitance and an estimated worst-case transition percentage, which usually obtained by simulations. Some margins are added in the estimated capacitance and the estimated worst-case transition percentage to cover the corner case. However, we assume uniform current distribution for the power network in our analysis, which cannot be the real case as the final placement is never evenly distributed. Therefore, in our experiments, we performed the commercial IR-drop analysis (Red-Hawk [19]) based on the final placement to validate that our produced power network can indeed control its worst-case IR drop under our predefined threshold in the real case.

VIII. SUMMARY OF DIFFERENCES

The content of this paper has never been published or is currently under review at any other journal or conference.

IX. CONCLUSION

In this paper, we presented a novel framework to efficiently build a robust but routing-friendly multilayer power network. The framework first showed how to allocate proper total metal width on each power layer to meet the IR-drop and EM constraints by considering the impact of the AP layer. Second, the framework defined an irredundant stripe width that can eliminate the redundant spacing between a power stripe and its adjacent wire and hence consumes less occupied tracks. The framework also defined the detour cost to estimate the potential detour caused by a stripe width. Then an optimal stripe width can be obtained by considering the number of occupied tracks and the detour cost. Last, the proposed framework applied a DP-based stripe relocation to further reduce the detour cost after the cell placement was done. Based on our practical experience, the proposed framework can effectively generate a power network with high routability and in turn significantly shorten the time to achieve the back-end design closure.

X. POTENTIAL FUTURE WORK

Decap insertion is a popular and effective technique to reduce the dynamic IR drop in practice. Conventionally, a decap insertion scheme is applied after the power network and the placement is done, and the decaps are added into the empty space of the placement [24], [25]. However, the added decaps in the empty space may not be close enough to the hotspot of the power network. Therefore, some later research works further attempted to build an effective distributed decap network while satisfying physical placement constraints [26], [27], or even modified the placement during decap insertion according to the hotspot reported for the previous version of the placement [28], [29]. In other words, decap insertion is a process highly correlated to the result of the automatic placement-and-routing and the hotspot resulting from the given power network and the current cell placement.

Therefore, predicting the amount of the IR drop that can be reduced by later decap insertion is a highly challenging task at the stage of determining the layout configuration of power network. However, if we can successfully estimate the IR drop combining the impact of both power network design and the later decap-insertion scheme, we can further adjust our power network design at early design stage and construct a more economic power network with less routing resource. Therefore, considering decap insertion at the stage of building a power network can be interesting, challenging, and useful future work.

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