Fast Transistor Threshold Voltage Measurement Method for High-Speed, High-Accuracy Advanced Process Characterization

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***Abstract*— As process technologies continually advance, process variation has greatly increased and has gradually become one of the most critical factors for IC manufacturing. Furthermore, these increasingly complex processes continue to make greater use of stressors for mobility enhancement, thus requiring large volumes of data for extensive characterization of layout-dependent effects (LDE) for validation of both SPICE models and design for manufacturing. Transistor threshold voltage (V_t) is a commonly used parameter both for characterization during process development and for monitoring of volume manufacturing. To adequately quantify local process variation or LDE, V_t must be measured for a sufficiently large number of device-under-tests (DUTs) to obtain a statistically representative sample population. The number of V_t measurements required to obtain such a statistically significant result, however, requires extremely long testing time, especially for array-based test structure designs including thousands of DUTs. In this paper, we present a very fast threshold voltage measurement methodology using an operational amplifier-based source-measure unit test configuration, which greatly improves testing efficiency and accuracy, and is not sensitive to process variation. The proposed test methodology can improve V_t testing time by a factor of 5–10 relative to the commonly used binary-search algorithm, and by a factor of ∼2 relative to an optimized interpolation algorithm, and achieves better accuracy (standard deviation of V_t = 0.15 mV, versus typical accuracy of ∼0.5 mV for the two algorithms mentioned). Furthermore, the layout and configuration of conventional test structures need not be modified to adapt the proposed methodology. The measured results from the most advanced process technology nodes demonstrate the testing efficiency and accuracy of the proposed test structure in characterizing the large number of DUTs required for quantifying process variation or LDEs.**

***Index Terms*— Design for manufacturing (DFM), Threshold voltage, Variation,**

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I. Introduction

As THE feature size of devices scales down, the device variability imposed by each process step does not scale accordingly. Therefore, the process variation of advanced process technology nodes greatly increases and becomes a critical factor in both IC design and manufacturing [1]. To design and manufacture in the presence of process variation, many research efforts have been focused on the areas of measurement, analysis, and modeling of variation during the past decade [2]–[9], [12]. Furthermore, modeling and design for manufacturing (DFM) of increasingly complex process technologies incorporating process features such as stressed contact etch-stop layers, SiGe source/drain [9], stress memorization technique [11], and so forth requires a much larger range of test structures and larger data volume to accurately characterize the layout-dependent effects (LDE) resulting from these process features. The need to accurately characterize both process variation and increasing complex LDE has dramatically increased the number of testing required during all stages of process development and manufacturing, which in turn demands the development of more efficient test structures and methods that can provide this data without increasing test time to unfeasible levels. During conventional device characterization for the study of LDE and process variation, a conventional test structure, i.e., a process control monitor (PCM) testline, is placed in a wafer's scribe line. The PCM testline has device-under-tests (DUTs) and I/O pads aligned along a straight line and uses four I/O pads to measure each DUT. Thus, both the height of a PCM testline and the required spacing in a scribe line are limited [19]. Only a relatively limited number of DUTs can be placed in such a testline configuration because of the limited number of I/O pads. To effectively use limited scribe-line space to place and individually measure a sufficiently large number of DUTs to address the characterization needs of DFM, LDE, and process variation, several array-based test structures are proposed to share I/O pads among DUTs and hence reduce the number of I/O pads required between the DUTs [13], [15], [16].

Transistor threshold voltage (V_t) is a commonly used parameter to quantify transistor performance both during process development and volume manufacturing [20]. There are several different definitions of the threshold voltage of a metal oxide semiconductor field-effect transistor (MOSFET)

device [24]. The most commonly used definition for process monitoring in IC foundries is constant current V_t. The constant current V_t measurement is generally performed by a binary search algorithm. The binary search algorithm, however, requires much longer testing time compared with measurement of other MOSFET parameters such as I_{on}, I_{off}, and so forth. Moreover, the number of DUTs significantly increases when array-based test structures are employed to collect a large enough sample size for statistically meaningful results, and the V_t measurements represent the most time-consuming portion of the characterization of these DUTs.

Operational amplifier (op-amp or OP)-based methods were proposed to simplify and accelerate V_t measurement [21]. Recently, the research of [23] has also proposed similar methods, employing an on-chip op-amp design combined with an addressable FET array. Such op-amp schemes enable rapid characterization of V_t distributions with large numbers of data samples. There are, however, several major challenges in on-chip OP-based amplifier design for V_t measurement. First, the V_t measured by OP-based test structures may be impacted by body effect because of nonzero source voltage, e.g., as would occur in the circuit of [23]. Second, variation of on-chip load resistance (R_{load}) can result in an inaccurate V_t measurement. This latter issue will become much more severe in modern advanced process technology nodes because of the scaling of feature size without corresponding scaling of variability. Finally, schemes using on-chip OP-based structures are limited by the op-amp accuracy and gain. In 0.35-μm technology, an OP gain of 100 dB is easily achieved using folded cascode design. The gain, however, decreases significantly in advanced technologies because of small transistor output resistance and reduction in headroom. In such advanced technologies, the design of op-amps with gain as high as 100 dB requires additional circuitry. Therefore, the layout area devoted to the op-amp significantly increases, which might prevent the design of practical testlines that can be placed within the wafer scribe line. Furthermore, device mismatch is very poor in the early stages of process development. Therefore, there may be substantial errors in the V_t measured by on-chip OP-based test structures during the early stages of process development.

In this paper, we propose a design and methodology for V_t measurement using high gain and high accuracy op-amp-based Source-Measure Units(SMUs) directly connected to the DUT. The OP-based SMUs are implemented using discrete ICs which are well calibrated by the tester supplier, and thus are not sensitive to process variation. The experimental results that we present, based on advanced process technologies, demonstrate that the proposed design reduced V_t testing time by a factor of 5–10 relative to the conventional binary search V_t measurement algorithm, while simultaneously delivering improved accuracy, with a V_t standard deviation below 0.15 mV. Moreover, combined with array-based test structure, the test time can be further improved due to time overhead saving from the connect, disconnect operation between SMUs and testlines I/O pads and prober index time, which is prober chuck moving time from one testline to another.

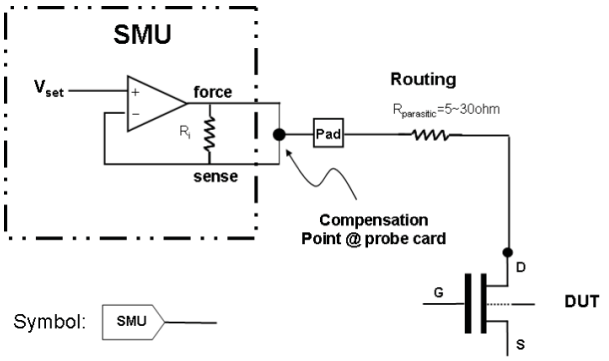

Fig. 1. Voltage compensation mechanism used in a conventional PCM testline. Hereafter, each SMU will be denoted by the symbol indicated in the lower left of the figure.

Another valuable example for the use of array-based test structures to characterize the statistical variation of a large number of transistors was contained in the research of [17], wherein a combination of an array of individually addressable identical devices was combined with an innovative comparator-based measurement scheme was used to extract the difference in the V_t of each device in the array compared with a reference transistor, and thus to determine the statistical distribution of V_t throughout the entire array. This technique was quite effective for quantifying the statistical distribution of V_t for a particular device layout, but because the quantity directly measured was the difference between the V_t of the addressed DUT and a reference transistor, the structure was limited to characterization of the statistical variation of multiple transistors with the same geometry and layout of the reference device. In contrast, the test structure we present can directly measure the dc transistor characteristics of each addressed device in the array, and thus does not require a reference device, and can accommodate multiple device geometries within the same array. The direct measurement of each addressed device without use of a reference also avoids measurement errors induced by deviations in the peripheral circuitry such as source follower mismatch. Finally, although the research of [17] constitutes a quite ingenious method of measuring the statistical variation of V_t, its principle focus was on V_t measurement, whereas the method we propose here-in can be readily extended to other standard transistor parametrics (e.g., I_{dsat}, I_{off}, etc.,) because the key measurement infrastructure is off chip.

II. Background

A. Measuring Constant Current V_t Using a Binary Search Algorithm

In a traditional parametric tester V_t measurement, the SMUs are configured as voltage sources, which can be modeled as unity-gain buffers as shown in Fig. 1 [19]. V_t can be defined as the gate-to-source potential required to drive the threshold drain-to-source current, $I_{ds}(V_t) = (I0,\ n)^* W_{eff}/L_{eff}$ for n-FET, and $I_{ds}(V_t) = (I0,\ p)^* W_{eff}/L_{eff}$ for p-FET, where I0, n and I0, p are parameters of a given process technology for n-FET and p-FET, respectively. In this paper, we use I0 = 20 nA/μm for both N and pMOS. Before beginning the binary

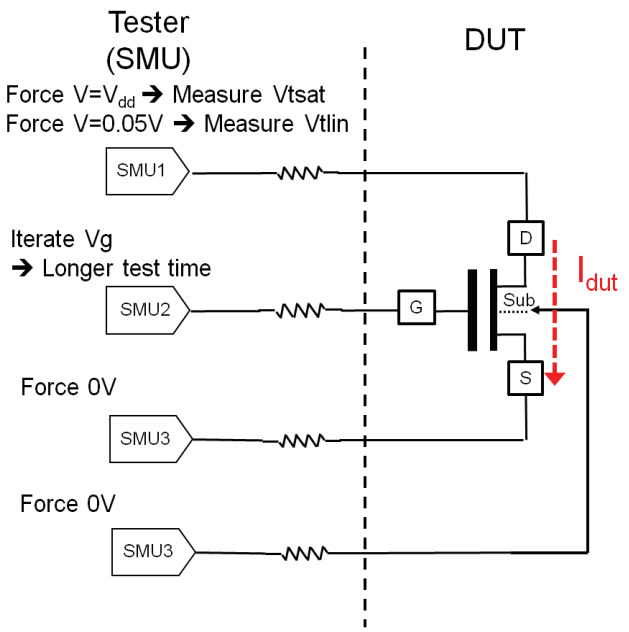

Fig. 2. SMU connection and bias condition for V_t measurement using a binary search approach for n-FET.

```
1.  double Va=Vgstart;;
2.  double Vb=Vgstop;
3.  double Itarget=It0*Weff/Leff
4.  double converge_criteria=1%;

5.  connect(smu1,drain);
6.  connect(smu2,gate);
7.  connect(smu3,source);
8.  connect (smu4,bulk);
9.  Vforce=(Va+Vb)/2;
10. for(int i=0; i<N; i++)
11. {
12.     force_v(gate_pin, Vforce);
13.     measure_i(drain_pin, Ids)
14.     double match=(Ids-Itarget)/Itarget *100;
15.     If(match < converge_criteria)
16.     {
17.         Vth=Vforce;
18.         return;
19.     }
20.     else
21.     {
22.         if(Ids<Itarget)
23.         {
24.             Va=Vforce;
25.             Vforce=(Vb+Vforce)/2;
26.         }
27.        If(Ids>Itarget)
28.         {
29.             Vb=Vforce;
30.             Vforce=(Va+Vforce)/2
31.         }
32.     }
33.     Vth=Vforce;
34. }
```

Fig. 3. Pseudocode of binary search V_t measurement.

search for V_t measurement, the following parameters of the binary search must be specified: 1) gate voltages V_{gstart} and V_{gstop}, which specify the range of gate voltages to be searched and 2) a convergence criteria for matching the target current. In the first iteration, SMU2 forces the search voltage value, $V_{\text{force}} = (V_{\text{gstart}} + V_{\text{gstop}})/2$, to the gate node of the DUT while SMU1 measures the drain current (I_{ds}) and compares it with the target value. If the matching criteria $(I_{\text{ds}} - I_{\text{target}})/I_{\text{target}} <$ matching tolerance, is met, V_t is assigned to V_{force}. If it is, however, larger than the matching criteria, another iteration must be performed. Before proceeding to the next iteration, V_{force} must be modified. If $I_{\text{ds}} > I_{\text{target}}$ then SMU2 forces the search voltage value $V_{\text{force}} = (V_{\text{gstart}} + V_{\text{force}})/2$. In contract, if $I_{\text{ds}} < I_{\text{target}}$ then SMU2 forces the search voltage value $V_{\text{force}} = (V_{\text{force}} + V_{\text{gstop}})/2$.

In subsequent iterations, the SMU2 applies gate voltage values above and below V_t, which become increasingly close to V_t with successive iterations until the current measured by the sense unit matches the target value within the specified criteria. Fig. 3 lists the pseudo-code implementation of a binary search algorithm for finding the gate voltage resulting in a specified drain current. The accuracy of the result obtained by this algorithm strongly depends on the convergence condition and the maximum number of iterations, which thus presents a trade-off between testing time and accuracy. Fig. 4 schematically shows the iteration of forcing voltage and measuring current for V_t measurement using the binary search algorithm.

Therefore, the binary search algorithm for V_t measurement typically requires much longer testing time than the measurement of other device parametrics such as I_{on}, I_{off}, and subthreshold swing. For the measurement of a number of DUTs large enough to obtain a statistically significant quantification of process variation, or to perform adequate characterization for LDE modelling or DFM verification, the test time correspondingly increases and may limit the number of DUTs that can be measured, thus also limiting the accuracy of the characterization.

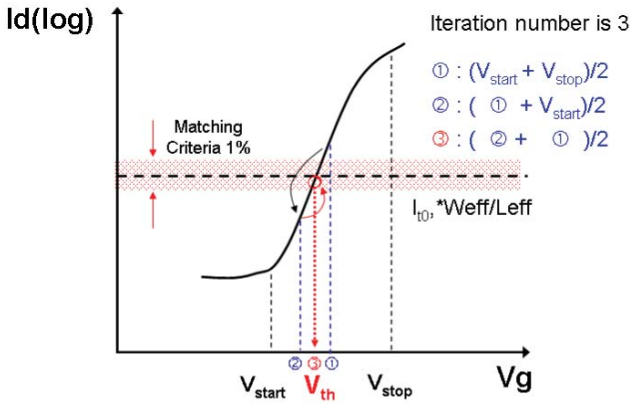

Fig. 4. Example of iterating V_g to obtain drain current matching target within specified criteria.

B. Improving Constant Current V_t Testing Time Using an Interpolation Methodology

One approach to reduce the number of SMU force-measure iterations below the number required by the binary search algorithm is to apply an interpolation algorithm. The number of force-measure iterations can be reduced from six to nine iterations for the binary search algorithm to three iterations for the interpolation algorithm. The interpolation method is performed by setting the two initially defined gate voltages, Vg_hi and Vg_lo, to corresponding drain current values very close to the target current (e.g., $I0, n^* W_{\text{eff}}/L_{\text{eff}}$ for n-FET). To minimize the interpolation error, one gate voltage is set to

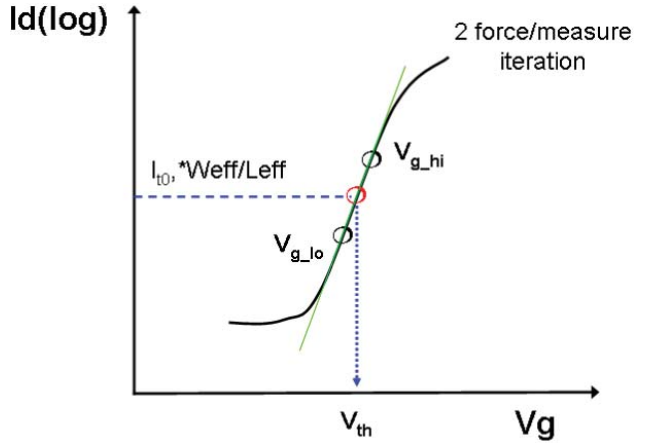

Fig. 5. Setting the initial gate voltage values to interpolate to the gate voltage corresponding to the target drain current. Log scale is used only for ease of visualization. In practice, linear scale is used for V_t interpolation.

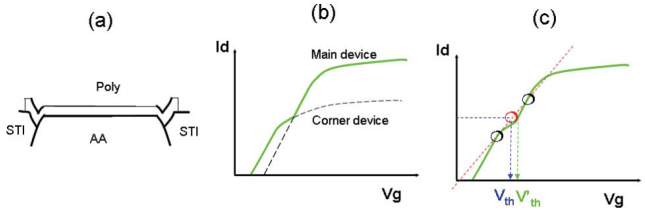

Fig. 6. Double-hump transistor I–V curve resulting from use of STI. (a) Cross-section of a transistor perpendicular to the channel length, including both the region where the gate lies over the active area (AA), i.e. the Main Device, and the two Corner Devices where the gate lies over the transition region between active area and STI. (b) Individual I–V characteristics of the main and corner devices. (c) I–V characteristic of the entire transistor including both main and corner devices. The two local maxima of Id, i.e. the "double hump" characteristic potentially results in very different values of Vt by the binary search and interpolation techniques.

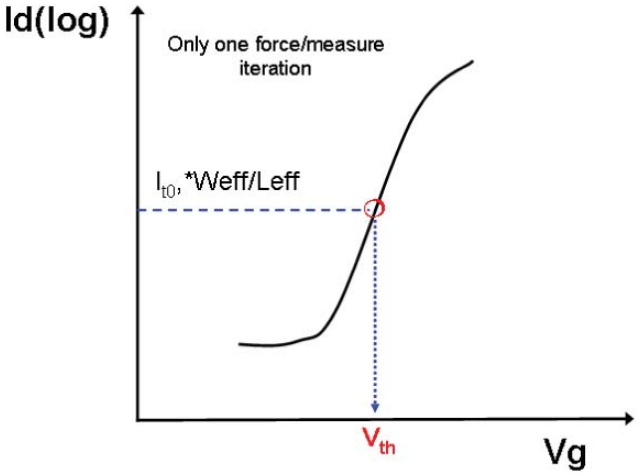

Fig. 7. Only a single force-measure iteration is required by the OP-based V_t measurement technique.

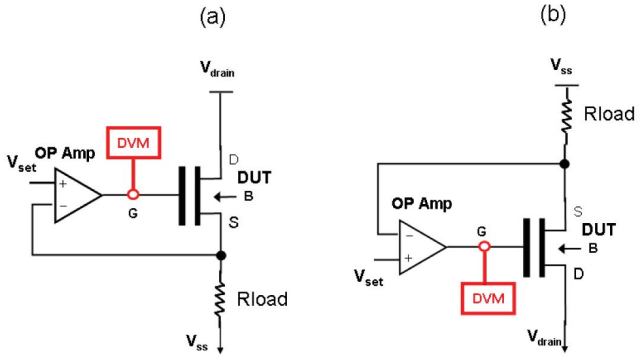

Fig. 8. Circuit schematics for OP-based V_t measurement, where the DUT is (a) n-FET and (b) p-FET.

drive a drain current slightly higher than the target current, and the other gate voltage drives a drain current slightly lower than the target, as shown in Fig 5. The V_t value can be simply obtained by interpolation because of the linear I–V characteristics in the subthreshold region. This interpolation methodology is easily applied to measure the variation of DUTs with identical or nearly identical dimensions because the same initial voltage settings and current criterion can be used for all DUTs. However, for the characterization of many DUTs with different transistor dimensions, e.g., for DFM, SPICE modeling or other process characterization, it may be difficult to define initial gate voltages appropriate to all DUTs. Moreover, in the case of a MOSFET fabricated using shallow-trench-isolation (STI), the gate region runs flat across the isolation. Therefore, the portion of the gate over the field region creates a two-dimensional fringing field on the corner and sidewall region as shown in Fig. 6(a), which effectively creates a corner parasitic MOSFET in parallel with the main DUT. The parasitic device turns on at a gate voltage lower than that of the main DUT channel, resulting in a hump in the I_d–V_g curve as shown in Fig. 6(b) [22]. As shown in Fig. 6(c), a MOSFET with such a hump in its I_d–V_g characteristic exhibits a significant difference between the values of V_t obtained by interpolation and binary search methodologies, respectively. Therefore, this interpolation technique cannot be applied to devices exhibiting nonlinear I–V characteristics in the subthreshold region, such as those with parasitic corner devices resulting from STI. As STI is a common feature of almost all modern CMOS technologies, this severely limits the utility of the interpolation technique.

C. Fast V_t Measurement Using an On-Chip Op-Amp-Based Test Structure

Although the number of force-measure iterations can be reduced from ~9 for binary search to two for the interpolation algorithm as described above, the V_t value obtained by the interpolation algorithm is less accurate than that obtained by binary search. The number of force-measure iterations for constant current V_t measurement can actually be further reduced to only a single iteration, while maintaining higher measurement accuracy, by adopting op-amp-based test structures using an on-chip op-amp. This technique for V_t measurement using only one force-measure iteration is shown in Fig. 7. Fig. 8 shows the circuit schematics for the op-amp-based test structure for V_t measurement. In Fig. 8(a), $V_{\rm set}$, $V_{\rm ss}$, V_b, and V_d are input terminals and V_g is the op-amp output, which is connected to both the DUT gate and a digital voltmeter which in turn measures V_g [21], [23].

In Fig. 8(a), where the DUT is a NFET, the DUT source voltage is forced to $V_{\rm set}$ by the op-amp feedback loop. The higher accuracy V_t measurement is performed by forcing a precise bias current of $(V_{\rm set} - V{\rm ss})/R_{\rm load}$, where $R_{\rm load}$ is the resistance of a precision load resistor and $V_{\rm ss}$ is typically equal to 0 V for the characterization of a NFET. By appropriate

selection of V_{set}, this current is set equal to the threshold current value and is fed to the source terminal of the DUT. The OP output voltage is automatically modulated by the OP feedback loop to maintain the threshold current, and it quickly converges to a voltage equal to the V_t of the DUT. Fig. 8(b) shows the V_t measurement setup for a p-FET, which is similar to that for a n-FET except that $V_{set} = V_{dd}$.

There are, however, several potential issues that may arise in this configuration. First, V_t measured by OP-based test structures may be impacted by body effect because of nonzero source voltage. For example, in the case of the NFET, if V_{ss} is grounded, then the bias current results in a small positive voltage at the DUT source terminal. If the DUT body is grounded, this results in body effect because of the positive voltage difference from source to body.

Although the impact of body effect may be less severe in silicon-on-insulator technologies such as those studied in [23], the impact may not be negligible in bulk silicon technology, which is most commonly used. Second, the DUT test structure used for V_t measurement must also be capable of measuring I_{on}, I_{off}, and additional key device parametrics (e.g., subthreshold slope, I_{dlin}, or other significant current points on the I–V characteristic such as the components of the I_{deff} metric of [25] or I_{dlin} at fixed gate overdrive used to decouple MOSFET channel and external resistance in [26]).

The circuit configuration of [23] could only be employed for V_t measurement and will be unable to measure other parametrics. Third, on-chip R_{load} variation can greatly compromise the accuracy of the V_t measurement, an issue that will become more severe in forthcoming advanced process technology nodes. Further, such a test circuit relies on an on-chip precision resistor, but the value of the precision resistor may also not be on target until the later stages of process development. The test program for this test structure must first characterize the precision resistor and then must adjust bias voltages accordingly. The fourth and final issue is the accuracy of the on-chip OP. In 0.35-μm technology, OP gain of 100 dB using a folded cascode OP is readily achieved, but in advanced technologies the low transistor output resistance and the aggressive power supply scaling from 3.5 V to below 1.5 V result in reduced headroom and thus significantly reduced OP gain. In addition, device mismatch is generally not well controlled in the early stages of process development. Therefore, the V_t measured by test structures using on-chip OPs can easily fail to accurately measure the true threshold voltage.

III. Design Methodology

A. OP-Based SMU for Fast V_t Measurement

As discussed in Section II-C, the reduced headroom in advanced process technologies might result in on-chip op-amp gain that is too low to achieve reliable V_t measurement. In addition, the voltage gain of an on-chip op-amp may significantly vary with transistor mismatch because of process variation, especially in advanced technologies below 65 nm. Rather than using an on-chip OP design, for the fast V_t measurement technique presented in this paper, we modify the

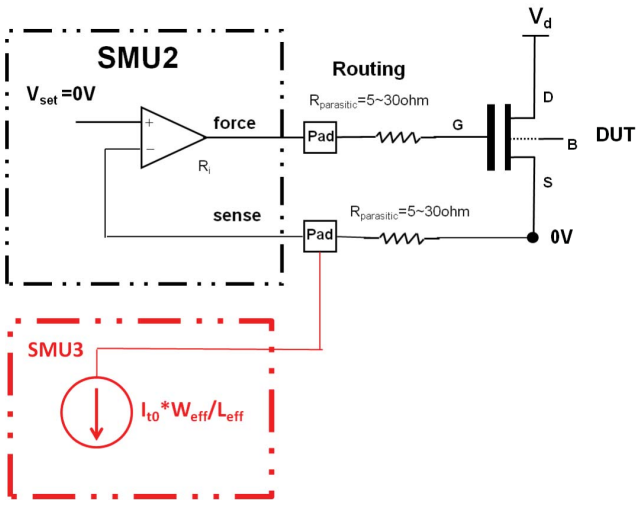

Fig. 9. Configuration of an OP-based SMU and a n-FET for V_t measurement with one force-measure iteration. The target current defined for V_t is forced as a negative current by an additional SMU.

configuration of the OP in the tester's SMU. Instead of the conventional unity-gain buffer configuration (e.g., as shown in Fig. 1), the SMU OP is connected as shown in Fig. 9 by separating the force and sense nodes and reconnecting the sense node to the DUT source node. In such a configuration, in contrast to the circuits of Fig. 1, SMU2 is no longer functioning as a unity-gain buffer at the gate terminal. Instead, in the proposed configuration, it is configured as a two stage operation amplifier, i.e., SMU2 plus DUT are connected to form a voltage follower. In addition, as the tester's SMU op-amp is constructed using discrete ICs, it can easily achieve very high-gain operation while remaining free from sensitivity to process variation. The overall gain of this two stage OP exceeds 100 dB. Therefore, the inverting input node and the noninverting input node can be considered connected by a virtual short. For the V_t measurement, V_{set} is 0 V, and the voltage at the source terminal is also forced to almost exactly 0 V because of the following two reasons. First, the op-amp's gain is high enough to enable the op-amp to effectively maintain the virtual short between the two op-amp input nodes. Second, the current (< 0.1 μA) flowing between sense pad and source node is small enough that the IR drop in this path has negligible impact. Meanwhile, SMU3 functions as the current source, forcing the negative target current used in the constant-current V_t definition, which flows completely through the DUT because of the high input impedance of the op-amp input terminals. Therefore, the output node of the op-amp is able to quickly drive the gate voltage to the correct value of V_t once V_{set}, V_d, V_b, and the target current for the constant current V_t definition are assigned. V_t can be measured in either the saturation or the linear region by appropriately adjusting V_d. Typically, $V_d = V_{dd}$ and $V_d = 0.05$ V are the bias conditions for saturation-mode V_t (V_{ts}) and linear-mode V_t (V_{tl}), respectively. This configuration affords several advantages. First, this configuration has high V_t measurement accuracy. The accuracy is better than the binary search approach because there is almost no error in the target current that is forced by a second SMU. The second benefit of

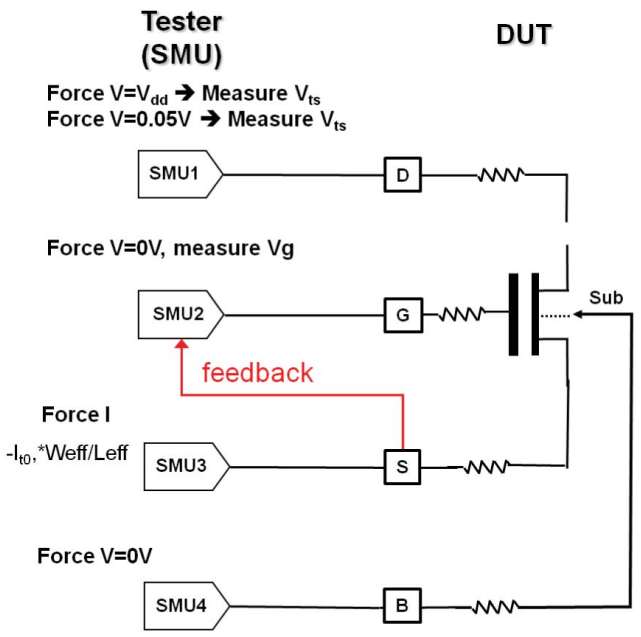

Fig. 10. SMU connections for fast V_t measurement by using the proposed OP-based SMU.

this OP-based SMU approach is the absence of body effect in V_t measurement. The third benefit is that multiple additional device parametrics, such as I_{on}, I_{off}, and so forth, can be measured in this configuration. For the V_t measurement, note that we deliberately avoid connecting the current source to the DUT drain terminal, because a less accurate V_t value would result from connection to the drain because of an extra junction leakage current path that would remove part of the reference current $I_{\text{ds}}\ (V_t) = I0, n^* W_{\text{eff}}/L_{\text{eff}}$.

B. Implementation for Stand-Alone DUT

Fig. 10 shows the SMU connections for fast V_t testing using an OP-based SMU. Other than the OP-based SMU2 connected to the gate and source terminals, there are two unity-gain buffers for the drain and bulk terminals, and one current source for the source terminal. SMU2, configured with separated force and sense nodes, is connected to both the gate and source terminals of the DUT. The drain and bulk terminals are connected to SMU1 and SMU4, respectively, and the negative current (i.e., target current) source is provided by SMU3. The body effect issue faced by on-chip OP test structures is completely eliminated in this test configuration. Four SMUs are required for the fast V_t measurement, the same number required by the binary search algorithm. As the OP-based SMU can read out the output voltage of the OP, there is no need for an additional SMU to sense the voltage at the gate terminal as required in the circuit of Fig. 8. Fig. 11 shows the fast V_t algorithm to obtain V_t with only a single force-measure iteration. Note that the voltages at each terminal must be forced in the sequence shown, i.e., first drain, then bulk, then gate, and lastly the negative current should be forced at the source. If this forcing sequence is not strictly observed, the voltage overshoot might damage or breakdown the DUT.

```
0.  set_force_limit(smu2,gate,0V,Vd)
1.  connect(smu1,drain);
2.  connect(smu2,gate,source);
3.  connect(smu3,source);
4.  connect(smu4,bulk);

5.  Itarget=It0*Weff/Leff

6.  Force_V(Drain, Vd);
7.  Force_V(Bulk, Vb);
8.  Force_V(Gate, 0V);
9.  Force_I(Source,Itarget)
10. Measure_V(Gate, Vth)
```

Fig. 11. Pseudocode of V_t measurement by OP-based SMU.

C. Implementation for Array Test Structure V_t Measurement

Although transistor characterization during technology development and manufacture monitoring requires the characterization of a number of stand-alone DUTs, because of the increasing importance of LDEs, it is increasingly challenging to adequately characterize a technology with a limited number of stand-alone DUT layouts. The typical width and length (W/L) matrix required for basic SPICE modeling may contain several tens of individual DUTs, but when multiple LDEs such as well-proximity effect and various stress-dependent geometry effects must be characterized, hundreds or even thousands of DUT layouts must be studied. Such studies can be performed on discrete DUTs in a development environment on a test vehicle, but even with the reduction in test time enabled by our proposed method, the area required for such a large number of DUTs renders it unfeasible to monitor a large number of DUTs in a production environment because all test structures must fit within the limited space in the wafer scribe line. This challenge, however, can be addressed by placing multiple DUTs in an compact addressable array and accessing the individual DUTs via a multiplexer and transmission gates. The basic tradeoff between stand-alone DUTs and array-based structures is straightforward. Stand-alone DUTs can be accessed with relatively straightforward measures to address any possible parasitics, and all traditional transistor characteristics can be measured. However, even the most innovative pad sharing techniques can only place approximately 20 DUTs in a typical scribe-line test structure having dimensions approximately 2500 × 60 μm, and contacted directly by an automated tester probe card. In contrast array-based structures require substantially more design effort to eliminate parasitics, which may otherwise introduce measurement inaccuracy. Further, some parametrics, such as the very low off-state currents of long channel transistors, may be challenging or impossible to measure in array test structures. With appropriate design of access circuitry, however, array test structures can perform accurate measurements of most key parametrics, such as I_{dsat}, V_{tsat}, and many other key points on the I–V characteristic, and over a thousand DUTs can easily fit in a single scribe-line test structure. The design measures required to achieve optimal accuracy in array-based test structures, as well as the details of the array-based test structure employed in this paper, were discussed at greater length in [19]. As discussed

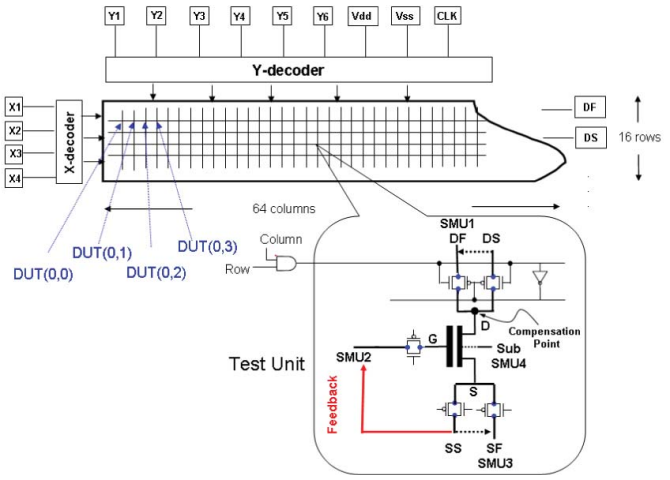

Fig. 12. V_t measurement by OP-based SMU in an array test structure.

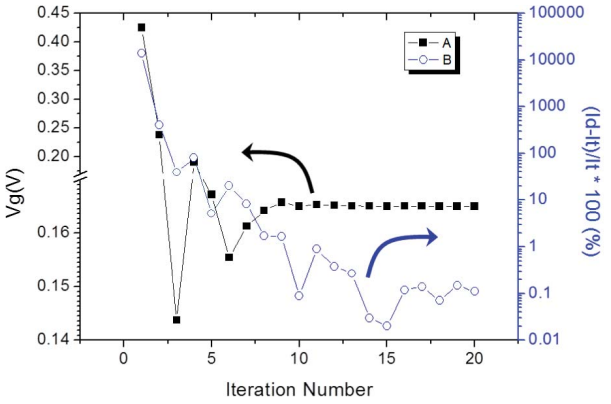

Fig. 13. Time trace of successive iterations for V_t measurement by binary search, showing gate voltage (left axis) and measured current matching percentage (right axis). I_d is the measured current at the drain node and I_t is the target current for V_t definition by the constant current criteria.

below, the test time reduction by our proposed test algorithm can be readily combined with array-based test structures to perform characterization of a large number of DUTs, which would otherwise be extremely challenging in a manufacturing environment because of prohibitively long test time. For this research, an addressable array containing multiple transistors with various values of W/L is used for the characterization of V_t variation.

Fig. 12 shows the proposed transistor array with $16 \times 64 = 1024$ test units. In-depth discussion of the design and operation of the array was discussed in [19], but its function is summarized in brief below. Each test unit consists of a few transmission gates and one DUT (a FET in this example). The DUT can be measured by selecting the corresponding test unit through the column decoder. As shown in Fig. 12, the gate terminals of the FETs in a selected column are connected to SMU2 and the source sense terminals are connected to SMU3, which is fed back to SMU2, while the switches connecting drain, source, gate, and bulk terminals in unselected columns are turned off. Typically, the transmission gates need to be sized large enough to have negligible voltage drop at the current level required for V_t measurement. In this experiment, however, the drain and source terminals of all DUTs are connected to one SMU with force/sense IR drop compensation, respectively. With this voltage compensation mechanism, wide metal routing for the drain and bulk terminals is not required to reduce the parasitic resistance of these connections, allowing a more compact testline layout. The V_t of the selected DUT is read out by SMU2. In addition, all periphery circuits, such as latches and decoders, are designed with 2.5-V I/O devices so that their background leakage current, including subthreshold leakage current and gate oxide leakage current, can be reduced, and their performance will not be affected by any process variation that may be present in the advanced process under research.

IV. Experimental Results

A. Binary Search V_t Testing Time

The time required for a single binary search force-measure iteration consists mainly of contributions from two stages in the execution of the algorithm: 1) the forcing of the voltage and 2) the current measurement. The time required to force a voltage is principally a function of the SMU settling time, which is relatively short, typically $\sim$100 μs. The time required for current measurement is determined by the current level to be measured and the sample size, which is defined by the integration time. This second contribution is strongly dependent on the magnitude of the target current if the integration time is set to the same value. For measurement of a lower current level, the SMU requires a longer measurement time because it must switch from the measurement mode for a higher current to that of a lower current. Typically, the time required for changing the current range a few ms because it requires the switching of electromechanical components in the tester.

In this experiment, it is determined to require approximately 7 and 30 ms for one force-measure iteration at the microampere and nanoampere current levels, respectively. As discussed in Section II-A, V_t is defined by the gate voltage resulting in the measured drain current matching the target current $I0^* W_{\text{eff}}/L_{\text{eff}}$ within a specified criteria, for instance 1%, which introduces about 0.5 mV error based on SPICE simulation. Fig. 13 (curve A) plots the gate voltage (V_g) versus iteration number throughout the successive force-measurement cycles of a V_t measurement by binary search. During the course of the measurement, V_g is set successively to values above and below V_t, approaching V_t with an increasingly tight tolerance, and converging when the drain current Id (measured by SMU1 in the connection scheme of Fig. 2) approximately matches the target current. Curve B plots the percent mismatch between the measured drain current and the target current, showing that typically nine or ten iterations are required to reach the 1% matching criteria.

To obtain representative V_t measurement times for the binary search algorithm, transistors of two different channel lengths are evaluated. Transistor A is a longer channel device with a target current in the nA range. Transistor B is a short channel device with a target current of order 1 μA. Table I lists the device characteristics and V_t testing times obtained using the binary search algorithm. The shorter channel transistor with microampere target current requires approximately 69 ms,

TABLE I
COMPARISON OF DEVICE CHARACTERISTICS AND TESTING TIME FOR V_t MEASUREMENT USING BINARY SEARCH FOR TWO DIFFERENT TRANSISTORS. DIFFERENT TEST TIMES RESULT MAINLY FROM THE DIFFERENT MAGNITUDES OF THE TARGET CURRENT

	Transistor A	Transistor B
Device size	Longer channel	Short channel
Target current	~ nA	~ μA
Average of testing time	270.06 ms	68.75 ms
Standard. dev of testing time	8.98 ms	20.83 ms
Iteration number	8–10	6–9

whereas the longer channel transistor requires a testing time of approximately 270 ms. The number of iterations required for measurement of the longer channel transistor is slightly higher than for the shorter channel transistor because of the inevitable noise increase from lower target current to be measured. Moreover, the testing time for the lower target current significantly increases by nearly 4× because of the additional time required for the SMU range to switch in order to accommodate the lower current level.

B. V_t Testing Time Improvement Using the Interpolation Method

According to the analysis in Section II-B, the V_t testing time using the interpolation method can be reduced to 60 and 14 ms for transistors A and B, respectively, because the interpolation method requires only two force-measure iteration cycles, compared with approximately 6–9 cycles for binary search.

Fig. 14 shows a scatter plot of V_t obtained from the binary search and interpolation methodologies for devices fabricated using an advanced process technology. Evidently the data obtained from these two methods exhibit excellent linearity even though the number of force-measure iterations is reduced to two by using the interpolation algorithm. In other words, the interpolation algorithm shows no degradation in the accuracy of the V_t measurement, but has a shorter testing time. As discussed in the previous section, the interpolation methodology is, however, only suitable for characterization of nearly identical transistor sizes having very similar target current values, and furthermore, these transistors must have no double hump or similar nonlinearities in their I_d–V_g characteristics.

C. Simulation of V_t Measurement Using OP-Based SMU

The configuration of Fig. 9 is verified by HSPICE simulations in an advanced process technology. In this simulation, a stand-alone DUT (nMOS) is directly connected to a high-gain op-amp with gain of approximately 100 dB. The bias condition of the gate, source, and bulk terminals is set as shown in Fig. 10 to emulate the test condition. To trace the voltage modulation at the gate terminal, the drain voltage is, however, swept from 0 V to V_{dd} rather than a fixed bias of 0.05 V or V_{dd} for V_{tl} or V_{ts} measurement. With the high-gain OP, the

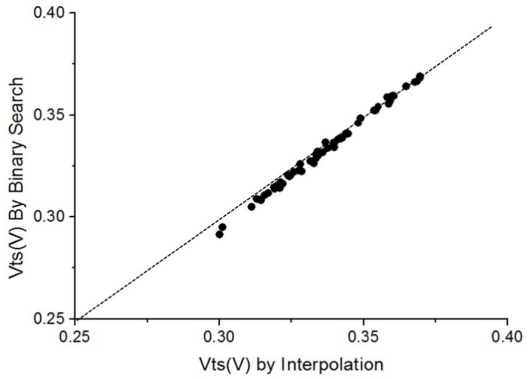

Fig. 14. Scatter plot of V_{ts} measurements by the binary search versus the interpolation method.

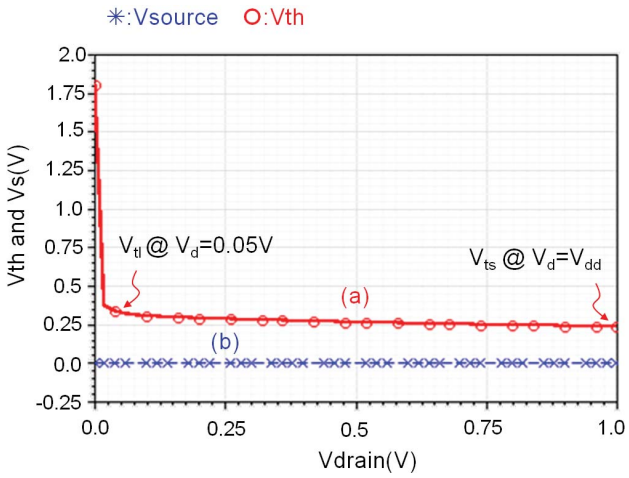

Fig. 15. Simulation of V_t measurement by an OP-based test structure. Plotted data are (a) OP output voltage, i.e., V_t and (b) DUT source voltage, which is clamped at 0 V because of virtual short to V_{set}.

voltage of the source terminal is clamped at 0 V by the virtual short with the OP noninverting input. Therefore, the absence of body effect in the V_t measurement in this configuration can be verified in simulation if the bulk terminal is also biased at 0 V. As plotted in Fig. 15, curve (a) shows that the voltage at the output node of the OP, i.e., V_t, is well modulated by a 10 mV change in the drain voltage. Curve (b), which represents the voltage at the source terminal, remains at 0 V for all values of the drain voltage, indicating that the inverting and noninverting inputs of the OP amp are a strong virtual short because the gain of the op-amp is sufficiently large. Therefore, by definition, the V_t in the saturation and linear regions can be measured by forcing $V_d = 0.05$ and $V_d = V_{dd}$ respectively, with no inaccuracy introduced by body effect.

The transient simulation for the validation of this array-based test structure is also checked. Fig. 16 shows the simulation waveform of DUT(0, 0) − DUT(0, 3) in the array-based test structure shown in Fig. 12. The voltage-modulated output signal is repeated periodically as the macro scans through the 1024 devices in the array, modulated by the clock period for address switching. These simulations demonstrate the repeatability of successive measurements and the time

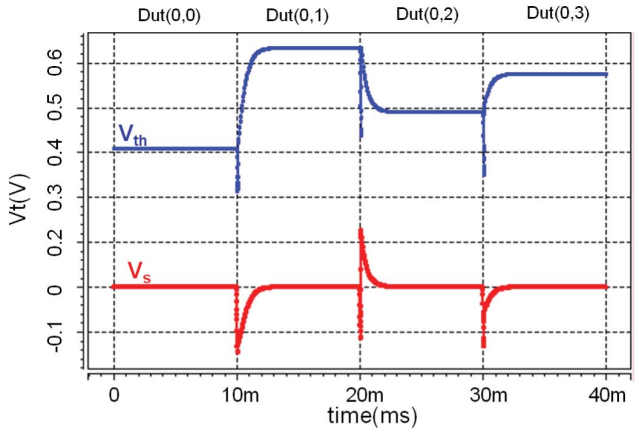

Fig. 16. Transient simulation of OP-based V_t measurement in an array-based test structure. Traces for the measurement of four DUTs are shown, where each DUT has a different threshold voltage.

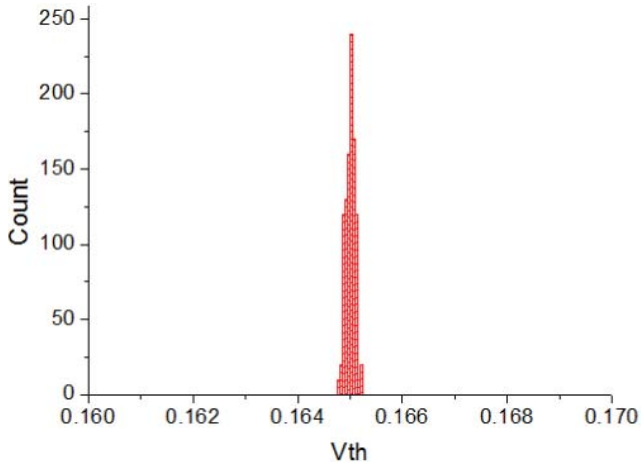

Fig. 17. V_t distribution obtained by 1000 repeated measurements on the same DUT (shorter channel transistor) by OP-based measurement of the array test structure.

stability of voltage levels between transitions. As indicated by the voltage trace of Fig. 12, although the specific V_t values of each of the four DUTs (DUT(0, 0) − DUT(0, 3)) are different, nearly identical settling time is achieved in each case. This indicates that the OP-based SMU can settle within a clock period of 2–3 ms with 1 pF parasitic capacitance.

This settling time does constitute a limitation to the speed of the OP-based measurement, but even with this settling time, because only a single iteration is required for convergence, the V_t measurement demonstrated here is a factor of $\sim$ 10 faster than that of the binary search algorithm (which requires $\sim$10 iterations to converge), and a factor of $\sim$ 2 faster than the interpolation method (which requires two iterations).

D. Stand-Alone DUT Test Result

The proposed OP-based V_t measurement method introduced in Section III-B delivers significant improvement in testing time and measurement accuracy. To demonstrate this, in this experiment, the measurement time and accuracy is evaluated for one of the DUTs fabricated using an advanced process technology. The V_t measurement by the proposed methodology is repeated 1000 times using an Agilent parametric tester to ensure the statistical significance of the result. As shown by the histogram in Fig. 17, the V_t value obtained by the OP-based methodology has a very small measurement error that can contribute to better measurement accuracy.

The standard deviation of the 1000 V_t measurements is approximately 0.15 mV, much smaller than the 0.5 mV error resulting from the 1% current matching criteria discussed in Section IV-A. In addition, the test time is significantly reduced from $\sim$ten force-measure iterations to one, i.e., from $\sim$60 to $\sim$6 ms for the short-channel transistor A of Table I, which is expected based on the discussion in Section III-A. The major reason for this improvement in testing time is the use of only a single force-measure iteration. Improved measurement accuracy is further ensured by precise setting of the target current and the absence of impact of imperfections and variability of an on-chip OP design, which may occur in an on-chip OP approach such as [23].

E. Array-Based Test Structure Result

The test speed improvement of OP-based V_t measurement is most significant in array-based test structures. In addition, to the test time savings from reducing $\sim$10 force-measure iterations to one, the array-based test structure avoids the time required for the connect and disconnect operations between SMUs and testline I/O pads for measurement of successive DUTs that must be performed before the force-measure iterations can begin. Typically, the time required for connect and disconnect operations, which are performed by mechanical switches, is about 1 ms. The time required for changing and latching addresses for DUT selection in array-based test structures is, however, less than 1 μs that is much faster than the connect and disconnect mechanical operations. In practice, for array-based test structure measurement, connection between SMU and pad is performed at the first address and disconnection is performed at the last address because the same SMUs are used for the force and sense terminals of all DUTs. Moreover, the testing time overhead can be further improved in array-based test structure by elimination of prober index time. In general, the prober index time is typically a few hundred ms if the required prober chuck displacement is less than 1 mm. In this experiment, a test time comparison is performed between (A) nonarray-based test structures and (B) array-based test structure. Both cases include $\sim$1 k DUTs with different W/L combinations. In case (A), nonarray test structures, however, required more a larger number of testlines and thus more layout area. Typically, only eight DUTs can be placed in one nonarray testline due the constraint that DUTs must not have excessive sharing of I/O pads. Therefore, 1 k DUTs requires $1000/8 = 125$ testlines in case (A). The V_t of each DUT is measured by the proposed methodology under two different test conditions: 1) nonarray DUTs in case A, which require a SMU connect and disconnect for each individual DUT and 2) an array-based test structure in case (B), which only requires a connect and disconnect operation of the first and last addresses, respectively. As shown in Table II, the time required specifically for the $\sim$1 k DUT V_t measurements is approximately 6000 ms for both cases (A)

TABLE II
TEST TIME COMPARISON OF OP-BASED V_t MEASUREMENT BETWEEN STAND-ALONE DUT AND ARRAY-BASED DUT

	(A) Nonarray DUT	(B) Array-Based DUT
Only measurement	$\sim$ 6000 ms	$\sim$ 6000 ms
Connect and disconnect	$\sim$ 1000 ms	$\sim$ 2 ms
Prober index time	$\sim 1000/8 \times 200$ ms	0 ms
Total testing time	$\sim$ 32 000 s	$\sim$ 6002 ms

and (B). However, case (A) it requires additional overhead of 1000 ms from SMU connect and disconnect operations. Moreover, case A utilizes 125 probe card touch downs instead of the single touch down of case (B). Therefore, case (A) requires 125 prober chuck displacements during measurement. Assuming a prober index time of 200 μs, case (A) incurs an additional penalty of approximately 125×200 ms are required for case (A). Therefore, the total test time is approximately 32 000 and 6002 ms for the proposed V_t measurement on nonarray and array-based test structures, respectively. The test speed is further improved by factor of 5$\times$ by taking advantage of a single connect/disconnect and elimination of the prober index time during measurement of the array-based test structure.

V. CONCLUSION

In this paper, we successfully developed a fast V_t testing methodology using an OP-based SMU to dramatically improve the test time required for V_t measurement. Using the proposed techniques, the V_t testing speed can improved by a factor of 5–10 relative to the binary search algorithm (the algorithm most commonly used in the authors' experience), and by a factor of $\sim$2 relative to the interpolation algorithm, with accuracy better than 0.15 mV (compared with $\sim$0.5 mV typically achieved by the binary search or interpolation algorithms). In addition, combined with a array-based test structure design including $\sim$1 k individually addressable FETs, the test time of V_t measurements can be further improved by a factor of 5$\times$ because of elimination of overhead due to multiple tester connect and disconnect operations and prober index times. A series of experiments were conducted on both mature and newly developed process technologies to validate the effectiveness and the superiority of the overall proposed test structure and its application.

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