Fabrication of tri-gated junctionless poly-Si transistors with I-line based lithography

2014 Jpn. J. Appl. Phys. 53 04EA01

(http://iopscience.iop.org/1347-4065/53/4S/04EA01)

Japanese Journal of Applied Physics **53**, 04EA01 (2014) **REGULAR PAPER**
http://dx.doi.org/10.7567/JJAP.53.04EA01

Fabrication of tri-gated junctionless poly-Si transistors with I-line based lithography

Cheng-I Lin[1], Ko-Hui Lee[1], Horng-Chih Lin[1,2*], and Tiao-Yuan Huang[1]

[1]*Department of Electrical Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan 300, R.O.C.*
[2]*National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.*
E-mail: hclin@faculty.nctu.edu.tw

Received September 9, 2013; accepted November 11, 2013; published online February 17, 2014

In this work, we have successfully demonstrated the feasibility of a method, which relies solely on I-line-based lithography, for fabricating sub-100 nm tri-gated junctionless (JL) poly-Si nanowire (NW) transistors. This method employs sidewall spacer etching and photoresist (PR) trimming techniques to shrink the channel length and width, respectively. With this approach, channel length and width down to 90 and 93 nm, respectively, are achieved in this work. The fabricated devices exhibit superior device characteristics with low subthreshold swing of 285 mV/dec and on/off current ratio larger than 10^7. © 2014 The Japan Society of Applied Physics

1. Introduction

Scaling of the gate length in conventional metal–oxide–semiconductor field effect transistor (MOSFET) demands ultra-shallow and abrupt source/drain (S/D) junctions[1] in order to boost the immunity against short-channel effects.[2,3] The reduction in gate length weakens the gate controllability over the channel potential. To circumvent this issue, new device architectures employing a multi-gated configuration together with ultra-thin or nanowire (NW) channels[4–10] have been proposed and widely explored. Recently, junctionless (JL) transistors[11–13] emerged as another feasible approach in nanometer-scale device applications. The JL scheme can reduce parasitic series resistance and eliminate issues associated with junction formation process encountered in the fabrication of extremely down-scaled MOSFETs[14] and three-dimensional (3D) stackable electronics.[15–17] The JL scheme is especially beneficial for the fabrication of NAND Flash memory devices with 3D architecture,[18] whose S/D doping process is difficult to accomplish with the conventional implantation technique. For the 3D architecture, JL devices are often built with poly-Si materials.[19–21] Taking the advantage of mature low-pressure chemical vapor deposition (LPCVD) and in situ doping technique, poly-Si-based JL transistors exhibit great potential for construction of future 3D electronics. To realize the device technology, the study of the nanometer-scale JL devices, like short-channel effects, reliability, and noise characteristics, is important.

As compared with traditional inversion-mode (IM) and accumulation-mode (AM) devices, the JL device is quite different in terms of architecture and conduction mechanism. For the IM device, an inversion layer is formed near the surface of the channel region as it is turned on, while in the JL device the conduction is mainly through the inner channel. The AM transistor bears some resemblance to the JL device in that the doping type of the substrate is the same as that of S/D in both cases. Nonetheless, the doping concentration is typically in the order of $10^{17}\,cm^{-3}$ which is much less than that of the S/D. As the AM device is turned on, the conduction is through a surface accumulation layer, rather than the inner channel as the JL device does.

Owing to the high carrier concentration ($>10^{19}\,cm^{-3}$) in the channel of JL devices, adoption of NW channels is essential to achieve good switching behavior as the channel length of the JL devices is scaled into the nanometer regime. For this purpose, costly deep UV[14] or e-beam writers[22] were usually employed in the device fabrication. For academic studies conducted on campuses, patterning of sub-100 nm dimensions usually relies on e-beam lithography with an extremely low throughput. In this work, based solely on I-line-based lithography, we proposed a method which employs spacer etching[23] and photoresist (PR) trimming techniques to shrink the channel length and width, respectively, of the JL devices down below 100 nm. The approach provides a useful alternative which is far more efficient than the conventional e-beam scheme for fabrication of nano-scale devices.

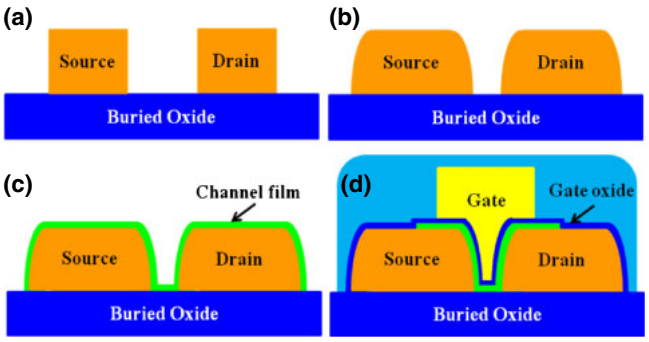

Fig. 1. (Color online) Illustration of process flow for fabricating the JL devices.

2. Device structure and fabrication

The main process steps for fabricating the short-channel tri-gated JL NW transistors are illustrated in Figs. 1(a)–1(d). First, a 200-nm-thick buried oxide layer was grown on the Si wafer. Next, a 180-nm-thick in situ doped n^+ amorphous Si layer was deposited by LPCVD system, followed by patterning with I-line-based lithography and subsequent anisotropic etching to form two isolated islands, as shown in Fig. 1(a). Afterwards another 150-nm-thick in situ phosphorus-doped n^+ amorphous Si layer was deposited and etched anisotropically to form sidewall spacers abutting the islands. After this step, the upside-down bowl-shaped studs (island plus spacer) were formed and later served as source and drain regions, as shown in Fig. 1(b), while a shrunk channel length (defined as the distance between the two studs) well below the limit of the lithography (~0.35 μm) could be readily achieved. Afterwards, an 11-nm-thick in situ doped n^+ amorphous Si layer was deposited to serve as the

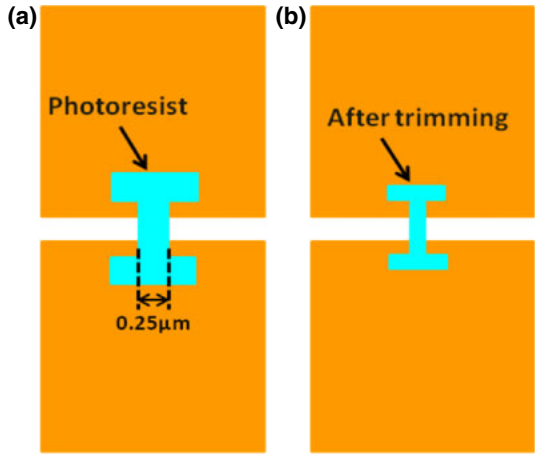

Fig. 2. (Color online) Illustration of the PR pattern (a) before, and (b) after PR trimming.

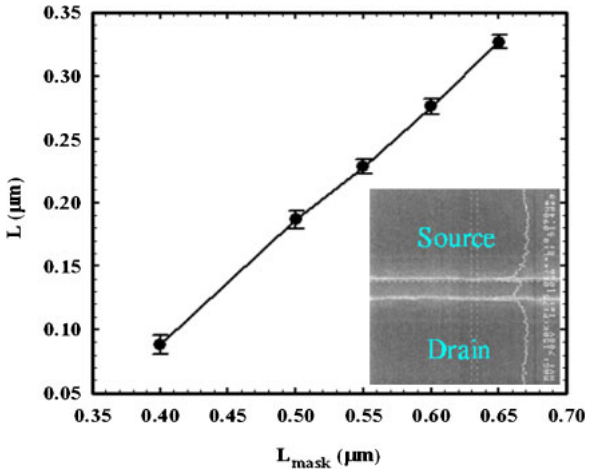

Fig. 3. (Color online) Measured channel length (L) after formation of sidewall spacers as a function of the designed length (L_{mask}) in the mask. The inset shows the SEM image of a JL transistor with L of 90 nm.

channel layer, as shown in Fig. 1(c), followed by a solid phase crystallization process at 600 °C in N_2 ambient for 24 h to transform the amorphous Si into poly-Si. Next, in order to narrow the channel width, PR trimming method was employed to shrink the width of the channel. As illustrated in Fig. 2(a), with an intentional over-exposure, the original width of the narrowest PR pattern generated with an I-line based stepper was 0.25 μm. The PR patterns were further slimmed down with an O_2 plasma, and the resultant pattern is shown in Fig. 2(b). Note that the combination of this technique with the aforementioned spacer etching makes it feasible to realize sub-lithographic channel dimensions. After the channel patterning, an 11-nm-thick tetraethoxysilane (TEOS) oxide layer was deposited by LPCVD to serve as the gate oxide, followed by the deposition of a 150-nm-thick in situ doped n^+ amorphous Si layer and then patterned to form the gate electrode. A 300-nm-thick TEOS oxide layer was then deposited to passivate the devices, as shown in Fig. 1(d). Next, after forming the contact holes through the passivation oxide, standard metallization steps were performed to form the test pads.

3. Results and discussion

3.1 Inspection of the resultant patterns

Figure 3 displays the channel length (L) measured by in-line scanning electron microscopy (SEM) after sidewall spacer formation as a function of the nominal channel length designed in the mask (L_{mask}). The measured channel length of the JL device is defined as the distance between the source and the drain studs. The inset in Fig. 3 is the SEM image showing a device with L of 90 nm. These measured results are obtained from 32 devices located in different dies distributed on a six-inch wafer. A linear relation between L and L_{mask} is observed, and L_{mask} designed in the mask can be shrunk averagely by 0.32 μm in the fabricated devices. Moreover, it is confirmed that L can be easily scaled down to 90 nm with good uniformity by the sidewall spacer technique.

Next, the formation of the trimmed channel is explored. Figures 4(a) and 4(b) show the top SEM images of devices with PR pattern of the channel before and after trimming treatment. Note that the designed channel width in this case is 0.4 μm. An intentional overexposure condition was performed to downsize the PR pattern to 0.25 μm [Fig. 4(a)], and then the PR trimming was employed to further shrink the dimension to around 90 nm [Fig. 4(b)]. Although the PR is attacked and etched off in an O_2 plasma environment during the trimming treatment, the resultant pattern remains sharp and in good shape. Figures 5(a) and 5(b) show top-view SEM images of devices with L of 90 nm and 0.5 μm, respectively, taken after anisotropic poly-Si etching and stripping-off of the PR. The horizontal AB line shown in Fig. 5(b) illustrates the direction perpendicular to the channel. As shown in the SEM images, the planar width (W) of the etched poly-Si channels is 93 nm, which is basically the same as that of the trimmed PR.

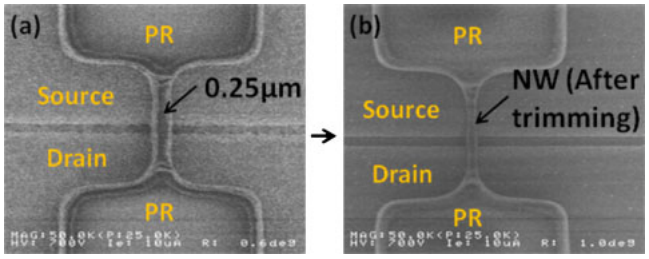

Fig. 4. (Color online) Top view of SEM image of a PR channel pattern (a) before and (b) after the trimming treatment. L of the device is 90 nm.

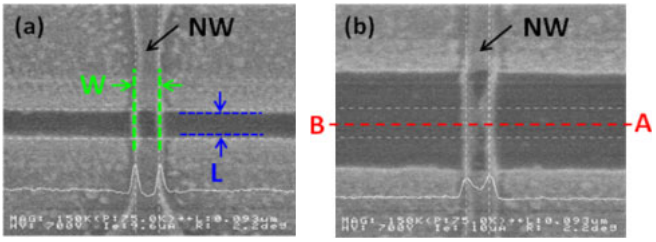

Fig. 5. (Color online) Top-view SEM images of NW channels connecting between source and drain regions with channel length of (a) 90 nm and (b) 0.5 μm. The PR patterns have been stripped off and the planar widths of the NW are 93 nm.

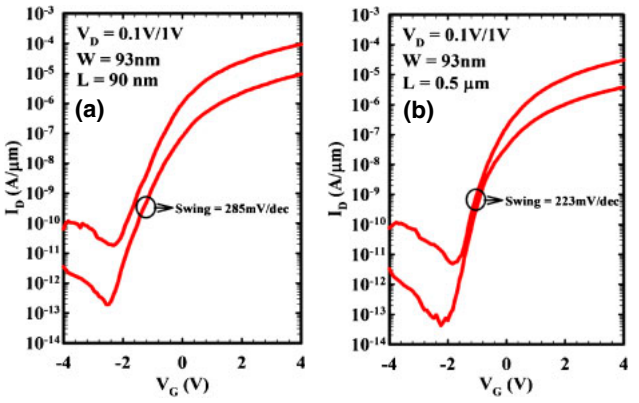

Fig. 6. (Color online) Transfer curves of JL devices with L of (a) 90 nm, and (b) 0.5 μm.

3.2 Electrical characteristics

Transfer characteristics of the fabricated JL transistors with W of 93 nm, and L of 90 nm and 0.5 μm, respectively, are displayed in Figs. 6(a) and 6(b). With the nanowire-scale channel achieved by the PR trimming technique, acceptable subthreshold characteristics can be retained even as the channel length is scaled to the nanometer regime. Figures 7(a) and 7(b) show the output characteristics of the JL devices with channel length of 90 nm and 0.5 μm, respectively. From the figures it is reasonable to see that the drain current increases as L is reduced. However, as L is downscaled to 90 nm, the large S/D resistances significantly affect the characteristics of the device, as shown in Fig. 7(a), despite the use of raised S/D structure in the present scheme. One of the reasons responsible for the high series resistance is the existence of a native oxide layer between different deposited poly-Si layers.[24] Further refinement and modification in S/D formation process, like the implementation of silicidation, can be adopted to address and resolve this issue.[25]

As compared with the device of 0.5 μm in channel length [Fig. 6(b)], it is seen that the subthreshold swing and drain-induced barrier lowering (DIBL) of the short-channel device [Fig. 6(a)] are degraded as a result of short-channel effects. That is, the penetration of electric field from the drain side into the channel has drawn an impact on the gate controllability. However, the JL device with L of 90 nm still shows good device performance with high I_{on}/I_{off} ratio ($>10^7$) and acceptable subthreshold swing (285 mV/dec).[18,26] In the devices, W (93 nm) and the channel thickness (11 nm) are both in the nanometer regime and thus the channel potential can be more tightly controlled by the gate bias. To highlight this point, Fig. 8 shows and compares the transfer characteristics of JL device with W of 93 nm, 0.2 μm, and 0.5 μm. In the figure, the drain current has been normalized to the effective channel width (W_{eff}), i.e., W plus two times of the film thickness of the channel. From the comparison it is obvious that the degradations in subthreshold swing and DIBL become more noticeable with increasing W. Shrinkage of the channel width transforms the gated configuration from planar-like to tri-gated scheme, thus the immunity to short-channel effects is promoted.[27]

Another interesting observation in Fig. 8 is that the off-state leakage as the gate voltage is smaller than −3.5 V is essentially independent of the channel width. Since the

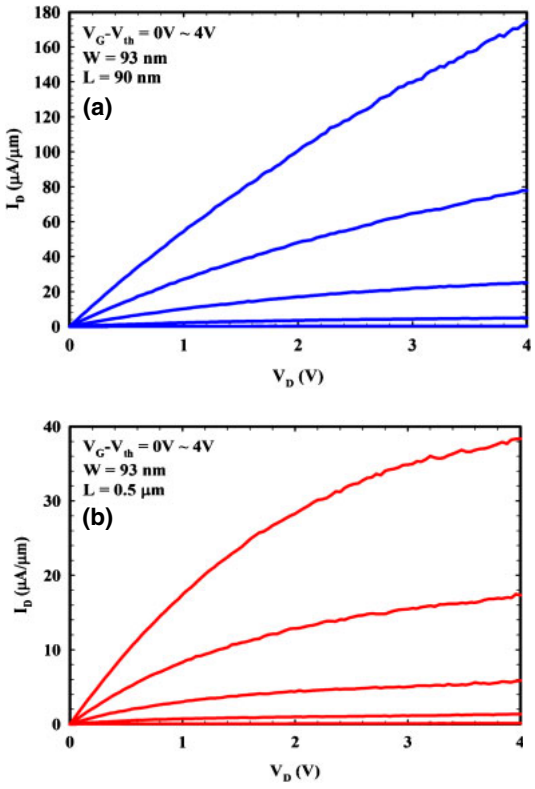

Fig. 7. (Color online) Output curves of JL devices with planar width of 93 nm and L of (a) 90 nm, and (b) 0.5 μm.

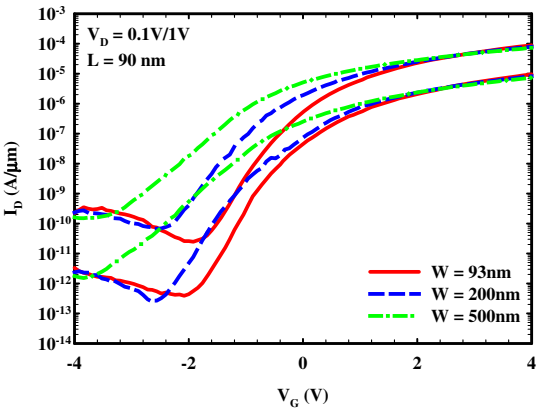

Fig. 8. (Color online) Transfer characteristics of fabricated JL transistors with different W of 93, 200, and 500 nm.

channel formation is done after the S/D spacer formation in the proposed scheme, the spacer etching would not damage the channel. From the above observation, it is further confirmed that the channel etching process indeed induces negligible damages on the sidewalls of the channel. Figure 9 shows the threshold voltage and subthreshold swing as a function of planar width at a drain bias of 0.1 V. Noteworthy is that the subthreshold swings of these devices are improved with smaller channel width, owing to better gate controllability. With a reduction in channel width, the shrinkage of the cross-sectional area through which the carriers transport facilitates complete carriers depletion in the channel by the gate to turn off the device. The threshold voltage is defined as the gate voltage when the drain current reaches $(W_{eff}/L) \times 10^{-9}$ (A). It can be seen in the figure that the threshold

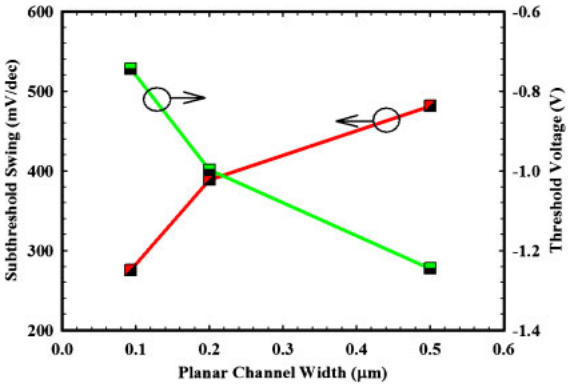

Fig. 9. (Color online) Subthreshold swing and threshold voltage as a function of planar channel width.

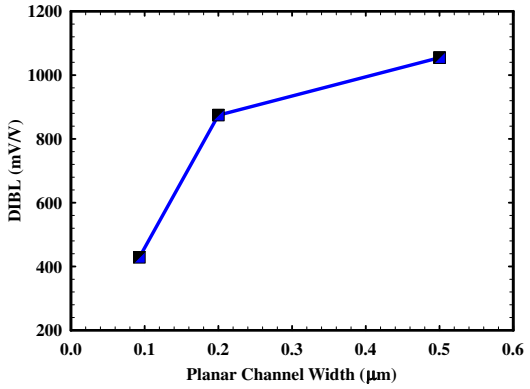

Fig. 10. (Color online) DIBL as a function of channel width.

voltage shifts positively and significantly as W is downscaled from 0.2 μm to 93 nm. In other words, the reduction in the channel width effectively helps the threshold voltages become more positive and serve as a well-behaved switching voltage. The scheme of tri-gated NW substantially promotes the device characteristics as compared with the planar transistors. Figure 10 shows the DIBL as a function of planar width for JL devices. It is observed that the DIBL effect is relieved with decreasing channel width. Especially for the device with channel width of 93 nm, the DIBL is significantly improved. This is again attributed to the enhancement of strong electrostatic gate controllability from the gate electrode as the channel width is reduced.

4. Conclusion

In this work, a simple method based solely on I-line-based lithography is proposed and has been successfully developed for fabricating short-channel tri-gated JL poly-Si NW transistors. This scheme employs the sidewall spacer etching to shrink the channel length of the tri-gated JL NW devices. PR trimming technique is subsequently implemented to narrow down the channel width of the devices. In situ doped n^+ amorphous Si layers deposited by LPCVD were employed in the construction of the devices. This work demonstrates that W and L of the fabricated JL devices can be readily scaled down to 93 and 90 nm, respectively, with good uniformity. With the aggressively narrowed channel width, the immunity to the short-channel effects for the nanometer-scale JL devices can be effectively promoted. Although the process conditions are not optimized yet, the fabricated devices exhibit good electrical characteristics in terms of acceptable subthreshold slope and high on/off current ratio.

Acknowledgments

The devices characterized in this work were fabricated in the Nano Device Laboratories (NDL). This work was sponsored in part by the National Science Council, Taiwan, under Grant NSC-102-2221-E-009-133, and NCTU-UCB I-RiCE program under Grant NSC-102-2911-I-009-302, and the Ministry of Education in Taiwan under ATU Program.

1) D. Pham, L. Larson, and J. W. Yang, Proc. Int. Workshop Junction Technology, 2006, p. 73.
2) Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S. J. Wind, and H.-S. Wong, Proc. IEEE **85**, 486 (1997).
3) C. Hu, Proc. IEEE **81**, 682 (1993).
4) H.-H. Hsu, T.-W. Liu, L. Chan, C.-D. Lin, T.-Y. Huang, and H.-C. Lin, IEEE Trans. Electron Devices **55**, 3063 (2008).
5) H.-C. Lin, W.-C. Chen, C.-D. Lin, and T.-Y. Huang, IEEE Electron Device Lett. **30**, 644 (2009).
6) X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, IEDM Tech. Dig., 1999, p. 67.
7) N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, W.-C. Lee, T.-J. King, J. Bokor, and C. Hu, IEEE Electron Device Lett. **22**, 487 (2001).
8) M. Im, J.-W. Han, H. Lee, L.-E. Yu, S. Kim, C.-H. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y.-K. Choi, IEEE Electron Device Lett. **29**, 102 (2008).
9) J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, IEDM Tech. Dig., 1990, p. 595.
10) J.-P. Colinge, *Physics of Semiconductor Devices* (Springer, New York, 2008).
11) J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. **5**, 225 (2010).
12) C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Appl. Phys. Lett. **94**, 053511 (2009).
13) R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, IEEE Electron Device Lett. **32**, 1170 (2011).
14) S. Barraud, M. Berthome, R. Coquand, M. Casse, T. Ernst, M.-P. Samson, P. Perreau, K. K. Bourdelle, O. Faynot, and T. Poiroux, IEEE Electron Device Lett. **33**, 1225 (2012).
15) H.-C. Lin, Z.-M. Lin, W.-C. Chen, and T.-Y. Huang, IEEE Trans. Electron Devices **58**, 3771 (2011).
16) H. Wang, M. Chan, S. Jagar, Y. Wang, and P. K. Ko, IEEE Electron Device Lett. **21**, 439 (2000).
17) E.-K. Lai, H.-T. Lue, Y.-H. Hsiao, J.-Y. Hsieh, C.-P. Lu, S.-Y. Wang, L.-W. Yang, T. Yang, K.-C. Chen, J. Gong, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, IEDM Tech. Dig., 2006, p. 41.
18) H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S. P. Hong, M. T. Wu, F. H. Hsu, N. Z. Lien, S.-Y. Wang, J.-Y. Hsieh, L.-W. Yang, T. Yang, K.-C. Chen, K.-Y. Hsieh, and C.-Y. Lu, Symp. VLSI Technology Dig. Tech., 2010, p. 131.
19) C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin, and T.-S. Chao, IEEE Electron Device Lett. **32**, 521 (2011).
20) H.-C. Lin, C.-I. Lin, and T.-Y. Huang, IEEE Electron Device Lett. **33**, 53 (2012).
21) H.-C. Lin, C.-I. Lin, Z.-M. Lin, B.-S. Shie, and T.-Y. Huang, IEEE Trans. Electron Devices **60**, 1142 (2013).
22) H. B. Chen, Y. C. Wu, C. Y. Chang, M. H. Han, N. H. Lu, and Y. C. Cheng, IEDM Tech. Dig., 2012, p. 232.
23) K.-H. Lee, H.-C. Lin, and T.-Y. Huang, IEEE Electron Device Lett. **34**, 720 (2013).
24) S. L. Wu, C. L. Lee, and T. F. Lei, IEEE Trans. Electron Devices **43**, 303 (1996).
25) J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T.-J. King, and C. Hu, IEDM Tech. Dig., 2000, p. 57.
26) S. Uchikoga, MRS Bull. **27**, 881 (2002).
27) B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, IEEE Electron Device Lett. **24**, 263 (2003).