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Effect of annealing processes on the electrical properties of the atomic layer deposition $Al_2O_3/In_{0.53}Ga_{0.47}As$ metal oxide semiconductor capacitors

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The influence of different annealing processes including post deposition annealing (PDA) and post metallization annealing (PMA) with various temperatures (250–400 °C) and ambient [N_2 and forming gas (FG)] on the electrical characteristics of $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs are systemically studied. Comparing to samples underwent high PDA temperature, the higher leakage current has been observed for all of samples underwent high PMA temperature. This has resulted in the degradation of capacitance–voltage (*C–V*) behaviors. In conjunction with the current–voltage (*J–V*) measurement, depth profiling Auger electron spectroscopy (AES) and high-resolution transmission electron microscopy (HRTEM) analyses evidence that the out-diffusion of metal into oxide layer is the main source of leakage current. The noticeable passivation effect on the Al_2O_3/InGaAs interface has also been confirmed by the samples that underwent PDA process. © 2014 The Japan Society of Applied Physics

1. Introduction

Among a variety of III–V compound semiconductors, $In_xGa_{1-x}As$ is one of the most potential candidates for high mobility channel in the future complementary metal–oxide–semiconductor (CMOS) technology.[1,2] However, the inherent poor quality of high-*k*/III–V semiconductor interface is still a critical issue that needs to be overcome. Great efforts have been focused on reducing typically high trap density at the interface between high-*k* materials and III–V semiconductor layer and some solutions were proposed in the literature such as interfacial passivation layer,[3–6] atomic layer deposition (ALD) of high-*k* layers,[7–16] chemical surface treatment,[17–19] or in-situ "self-cleaning" effect of trimethylaluminum (TMA).[20–22] Furthermore, forming gas annealing (FGA) was also reported in passivation both oxide border traps and interface defects which resulted in significant reduction of interface trap density (D_{it}).[23–25] Recently, Hu et al. reported on the special benefits of using FGA process to improve Al_2O_3/InGaAs interface quality and the leakage current.[26] In this work, the densification of oxide layer when samples were post metallization annealed at high temperature was found to be a root cause of high gate leakage current.[26] To verify this claim, we have designed a series of experiments with various annealing processes including post deposition annealing (PDA) and post metallization annealing (PMA) on the Al_2O_3/InGaAs structure. The results show that samples with high PDA- but low PMA-temperature exhibit good capacitance–voltage (*C–V*) behavior and low gate leakage current. On the other hand, samples with high PMA temperature reveal very high leakage current regardless of annealing in N_2 or FG ambient. In conjunction with depth profiling Auger electron spectroscopy (AES) and high-resolution transmission electron microscopy (HRTEM) analyses, we come to a conclusion that the diffusion of gate metal into oxide layer at high annealing temperature is the most likely origin of higher leakage current in Al_2O_3/InGaAs structure.

2. Experiment

The wafers used in this study were solid source molecular beam epitaxial grown 100 nm n-$In_{0.53}Ga_{0.47}As$ layer ($5 \times 10^{17}/cm^3$ doping) on n^+-InP substrates. Prior to surface treatment, the samples were degreased in acetone and isopropanol at room temperature. The HCl treatment was used as chemical surface passivation by dipping samples in HCl : H_2O (1 : 10) solution for 2 min followed by rinsing in deionized (DI) water. After drying with blowing N_2, the samples were loaded into ALD chamber (Cambridge NanoTech Fiji-202 DCS) for Al_2O_3 deposition. The in-situ TMA pretreatments was done by applying ten cycles of TMA/Ar (half an ALD cycle) followed by the growth of 90 cycles of Al_2O_3 films. During both TMA pretreatment and deposition processes, the substrate temperature was kept at 250 °C. After oxide deposition, two series of samples with different annealing processes were performed as described in Table I. In PDA series, samples were annealed with PDA process at 400 °C in N_2 or in FG for 5 min followed by gate metal and back side ohmic contact depositions and finished with PMA at low temperature of 250 °C in N_2 for 30 s. Samples of PMA series were deposited with gate metal and back side ohmic contact right after oxide deposition and followed by PMA at 300 °C, 350 °C, 400 °C in N_2 or 400 °C in FG for 5 min. The gate and back side ohmic metals were formed with electron beam evaporation of Pt and Au/Ge/Ni/Au, respectively.

Table I. List of samples with annealing processes of different ambient and annealing temperatures.

Sample	PDA process	Gate metal	Backside Ohmic	PMA process
PDA-400-N_2	400 °C in N_2 for 5 min	Pt	Au/Ge/Ni/Au	250 °C in N_2 for 30 s
PDA-400-FG	400 °C in FG for 5 min	Pt	Au/Ge/Ni/Au	250 °C in N_2 for 30 s
PMA-300-N_2	N/A	Pt	Au/Ge/Ni/Au	300 °C in N_2 for 5 min
PMA-350-N_2	N/A	Pt	Au/Ge/Ni/Au	350 °C in N_2 for 5 min
PMA-400-N_2	N/A	Pt	Au/Ge/Ni/Au	400 °C in N_2 for 5 min
PMA-400-FG	N/A	Pt	Au/Ge/Ni/Au	400 °C in FG for 5 min

3. Results and discussion

The *C–V* and current density–voltage (*J–V*) characteristics

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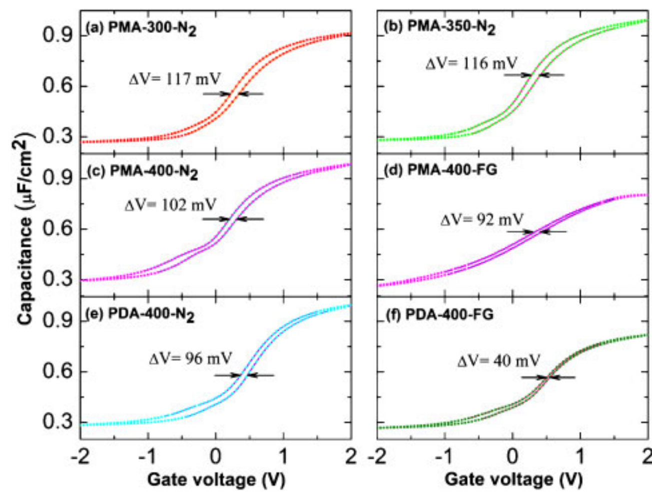

Fig. 1. (Color online) Bidirectional C–V characteristics of samples measured at a frequency of 1 MHz. (a) PMA at 300 °C in N_2 for 5 min. (b) PMA at 350 °C in N_2 for 5 min. (c) PMA at 400 °C in N_2 for 5 min. (d) PMA at 400 °C in FG for 5 min. (e) PDA at 400 °C in N_2 for 5 min. (f) PDA at 400 °C in FG for 5 min.

were conducted by using an HP4284A LCR meter and a Keithley 4200 semiconductor analyzer system, respectively. Figure 1 shows the bidirectional C–V responses at 1 MHz of $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ structures fabricated with different PDA and PMA processes. In general, the hysteresis near flat band of the samples annealed at 400 °C is smaller than that of the samples annealed at lower temperatures. Annealing in FG always results in larger reduction in hysteresis as compared to annealing in N_2 ambient, which is in consistent with report in Ref. 26. For the samples annealed at 400 °C, it is apparent that PDA step is more effective than PMA step which is demonstrated by the better C–V properties of PDA samples (Fig. 1). From Figs. 1(d) and 1(f), the PMA-400-FG sample after being treated in FG ambient still has significant hysteresis value (~92 mV), whereas, the PDA-400-FG sample exhibits the smallest C–V hysteresis value of only 40 mV illustrating a good interface quality of FG process.

Figure 2 shows the multi-frequency C–V characteristics of the samples PDA-400-N_2 and PDA-400-FG respectively. Both two samples exhibit good electrical characteristics of distinct accumulation/depletion regions and small frequency dispersion in accumulation region which are comparable with those of previous studies.[27–29] The C–V inversion behaviors of the two samples are nearly flat which implies that the minority carriers are nearly free from interfaces trapping.[30] The sample PDA-400-FG exhibits smaller frequency dispersion (2.55% per decade) than that of the sample PDA-400-N_2 (3% per decade). The frequency dispersion in the accumulation region is dominated by the response of border traps and the inversion *hump* reveals the interaction between minority carrier and interface states are well known.[24,31,32] On the basis of these facts, the small accumulation frequency dispersion and the small inversion *hump* in the multi-frequency C–V response of the sample PDA-400-FG represent a reduction of both border traps and interfaces states in this sample. Compare to PDA-400-N_2 sample, a slightly reduction of maximum capacitance value was observed for PDA-400-FG sample. It may be due to the incorporation of hydrogen into Al_2O_3 during annealing

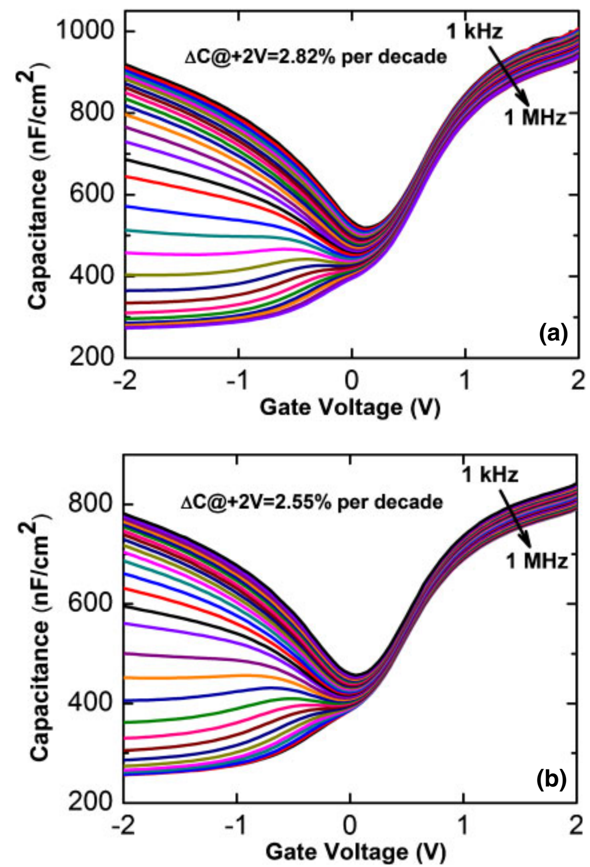

Fig. 2. (Color online) Multifrequency C–V characteristics of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors. (a) PDA-400-N_2 sample with frequency dispersion value of 3% at a gate bias of 2 V. (b) PDA-400-FG sample with frequency dispersion value of 2.55% at a gate bias of 2 V.

process which resulted in the reduction of dielectric value of the Al_2O_3.[24,25)]

In recent studies, the conductance method is proposed as a reliable method for extracting the interface state density in high-k/$In_{0.53}Ga_{0.47}As$ structures.[33,34] The D_{it} value is estimated by the maximum normalized parallel conductance peak, $(G_P/\omega)_{max}$, and is defined as

$$D_{it} = \frac{2.5}{Aq}\left[\frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}\right],$$

where A is the device area, ω is the applied angular frequency, C_m and G_m are the measured capacitance and conductance, respectively. Applying this method, the interface trap densities at trap energy level of 0.2 eV below the conduction band edge (E_c) is extracted to be 1.5×10^{12} and 1.375×10^{12} cm^{-2} eV^{-1} for the samples PDA-400-N_2 and PDA-400-FG, respectively. Obviously, the low D_{it} values indicate an essentially unpinned Fermi level which is in agreement with the best C–V characteristics of the samples underwent PDA process.

The J–V characteristics of the samples in Fig. 3 clearly show that the leakage current densities of the PMA samples are approximately six orders of magnitude higher than that of the PDA samples regardless of annealing ambient. The very large leakage currents in the samples with high PMA temperature lead to the worse C–V characteristics. In contrast, the PDA step could improve the Al_2O_3/InGaAs interface and oxide qualities, thus, samples experienced this step reveal a

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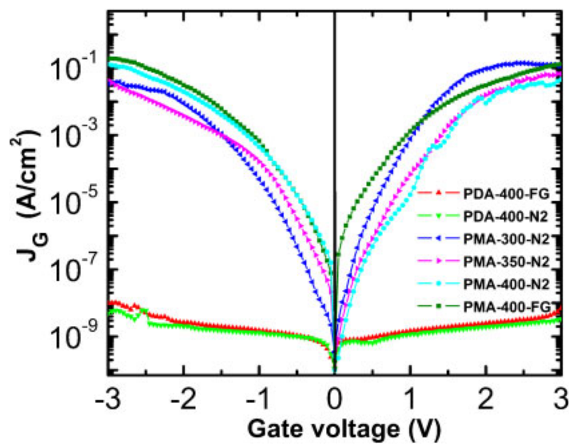

Fig. 3. (Color online) Leakage current density versus gate bias (J–V) of samples with various annealing processes.

low leakage current since the leakage current is dominated by trap-assisted tunneling conduction mechanism at low electric field region.[35] These observations strongly suggested that the sequence of thermal treatment does have a pronounced influence on electrical properties of the structures. Actually, the impact of thermal treatment sequence is even more significant than that of the annealing ambient as can be evidenced from the gate leakage current of samples PDA-400-N_2 versus PMA-400-FG. The low and stable gate leakage current densities of the PDA samples as compared to the PMA samples in spite of the identical annealing temperature reveals that the leakage current of samples annealed at high temperature is not originated from the densification of oxide layer as proposed in Ref. 26. Indeed, if densification of oxide layer is the cause, then the leakage currents of these samples are expected to be similar. However, it was not the case as proved clearly in Fig. 3. In our opinion, the high leakage current in all PMA samples could only be explained by the diffusion of gate metal into oxide layer during long time and high temperature PMA process.

In order to verify the metal diffusion into Al_2O_3 due to PMA process, HRTEM study was performed. Figures 4(a)–4(c) show the cross-sections HRTEM images of the samples with PDA at 400 °C, PMA at 300 and 400 °C, respectively. The oxide thickness of the samples is similar (~9 nm), implying that the effect of densification process on the leakage current is not fully optimized. The HRTEM image of the sample annealed at 400 °C before gate metal formation presents the clear metal/oxide/semiconductor region without any evidence of metal out-diffusion and the interfacial layer formation [Fig. 4(a)]. Whereas, the PMA sample annealed at 300 °C exhibits an interfacial layer of roughly 2 nm between the gate and oxide regions indicating the out-diffusion of Pt into Al_2O_3 oxide layer occurred [Fig. 4(b)]. Upon increasing the PMA temperature to 400 °C, the interfacial layer expands and the oxide layer even appears to be homogeneous, which is attributed to the out-diffusion of Pt at this annealing condition [Fig. 4(c)]. This confirms that the major effect of thermal annealing is the out-diffusion of Pt metal which leads to high leakage current. For further confirmation, the depth profiling AES analyses of PMA and PDA samples annealed at 400 °C were performed and the

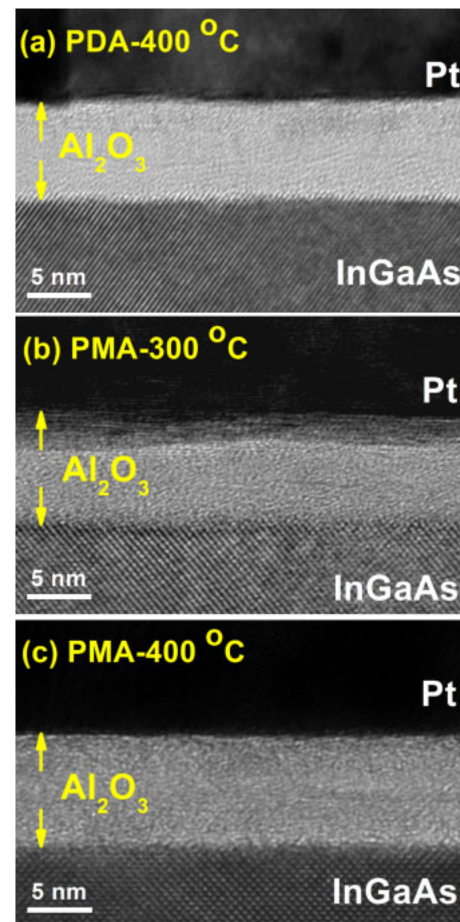

Fig. 4. (Color online) HRTEM images of the $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ structures: (a) PDA treated at 400 °C for 5 min; (b) PMA treated at 300 °C for 5 min; (c) PMA treated at 400 °C for 5 min.

results are shown in Fig. 5. It proves that there is a strong diffusion of Pt into Al_2O_3 for the PMA sample, whereas the PDA sample shows less Pt diffusion. These data support the conclusion that Pt diffusion during PMA step is the cause of the dramatically increase in gate leakage current in the $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs structure. These results also somewhat stand in contrast to the argument that the densification of oxide layer was responsible for the high leakage current as proposed by Hu et al.[26]

4. Conclusions

In conclusion, the electrical characteristics of $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with different annealing processes are presented. The results show that the samples underwent high PDA- and low PMA-temperature exhibited better C–V behaviors with extremely low leakage current as compared to that of the samples underwent high PMA temperature. The high annealing temperature treatment after metal deposition resulted in the incorporation of metal into the Al_2O_3 layer as demonstrated by HRTEM and depth profiling AES analyses. The metal out-diffusion can be considered as the root cause of the larger leakage current density which results in the MOSCAPs electrical characteristics degradation. Post deposition annealing process was found to improve the C–V behaviors of the MOSCAPs as well as effectively prevent the high leakage problem of the MOSCAP structures.

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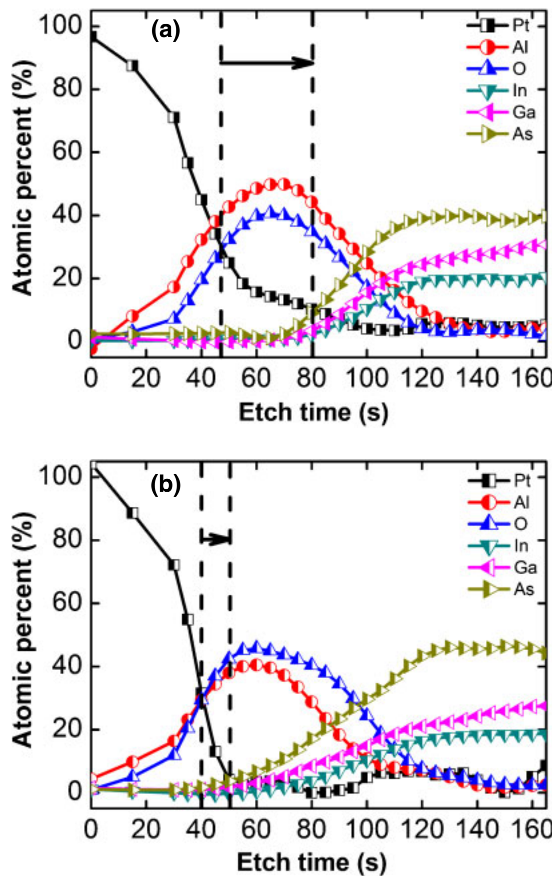

Fig. 5. (Color online) The Auger depth profiling analyses of (a) sample annealed after gate formation and (b) sample annealed before gate formation.

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