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Schottky barrier height modification of metal/4H-SiC contact using ultrathin TiO_2 insertion method

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The fabrication processes, electrical characteristics, and reliability of the Schottky barrier diodes (SBDs) on an n-type 4H-silicon carbide (SiC) substrate are investigated. To modulate the Schottky barrier height (SBH), titanium dioxide (TiO_2) is inserted at the interface between the metal and the SiC substrate. Ni, Mo, Ti, and Al are chosen to form SBDs. The maximum SBH modulation of 0.3 eV is obtained with a 5-nm-thick TiO_2 layer. The SBH pinning factors of the SBDs without TiO_2 insertion and with 2-nm-thick TiO_2 insertion are similar. Therefore, the mechanism of the SBH modulation is attributed to the interface dipole-induced potential drop. Finally, the reliability of the SBD with TiO_2 insertion is evaluated. The SBH, ideality factor, and reverse leakage current are stable after high forward current stress at 300 A/cm^2 for 15000 s. This work provides a simple method to modulate the SBH on SiC and is feasible for SBD application.

1. Introduction

Schottky barrier diodes (SBDs) have been utilized as rectifying devices because of their high switching speed and low minority carrier storage effect compared with pn diodes. However, the reverse breakdown voltage of Si-based SBDs is usually lower than 200 V because the narrow band gap of Si is only about 1.12 eV.[1)] Simultaneously, Si-based SBDs suffer from a high thermal generation rate of minority carriers, which leads to vital leakage current when operating at temperatures higher than 150 °C.

Among more than 170 crystalline polytypes in the silicon carbide (SiC) system, 4H-SiC has been regarded as a candidate for high-power and high-frequency electronic devices owing to its wide band gap (~3.26 eV), high thermal conductivity (~5.0 W cm^{-1} K^{-1}), and high electron mobility (~1000 cm^2 V^{-1} s^{-1}).[2–4)] Besides, SiC is chemically inert and has strong mechanical hardness. These properties are beneficial to operate the SiC power devices in harsh environments, e.g., motor control systems or automobile electronics. SiC-based SBDs have many advantages, such as high breakdown voltage (>600 V) and low switching loss.[5–9)] To avoid unnecessary power consumption due to parasitic resistance, all semiconductor devices require a low Schottky barrier height (SBH) and a low contact resistivity at the metal/semiconductor contacts, which result in bi-directional current flowing through the contacts and low on-resistance (R_{on}).

Considering the Fermi-level pinning effect, the SBH can be expressed as

$$\Phi_{bn} = S(\Phi_m - \Phi_{CNL}) + (\Phi_{CNL} - \chi), \quad (1)$$

where S is the pinning factor, χ is the electron affinity of the semiconductor, Φ_m is the metal work function, and Φ_{CNL} is the semiconductor charge neutrality level.[10)] The published SBHs are drawn as a function of the metal work function (Φ_m) in Fig. 1.[11–17)] The S factor is approximately 0.6–0.7. Although we can achieve a lower SBH and contact resistance by applying lower Φ_m metals, lower Φ_m metals are active and may not be stable during the remaining semiconductor processes. To reduce the SBH and the contact resistivity, most studies have figured out that an ohmic contact can be formed by a high-temperature (>900 °C) annealing process between a heavily doped SiC substrate (>5 × 10^{18} cm^{-3}) and various metals, such as Ni and Ti.[18–24)] In general, the specific contact resistance can be lower than 1 × 10^{-4} Ω cm^2 but higher than 1 × 10^{-6} Ω cm^2.

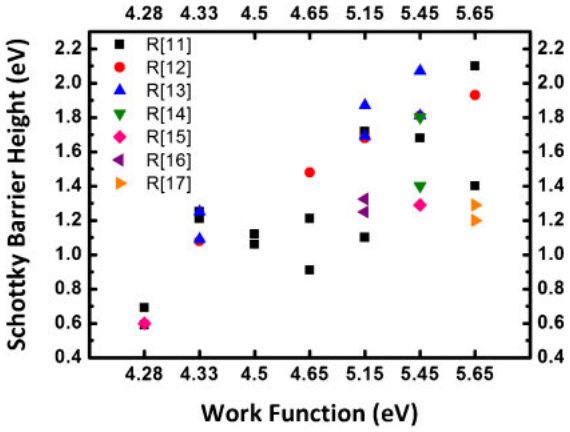

Fig. 1. (Color online) Distribution of Schottky barrier height as a function of metal work function reported in the literature. The pinning factor is approximately 0.6–0.7.

Except for the ohmic contact, introducing a high dielectric constant (high-k) thin film in Si-, Ge-, and GaAs-based SBDs has been proposed to modulate SBH and contact resistivity in recent experiments.[25–27)] Different kinds of dielectrics, e.g., Si_3N_4,[28,29)] MgO,[30)] Al_2O_3,[31,32)] GeO_x,[33)] and TiO_2,[27)] have been employed. Several models have been proposed to explain the SBH modulation mechanism. (1) The inserted dielectric layer could block the work function penetration and reduce the metal-induced gap states (MIGS) to relax the Fermi-level pinning.[30,33,34)] (2) The formation of dipoles at the dielectric/semiconductor interface would provide a potential drop in the carrier transport path to modulate the SBH.[25,35,36)] Recently, Hu et al. have proposed that (3) the fixed oxide charge would exist in a non-ideal, amorphous, and non-stoichiometric dielectric layer and also provide an extra potential drop.[26)] Furthermore, Fermi-level pinning at the metal/dielectric interface is also observed.[37–39)] These explanations are verified in this work.

Compared with the ohmic contact formation by high-temperature annealing, the dielectric insertion method avoids the silicidation process and reduces the thermal budget substantially. Nevertheless, studies have seldom used this method on SiC-based SBDs to modulate SBH so far. In addition, some basic properties have not been studied yet, for example, the SBH control and the contact resistance of the metal/dielectric/SiC contacts.

In this work, we fabricate and characterize the 4H-SiC SBDs with a TiO_2 interfacial layer. It is demonstrated that the TiO_2 layer is able to reduce the SBH on SiC-based SBDs effectively as on Si- and Ge-based SBDs. The stability of the metal/TiO_2/SiC contact is also evaluated by applying current stress at room temperature.

2. Experimental methods

The SBDs were fabricated on an n-type nitrogen-doped (0001)-oriented 4H-SiC substrate with a doping concentration of $1 \times 10^{18}\,cm^{-3}$, with a 5-μm-thick epitaxial layer with a doping concentration of $3 \times 10^{15}\,cm^{-3}$, which was purchased from CREE. First of all, the substrate was cleaned by the standard RCA cleaning process followed by a 200-nm-thick oxide deposition using a plasma-enhanced chemical-vapor-deposition (PECVD) system. This oxide layer was used to protect the front-surface of samples. Native oxide was removed by dipping samples in diluted HF (DHF) solution and then a Ni/TiN stack (100 nm/30 nm) was deposited at the backside of samples using a sputtering system. Samples were then annealed at 1000 °C in N_2 ambient for 30 s to form good ohmic contacts. After the annealing process, the $H_2SO_4 : H_2O_2 = 3 : 1$ solution was used to remove the unreacted metal. The front-side protection layer was removed by buffer oxide etchant (BOE) solution.

For the sake of creating a uniform and hydrophilic surface before TiO_2 deposition using an atomic layer deposition (ALD) system, the samples were soaked in the $H_2SO_4 : H_2O_2 = 3 : 1$ solution for 10 min. Soon afterwards, blanket TiO_2 films with various thicknesses were deposited at 250 °C in thermal mode using tetrakis(dimethylamino)titanium (TDMAT) and H_2O as precursors. In contrast, the reference samples bypassed the soaking in sulfuric acid and the TiO_2 deposition to maintain pure metal/SiC interfaces.

The front-side contacts were patterned by photolithography and cleaned by DHF immersion. The radii of contacts were 400, 200, 100, and 50 μm. Different metals were deposited by sputtering or a thermal evaporation system, followed by deposition of a 300-nm-thick Al layer for probing. Then, metals beyond the contacts were lifted-off by ultrasonic oscillation in acetone. Finally, samples were alloyed at 500 °C for 5 min in vacuum. The key process conditions are listed in Table I.

Electrical measurements were performed at room temperature using a semiconductor parameter analyzer (Agilent 4156C). The cross-sectional structure of SBD was inspected by transmission electron microscopy (TEM; JEM-2100F).

3. Results and discussion

3.1 Effect of TiO_2 thickness

Figure 2 shows sketches of the Ni/TiO_2/SiC band diagram. TiO_2 is selected as the insertion dielectric because of the negative electron barrier between SiC and TiO_2, so that no extra resistance exists and a sufficiently high carrier tunneling probability or thermionic emission rate to obtain a high forward conduction current can be expected.

Table I. Key process conditions.

	Contact metal			
	Al	Ti	Mo	Ni
Metal thickness (nm)	300	100	30	100
Deposition method	Thermal evaporation	Sputtering	Sputtering	Sputtering
TiO_2 thickness (nm)	0, 2	0, 1, 2, 5, 8	0, 2	0, 1, 2, 5, 8
Annealing	500 °C/5 min/in vacuum furnace			

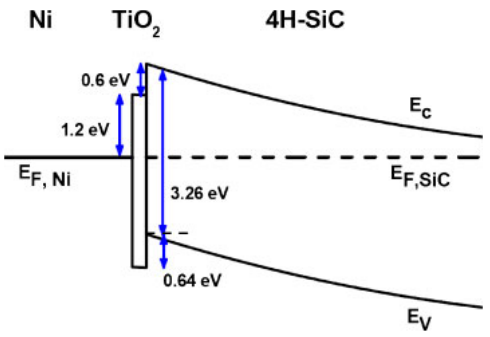

Fig. 2. (Color online) Band diagram of a metal/TiO_2/4H-SiC Schottky barrier diode. The conduction band of TiO_2 is lower than that of SiC, which is preferred to avoid extra electron tunneling resistance.

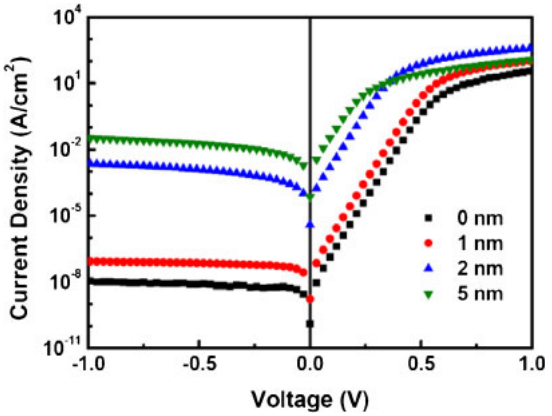

Fig. 3. (Color online) *I–V* characteristics of the Ti SBDs with various TiO_2 thicknesses. Thicker TiO_2 brings about a lower SBH and a higher reverse current.

Firstly, we alter the thickness of the TiO_2 layer to determine the most effective modulation. Figure 3 shows the current–voltage (*I–V*) characteristics of the Ti SBDs with various TiO_2 thicknesses. According to the basic thermionic emission model, the *I–V* characteristic can be expressed as

$$I = AA^*T^2 \times \exp\left(-\frac{q\Phi_{bn}}{kT}\right) \times \left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right], \quad (2)$$

where A is the SBD area, A^* is the effective Richardson constant ($146\,A\,cm^{-2}\,K^{-2}$),[40] k is the Boltzmann constant, and T is the absolute temperature. The ideality factor (η) can be extracted as a qualitative benchmark of SBDs. The SBD without a TiO_2 layer exhibits the highest average SBH and

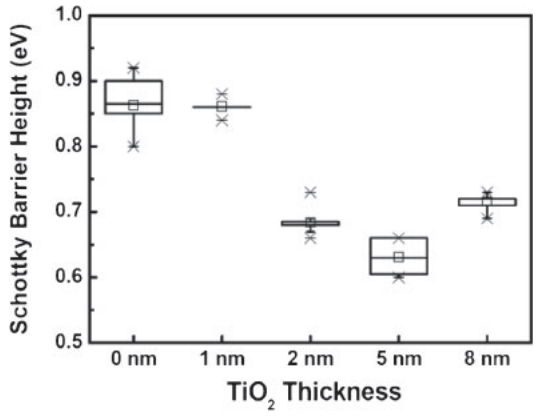

Fig. 4. Distribution of Schottky barrier height as a function of TiO_2 thickness. A 0.2 eV SBH reduction is approached with a 2-nm-thick TiO_2 insertion. The boxes are defined by the 25th and 75th percentiles. The whiskers are defined by the 5th and 95th percentiles. The median, mean, and maximum/minimum values are represented by the line in the box, the square in the box, and the asterisks, respectively.

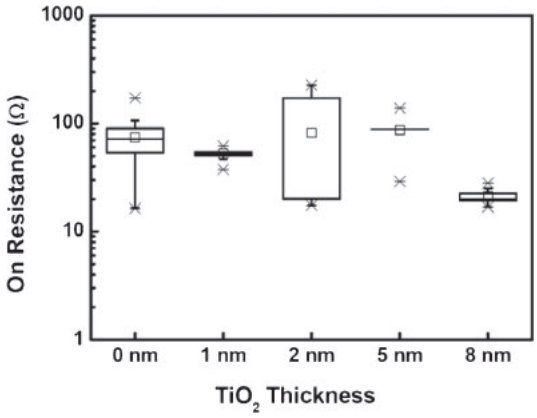

Fig. 5. Distribution of on-resistance as a function of TiO_2 thickness at $V = \Phi_{bn}$. The compact range indicates that the on-resistance is not degraded by the TiO_2 layer. The boxes are defined by the 25th and 75th percentiles. The whiskers are defined by the 5th and 95th percentiles. The median, mean, and maximum/minimum values are represented by the line in the box, the square in the box, and the asterisks, respectively.

the lowest leakage current. On the other hand, as shown in Fig. 4, the SBDs with TiO_2 insertion show modulated characteristics and the average SBH decreases from 0.9 to 0.63 eV as the TiO_2 thickness increases from 0 to 5 nm. As the thickness of the TiO_2 layer exceeds 5 nm, the carrier tunneling probability or thermionic emission rate decreases dramatically. Therefore, the SBDs turn out to have a higher average SBH (~0.75 eV). This trend of SBH modulation is similar to that observed on a Ge substrate.[27] It is known that the SBH would be affected by the surface defects.[41–43] Figure 4 shows that the SBH variation of the SBDs with TiO_2 insertion is lower than that without TiO_2 insertion. This result implies that the TiO_2 layer can passivate the surface defects to improve the device uniformity.

Figure 5 shows the R_{on} distribution versus TiO_2 thickness. On purpose, we extracted R_{on} at $V = \Phi_{bn}$ to unify the turn-on situation of different SBDs. R_{on} is not degraded by the TiO_2 layer as expected because of the negative conduction band off-set between TiO_2 and SiC. Since the SBDs are fabricated on the substrate with a lightly doped epitaxial layer, R_{on} is dominated by the resistance of the epitaxial layer. To reduce the extracted specific contact resistance, the doping concentration near the interface of the metal/SiC contact should be raised and suitable test structures such as the transmission-line method (TLM) structure or the cross-bridge Kelvin resistor (CBKR) structure should be employed.

3.2 SBH modulation mechanism

In Fig. 6, compared with pure metal/SiC SBDs, we use a 2-nm-thick TiO_2 layer as a standard condition to study the SBH modulation with various metals. The pinning factors S can be extracted from the slope of the linear regression of the SBH versus metal work function plot. The metals we used are Ni, Mo, Ti, and Al with work functions of 5.15, 4.65, 4.33, and 4.16 eV, respectively. The pinning factor of pure metal/SiC SBDs is about 0.8, which is slightly higher but still comparable to the pinning factor obtained from Fig. 1. In contrast, the pinning factor of the metal/TiO_2 (2 nm)/SiC SBDs is about 0.87, which is similar to the pinning factor of the pure metal/SiC SBDs.

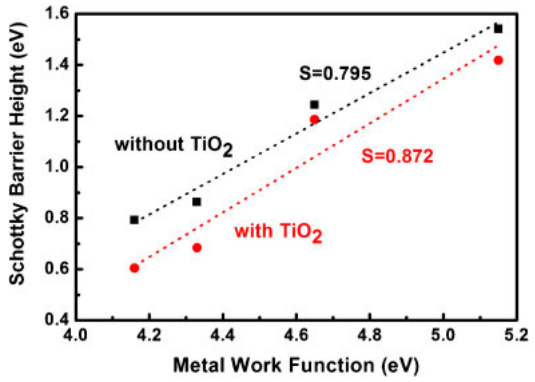

Fig. 6. (Color online) Distribution of Schottky barrier height as a function of metal work function. The pinning factor does not change significantly, but the SBHs of Ni, Ti, and Al SBDs reduce by about 0.2 eV uniformly when TiO_2 is inserted.

As mentioned in the introduction, one of the SBH modulation mechanisms is MIGS. If this is the main mechanism, the Fermi level pinning effect should be eliminated and the pinning factor should be much closer to 1 after TiO_2 insertion. However, there is only a slight difference between both conditions, which indicates that the inserted TiO_2 layer does not depin the Fermi level effectively. MIGS may be not the main mechanism for barrier lowering. The high pinning factor also implies that MIGS are not severe on the SiC SBDs. Meanwhile, various metals exhibit a similar level in the SBH modulation. The average SBH values of Ni-, Ti-, and Al-contacted diodes decrease uniformly by ~0.2 eV when a 2-nm-thick TiO_2 layer is inserted. Therefore, the effect of the TiO_2 layer is to shift the SBH but not to relax the Fermi level pinning.

It has been suggested that the fixed oxide charges in the inserted dielectric or the dipole at the dielectric/SiC interface would induce an extra potential drop.[25,26,35,36] This potential drop reduces the SBH. Besides, owing to the 500 °C alloying process on all samples, a new interfacial layer may be formed to modulate the SBH. The cross-sectional structure of the Ni

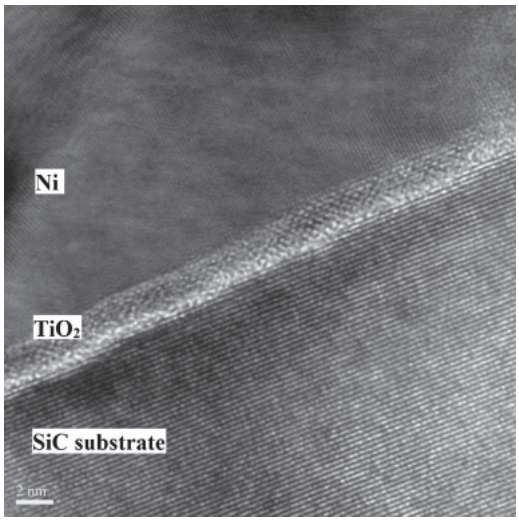

Fig. 7. TEM image of Ni SBDs with a 2-nm-thick TiO_2 insertion. Three clear layers, Ni, TiO_2, and SiC, are separate and no new interfacial layer was formed. The TiO_2 layer has become polycrystalline after the alloying process.

SBD with a 2-nm-thick TiO_2 layer was inspected by TEM. As shown in Fig. 7, three layers, Ni, TiO_2, and SiC, are clearly distinct and no new interfacial layer was formed during the alloying process. It is concluded that the SBH modulation is not induced by the formation of a new interfacial layer. At the same time, the image of the TiO_2 layer shows an ordered arrangement, which indicates that, the TiO_2 layer becomes crystallized during the alloying process. We assume that the relative dielectric constant of the TiO_2 layer is 80.[44] If the main mechanism of the SBH reduction is due to the fixed oxide charge, to approach a 0.2 eV reduction in the band diagram, the estimated amount of fixed oxide charge would be as high as $4 \times 10^{13}\,cm^{-2}$. However, the amount of fixed oxide charge should be decreased substantially as the dielectric layer crystallizes. Consequently, we postulate that the interface dipoles induced by the inserted TiO_2 layer affect the SBH reduction effectively rather than the fixed oxide charge. It should be noted that the SBH is not pinned at the metal/TiO_2 interface, as reported in the literature.[38,39] A possible reason for this is that the TiO_2 is not thick enough to prevent the interaction of wave-functions between the metal and the SiC substrate. The Fermi-level pinning effect with different TiO_2 thicknesses and alloying temperatures should be studied to clarify the pinning mechanism between the metal and the dielectric layer.

3.3 Reliability testing

Figure 8 shows the SBH, ideality factor, and reverse biased leakage current of the Ti SBD with 2-nm-thick TiO_2 stressed with accumulated time. A high stress current of about 300 A/cm^2 was applied at forward bias under room temperature. In Fig. 8(b), the reverse biased leakage current was measured when the stress duration was finished. A minor increase in the reverse biased leakage current is observed. However, the variations before and after stress are only 8.4 and 7.4% at −3 and −100 V, respectively. The extracted SBH and ideality factor are constant. According to the consistent results before and after testing, it is suggested that the TiO_2 layer is stable for forward stress.

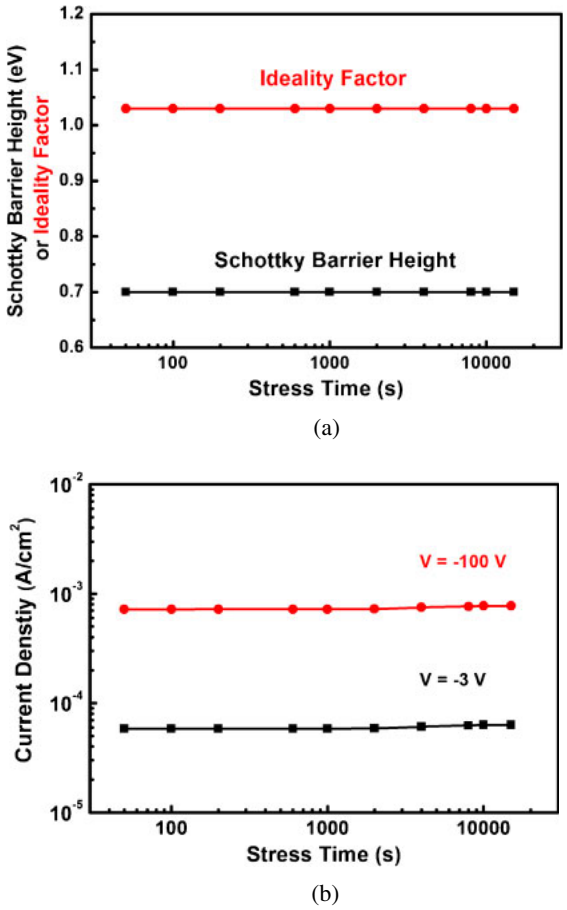

Fig. 8. (Color online) Parameters of the Ti/TiO_2 (2 nm)/SiC SBD after current stress at ~300 A/cm^2 for 15000 s. The parameters are (a) Schottky barrier height and ideality factor and (b) reverse current at $V = -3$ and −100 V. All parameters are very stable.

Figure 9 shows the electric fields at both sides of the TiO_2/SiC interface at reverse biases of −3 and −100 V and the voltage drops across the TiO_2 layer as a function of the TiO_2 thickness. The parameters used for the calculation are permittivity of TiO_2 is 80, permittivity of SiC is 10, doping concentration of SiC is $3 \times 10^{15}\,cm^{-3}$, and thickness of the SiC epitaxial layer is 5 μm. Since the dielectric constant of TiO_2 is 5–8 times higher than that of the SiC and the TiO_2 thickness is much smaller than the depletion width in SiC, the TiO_2 capacitance is much higher than the depletion capacitance. Therefore, almost all of the voltage drops across the SiC but not across the TiO_2 layer. Furthermore, the electric field in TiO_2 is much lower than the critical field of TiO_2, which is about 0.3 MV/cm.[45] These results indicate that the inserted thin TiO_2 layer would not affect the reverse breakdown performance of the SBD. Nevertheless, SiC-based SBDs are usually operated at near breakdown voltage and under high-temperature condition. To simulate the work environment, more harsh reliability tests should be applied on the SBDs with TiO_2 inserted.

4. Conclusions

In this study, SBDs on 4H-SiC substrates were fabricated with different TiO_2 thicknesses to investigate the effect of the dielectric insertion on the SBH modulation. The maximum

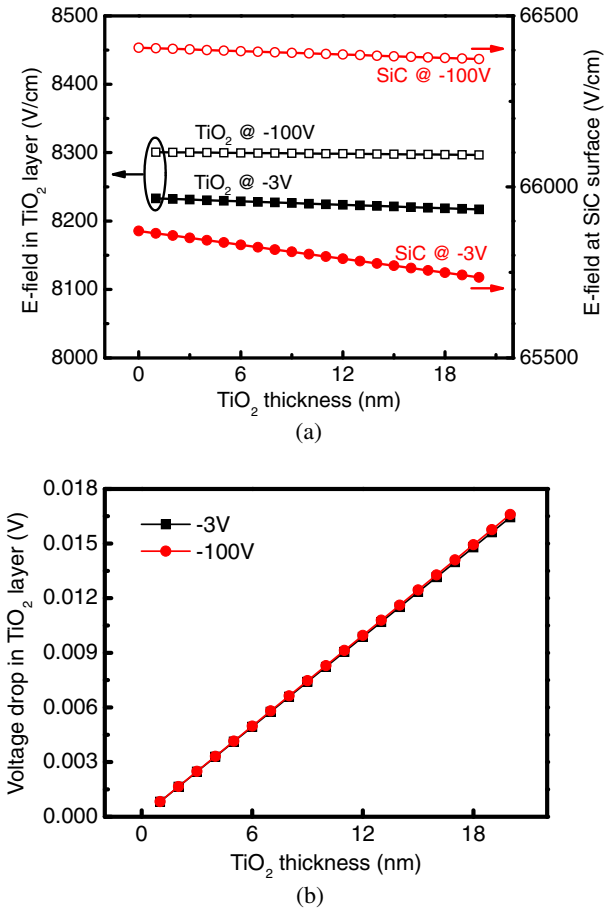

Fig. 9. (Color online) (a) Calculated electric fields at both sides of the TiO_2/SiC interface and (b) calculated voltage drops across the TiO_2 layer at $V = -3$ and -100 V.

SBH modulation of 0.3 eV is achieved with a 5-nm-thick TiO_2 insertion layer between Ti and SiC. The similar R_{on} distributions suggest that the TiO_2 insertion does not degrade the SBDs. The pinning factor increases slightly from 0.8 to 0.87 so that the MIGS model cannot explain the change of the SBH completely. The fixed oxide charge model or newly formed interfacial layer are also excluded because the TEM image of the Ni/TiO_2 (2 nm)/SiC structure shows no new interfacial layer but a gradually crystallized TiO_2 layer. The main mechanism of the SBH modulation is attributed to the interface dipole. Finally, a high-level current stress was applied on the SBDs with TiO_2 inserted. The SBH, ideality factor, and reverse leakage current are similar before and after stress. It is suggested that the dielectric insertion technique can be used to control the SBH of SBDs and to form low resistance ohmic contacts.

Acknowledgements

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