ECS Transactions, 53 (3) 59-67 (2013)
10.1149/05303.0059ecst ©The Electrochemical Society

The Materials Integration of Ge and $In_xGa_{1-x}As$ on Si Template for Next Generation CMOS Applications

Edward Yi Chang[a,b], Shih-Hsuan Tang[a], Yueh-Chin Lin[a]

[a] Department of Materials Science and Engineering, National Chiao Tung University
1001 Ta-Hsueh Rd., Hsin-chu 300, Taiwan, R.O.C
[b] Department of Electronics Engineering, National Chiao Tung University
1001 Ta-Hsueh Rd., Hsin-chu 300, Taiwan, R.O.C

In the study, the growth of InAs on Si is demonstrated using "interface blocking" technique with SiGe layers as buffer layer.
the growth of high quality Ge film on GaAs substrate by ultra high vacuum chemical vapor deposition and high quality InAs material on Ge/SiGe/Si template grown by molecular beam epitaxy will be particularly reported. By the observation of XRD and AFM, both Ge film grown on GaAs material and InAs grown on Si substrates demonstrate high crystallinity and good surface morphology. The developed epitaxial materials systems including Ge on GaAs and InAs on Si are useful for future III-V/Ge/Si integration for next generation high speed low power CMOS application as well as for RF/digital mixed signal circuit application in the future.

Introduction

Recently, the semiconductor industry community faces challenges from the continued reduction of device feature sizes for silicon devices. Meanwhile, the III-V compound semiconductor materials such as InSb, $In_xGa_{1-x}As$ attract a lot of attentions for post CMOS applications, because these materials have significantly higher carrier mobility than silicon. For example, InAs has an electron mobility of 20000 $cm^2V^{-1}s^{-1}$. High-speed devices such as quantum-well field-effect transistors (QWFETs) made from these III-V materials have demonstrated very low gate delay time. Meanwhile, for the post CMOS applications, Ge is considered as a good candidate for p-channel material because of its high hole mobility (1,900$cm^2V^{-1}s^{-1}$). The Ge epitaxial film grown on GaAs is of immense interest due to the lattice mismatch is practically zero (~0.08%) which ensures large critical thickness and low dislocation density, strain-free Ge epitaxial film. As a result, they have the great potential as the transistor-channel materials for quantum-well field-effect transistors and show very attractive and tangible merits over scaled Si MOSFETs. In addition, these devices are well established on GaAs and InP substrates with high cost. These problems can be solved by growing SiGe buffer layers on Si substrate as the templates for high-hole-mobility Ge for p-channel and high-electron-mobility III-V materials, such as $In_xGa_{1-x}As$ or InAs, for n-channel with the complementary circuitry architecture. A seamless, robust heterogeneous integration scheme of III-V nFETs and Ge pFETs on silicon will allow high-speed, low-voltage transistors to couple with the mainstream Si CMOS platform, while avoiding the need for developing large diameter III-V substrates with a substantial reduction in cost, reduced brittleness and increased size.

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Experimental Process

InAs on Si material growth

For the SiGe/Si template for further $Al_{0.5}Ga_{0.5}Sb$/InAs structure growth, epitaxial SiGe and Ge layers were grown by UHVCVD equipment using silane (SiH_4) and germane (GeH_4) as the Si and Ge sources. The 4" Si substrates were cleaned by immersing in deionized water (DI water) for 3 mins and dipped in 10% hydrofluoric acid (HF) for 5 seconds to remove silicon oxide. Oxide-free surfaces passivated by the dangling bonds terminated with hydrogen are obtained by the HF dipping process.

In the growth of the 1st SiGe buffer layer at 350°C, the composition of Si and Ge are 0.1 and 0.9. Then the 2nd SiGe buffer layer where the composition of Si and Ge are 0.05 and 0.95 was grown on the top of the 1st SiGe buffer layer at 350°C and finally the pure Ge layer was grown on this structure. Between the processes of each epitaxial layer, an annealing step is introduced for 10 minutes at 600 °C to improve the crystal quality of the epitaxial layers. Finally, annealing was performed again at 600 °C for 10 min in order to remove defects that are possibly generated in the growth of Ge layer. The structure can be the SiGe/Si template for further integration with $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT (high electron mobility transistor) structure.

The Fig. 1(a) demonstrates the $Al_{0.5}Ga_{0.5}Sb$/InAs structure grown on a SiGe/Si template. Three epitaxial growth systems were used to grow this structure. First, an ultrahigh vacuum chemical vapor deposition (UHVCVD) system was used to grow the SiGe/Si template as mentioned above. Then, a commercial metal organic chemical vapor deposition (MOCVD) was utilized to grow a thin GaAs film on the top of the Ge film (1). Finally, the high quality $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure was grown by a molecular beam epitaxy (MBE) system.

During the MOCVD growth, the growth pressure of the GaAs film is 40 torr, and V/III ratio is 100 (1). Finally, the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT was grown on top of the Ge layer by MBE system and the wafer was baked at 630 °C for 1 min before the growth. The buffer layers were grown at 560°C including a GaAs layer, an AlSb layer, two GaSb/AlSb superlattices, and two $Al_{0.5}Ga_{0.5}Sb$ layers to accommodate the 7% lattice mismatch between the $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT structure and the Ge layer. Then an InAs channel layer including a 50 nm $Al_{0.5}Ga_{0.5}Sb$ layer, a 15 nm InAs layer, a 13 nm $Al_{0.5}Ga_{0.5}Sb$ layer (Schottky layer), and a 3 nm GaSb layer (cap layer) was grown on the top of the buffer layer to form the AlGaSb/InAs HEMT structure. The growth temperature of InAs layer and $Al_{0.5}Ga_{0.5}Sb$ layer was set at 520 °C to obtain a good quality InAs channel layer.

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

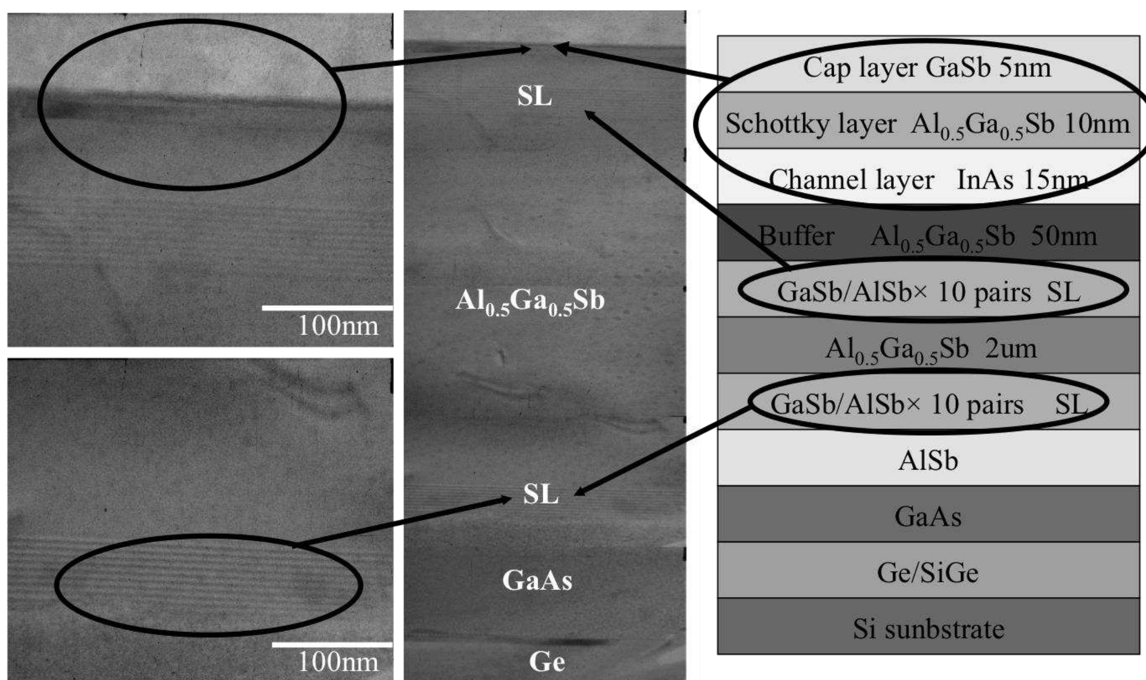


Figure 1. The illustration of $Al_{0.5}Ga_{0.5}Sb$/InAs HEMT on Si substrate and the cross-sectional TEM images

Ge/GaAs material growth

In the Ge epitaxial growth, epi-ready GaAs 2-inch (100) wafers were used as substrates for Ge deposition. GeH_4 was used as the Ge source in the UHVCVD system. The as-received GaAs wafer was loaded into the load-lock chamber without any pre-cleaning after breaking the N_2 filled package. The native oxide (As_2O_3 and Ga_2O_3) on the GaAs surface could be removed by a prebake step in the growth chamber at 600°C, because the native oxide of GaAs would be decomposed at high temperature. Due to the sensitive nature of the GaAs substrate surface, the prebake time should be controlled carefully to prevent the decomposition and overpressure of GaAs. During the growth of the 250nm Ge film at 600°C, the GeH_4 flow rate and the growth pressure was fixed at 10 sccm and 20 mTorr.

Ge/GaAs MOSCAPs

For the Ge/GaAs MOSCAPs (metal oxide semiconductor capacitor) fabrication, the Ge/GaAs wafer was degreased in acetone and isopropanol followed by the removal of native oxide using HF (49%): H_2O=1:100 solution and finally rising with deionized (DI) water. After the HF treatment, one sample went through rapid thermal oxidation (RTO) to grow a thin GeO_2 film prior to the deposition of Al_2O_3. The RTO was performed at 450 °C for 5 minutes in oxygen atmosphere. After that, ~10nm atomic layer deposition (ALD) Al_2O_3 was deposited at 250 °C as the MOSCAP dielectric. Post deposition annealing (PDA) was carried out at 400°C for 5 minutes in forming gas (2) followed by e-beam evaporated Pt/Au (500Å/1000Å) gate metal and Ti/Au (500Å/1000Å) ohmic

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

contact, respectively. Finally, post metal annealing was performed at 250 °C for 30 seconds in forming gas.

Results and Discussion

InAs on Si material growth

The TEM analysis of SiGe/Si template reveals that propagated dislocations were bent sideward and terminated very effectively at the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces, so the threading dislocation density of Ge film is 8.3×10^{6} cm^{-2} measured by the etching pit method. Through the AFM tapping mode measurement shown in fig. 2, the root mean square (RMS) roughness of the Ge surface is 32 Å.

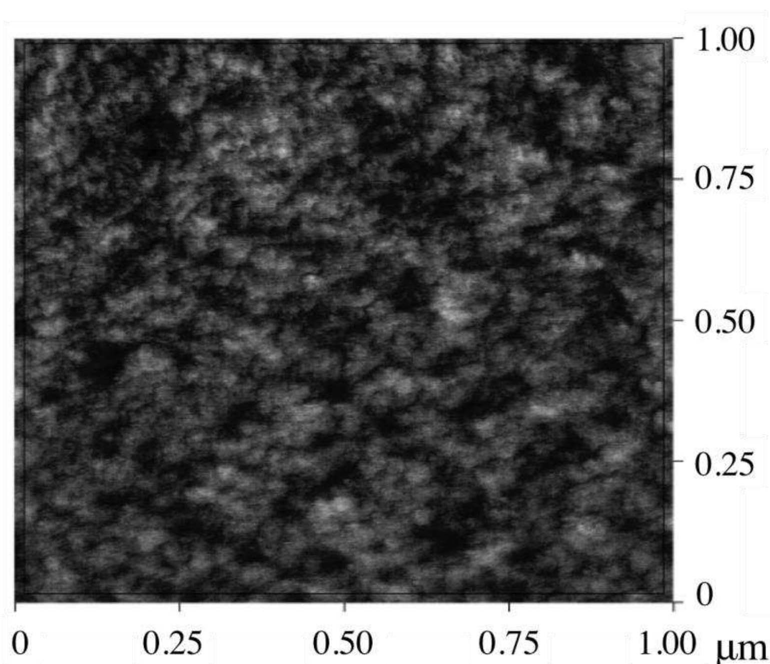


Figure 2. The root mean square (RMS) of the Ge surface is 32 Å by AFM measurement.

It is obvious from the cross-sectional TEM images (Fig. 1b) of the $Al_{0.5}Ga_{0.5}Sb/InAs$ HEMT on Ge with SiGe buffer layer that the interfaces of buffers were quite smooth, and the defect density in the InAs channel is pretty low. And the RMS roughness of the $Al_{0.5}Ga_{0.5}Sb/InAs$ HEMT on Si wafer surface was 19.1 Å. From the high resolution x-ray diffraction (HRXRD) analysis, these major peaks are very clear, and it indicates that the crystalline quality of the HEMT structure was very good. The room-temperature electron mobility of 27300 cm^2/Vs was achieved for the $Al_{0.5}Ga_{0.5}Sb/InAs$ HEMT grown on SiGe/Si template. This is the highest mobility for a HEMT structure grown on Si substrate reported so far and that a very-high mobility $Al_{0.5}Ga_{0.5}Sb/InAs$ HEMT structure has been demonstrated with a well designed buffer layer.

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Ge/GaAs material growth

The crystal quality of 250nm Ge film deposited at 600°C was checked by HRXRD measurement (Bede D1 XRD system). The double axis scanned result is shown in Fig. 3 with the GaAs substrate peak at zero. The appearance of fringes on both sides of Ge and GaAs peaks implies a parallel and very good interface existed in this Ge/GaAs heterojunction structure (3).
The RMS roughness of Ge film was only 0.132 nm by AFM measurement. Figure 4 shows the cross-sectional TEM micrograph of a 2.75 µm thick Ge film deposited on a GaAs substrate at 600 °C. A few misfit dislocations are detected at the interface, but no threading dislocations are seen.

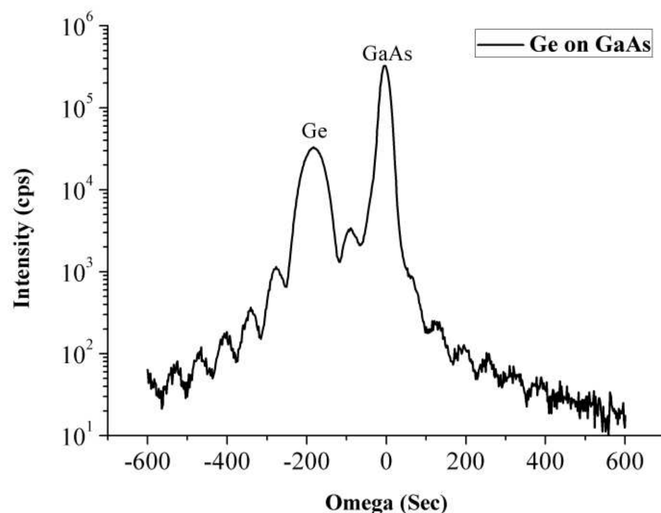


Figure 3. XRD measurement of a 200 nm Ge film on a GaAs substrate. The fringes on both sides imply a sharp Ge/GaAs interface

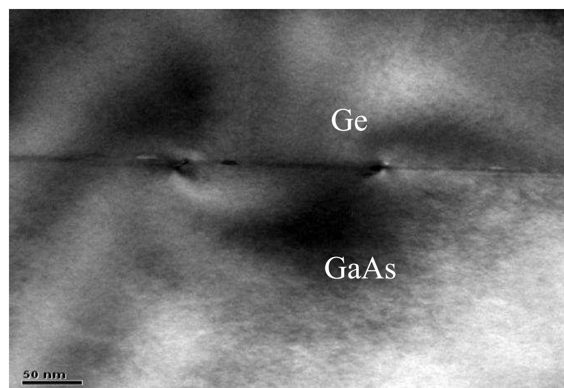


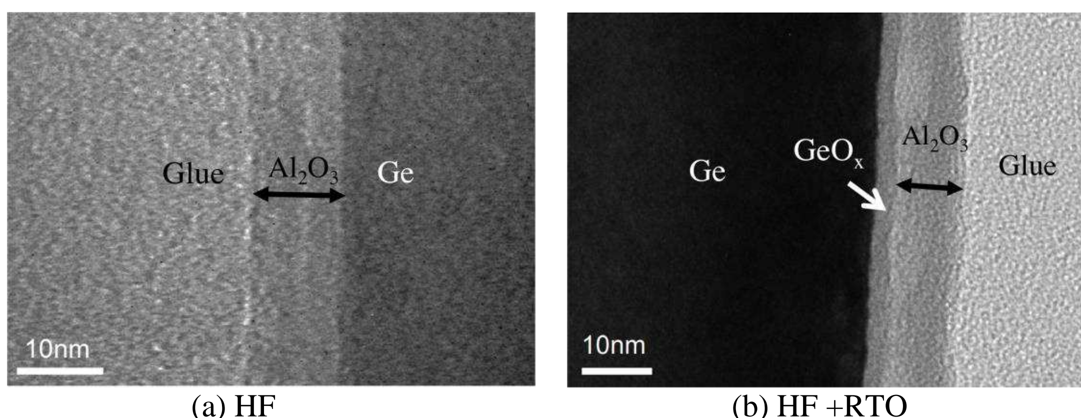
Figure 4. Cross-sectional TEM image of Ge on GaAs. A few misfit dislocations are seen at the interface but no threading dislocation is detected.

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Ge/GaAs MOSCAPs

The multi-frequency C-V behavior of Al_2O_3/Ge/GaAs MOSCAPs with HF treatments measured at the frequencies from 100 Hz to 100 kHz shows p-type behavior, indicating that the Ge epitaxial layer exhibits n-type doping which is in agreement with the previous study and is related from the arsenic auto-doping effect during the growth of Ge epitaxial film on GaAs (4).

According to the TEM analysis of figure 5, it is obvious that a GeO_x interfacial layer with 2.5nm has been obtained after RTO treatment. From the capacitance-voltage measurement, we can notice that the capacitance of the sample with RTO treatment is lower than the one without RTO. It is because the GeO_x formed after RTO treatment increases the equivalent oxide thickness (EOT) of the MOSCAP sample compared to the sample without RTO. For all we know, the capacitance of the MOSCAP varies inversely as the EOT value, so the capacitance value of samples with RTO treatment would be lower corresponding to larger EOT value. The sample treated with HF only is analyzed by TEM also to compare with the samples treated by HF plus RTO. From the figure (5a), there is no GeO_x interfacial layer between Ge film and Al_2O_3, and it implies that the GeO_x is formed only during RTO process.



(a) HF (b) HF +RTO

Figure 5. The TEM analysis of Ge/GaAs MOSCAP without and with RTO treatment

From the current-voltage characteristics of Al_2O_3/Ge MOSCAPs (Figure 6), it is obvious that the leakage current is smaller than 10^{-8} A/cm^2 in the range -5V to 3.5V gate bias and the I-V behaviors in both samples are very similar. It implied that Al_2O_3 deposited by ALD had a very good quality and RTO process does not create any surface damage.

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

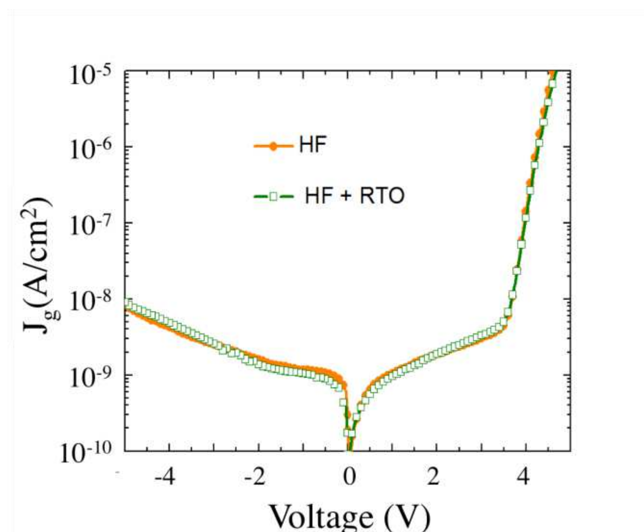
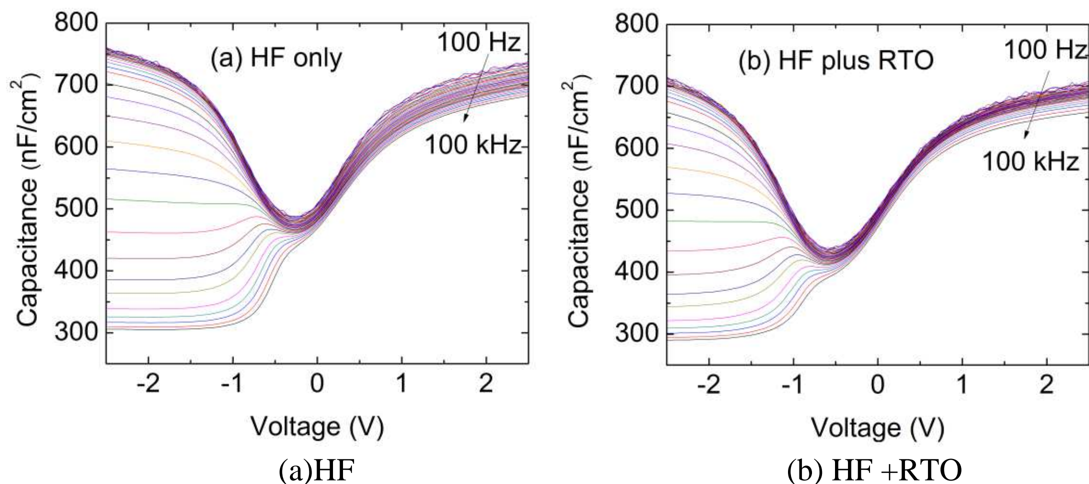


Figure 6. The current-voltage characteristics of Al_2O_3/Ge MOSCAPs

From figure 7, Excellent C-V curves with good inversion behaviors were observed for both the samples, and the sample shows smaller frequency dispersion in accumulation region and depletion region as compared with the sample with HF treatment, and capacitance of the sample with RTO treatment is lower due to the contribution of GeO_x layer.



(a)HF (b) HF +RTO

Figure 7. The capacitance-voltage measurement of Ge/GaAs MOSCAP (a)without and (b)with RTO Treatment

For high performance MOSFET, the interface quality of the MOS capacitor is very important, and the lower D_{it} is needed. The higher D_{it} value has a significant effect on the transistor performance by increasing the transistor sub-threshold slope, drain-induced barrier lowering, etc. The values of D_{it} of these samples were extracted by conductance method (5).

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

At different gate voltages in the depletion region, the D_{it} values estimated at near Ge mid-gap by conductance method are 1.2×10^{13} $eV^{-1}cm^{-2}$ for samples with HF treatment through Figure 8. The D_{it} estimation was took into consideration of the weak inversion response, resulting in the overestimation of the D_{it} (6). For more accurate estimation of D_{it}, full conductance method needs to be applied and the true values should be one order lower than these above values, i.e. about mid 10^{11} $eV^{-1}cm^{-2}$ for the case treated by HF (6).

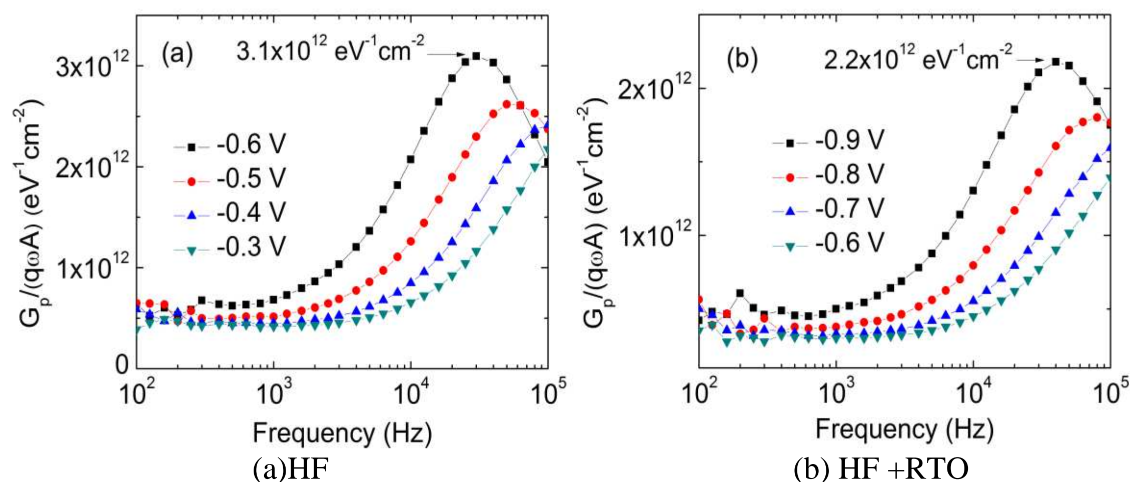


Figure 8. The $G_p/q\omega A$ versus frequency measurement for Al_2O_3/Ge/GaAs samples (a) with HF treatment (b) with HF plus RTO treatment

Conclusion

Both Ge films grown on GaAs and InAs films grown on Si substrate demonstrate high crystallinity and good surface morphology as observed by XRD and AFM. Furthermore, the fabrication process and electric characteristics of Ge/GaAs MOSCAP were discussed in the study. The developed epitaxial materials systems and device fabrication including InAs on Si and Ge on GaAs are useful for future III-V and Ge integration on Si substrates for next generation high speed low power CMOS as well as for RF/digital mixed signal circuit applications in the future.

References

1. Edward Yi Chang, Tsung-His Yang, Guang-Li Luo, and Chun-Yen Chang, J. Electron. Mater., **34**, 23 (2005).
2. H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, Appl. Phys. Lett., **97**, 042903 (2010).
3. M. Zhu, H. C. Chin, G. S. Samudra, and Y. C. Yeo, J. Electrochem. Soc., **155**, H76 (2008).
4. S. H. Tang, Edward Y. Chang, M. Hudait, J. S. Maa, C. W. Liu, G. L. Luo, H. D. Trinh, and Y. H. Su, Appl. Phys. Lett., **98**, 161905 (2011).

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

5. D. K. Schroder, Semiconductor Material and Device Characterization, Wiley, New Jersey (2006).
6. K. Martens, C. O. Chui, G. Brammertz, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices, **55**, 547 (2008).

Downloaded on 2014-12-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).