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Effect of layout on electromigration characteristics in copper dual damascene interconnects



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ABSTRACT

This study demonstrates that the electromigration (EM) behavior of dual damascene Cu lines is strongly affected by the layout which surrounded the tested EM lines, especially for Cu line below 0.10 μ m used for 40 nm or below technologies. The Cu EM lifetime declines as the number of local dummy lines increase, and the global dummy line density increases with the width of the Cu line below 0.063 μ m. This work presents mechanisms of layout effects that explain the EM characteristics and can be exploited to improve the layout effect. Therefore, not only the stressed Cu line structures, but also the surrounding layouts must to be considered in assessing EM reliability of a real IC circuit in 40 nm or below technology.

1. Introduction

Electromigration (EM)-induced failure is one of the most serious reliability issues concerning interconnects in integrated circuits as the features of ICs are scaled down to submicron dimensions [1,2]. Most works have demonstrated that the Cu EM performance is dominated by the interface/surface that is available for mass transport [3,4] and by back stress that is applied to the Cu line [5,6]. That is, enlarging the dimensions (thickness and width) of the Cu line or shortening Cu line length enhances EM performance, and vice verse.

Most studies have pointed out that EM characteristics are determined by the dimensions of the stressed Cu lines, and not that the dummy layout that surrounded the stressed Cu line is significantly involved [7,8]. However, in real circuit design, the power Cu lines are surrounded by various dummy structures in to improve process control. The effect of the dummy layout effect on EM characteristics is not well understood. Therefore, this work will attempt to evaluate the effect of both the local and the global dummy layout on EM behavior. Finally, mechanisms that explain the EM characteristics of the effect of the dummy layout are proposed.

2. Experimental

The EM test structures with 250 μ m-long metal lines with different metal widths (0.1 μ m and 0.063 μ m) were evaluated in this

study. Electrons under electrical stress flow from the lower metal line to the higher metal line through the via as presented in Fig. 1. Various layouts of both local dummy and global dummy lines displayed in Fig. 2, are compared. The Cu interconnects were embedded in low-k (k = 2.5) material and processed with an SiCN capping layer. The via dimension is the same as that of the metal width. The stress temperature varied from 275 °C to 350 °C at a fixed current density of 2.0 MA/cm² based on the drawing cross-sectional area of the Cu line. A sample size of 20–30 was used in each experiment. The increase in resistance with time was monitored until failure. A failure criterion of a 10% increase in resistance was adopted. The current supply was stopped at a 30% increase in order to minimize the damage to the Cu interconnects by electromigration for physical failure analysis.

3. Results and discussion

3.1. Electromigration result

3.1.1. Effect of local dummy layout

Fig. 3 presents the time-to-failure (TTF) lognormal distribution for 0.1 μm-wide Cu lines with various dummy layouts that surround the Cu EM tested line. As presented in Fig. 3, EM-induced failure times obtained using the three various tested layouts are similar, independently of for the surrounded layout. Additionally, the EM lifetime for the test line without the dummy structure is slightly longer than that with the dummy layout. This slight improvement in EM failure time in the accelerated EM test did not result in a significant difference in projected EM lifetime under

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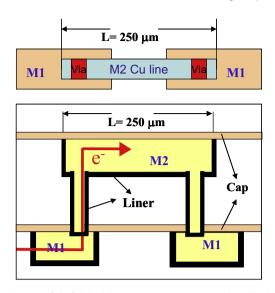


Fig. 1. Schematic of via-fed dual damascene test structure employed in this study.

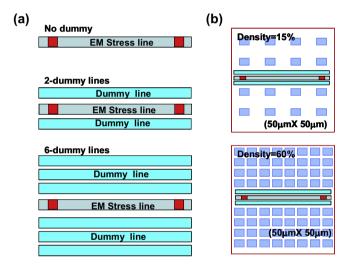


Fig. 2. Schematic of the test structure layout with various dummy environments (a) local dummy lines that surround the tested Cu line; (b) global dummy lines in a $50~\mu m \times 50~\mu m$ area.

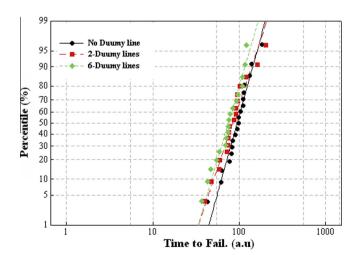


Fig. 3. Failure time distribution for various local dummy layouts for 0.1 μm width Cu metal line.

real operating conditions. Therefore, for 0.1 µm-width Cu lines, the EM characteristics are independent of the surrounded dummy layout, and are affected only by the tested Cu lines. However, when the width of the Cu line is further decreased to 0.063 µm, a completely different result was obtained as shown in Fig. 4. In contrast to the result for 0.1 µm-wide Cu lines, the EM failure time is significantly affected by the dummy lines that surround the EM tested lines. The EM lifetime is shorter for the tested Cu lines with more dummy lines than those with fewer dummy lines. Moreover, the Cu lines without any dummy lines still exhibit the longest EM lifetime. To investigate this difference that is caused by the dummy layout, EM tests were performed at three stressing temperatures to determine the activation energy (Ea). The activation energies (Ea) in Fig. 5 were found to be \sim 0.88–0.92 eV, independent of the local dummy layout. These activation energies indicate that Cu/ ESL interfacial diffusion dominated electromigration [9,10]. As observed previously, the tend of EM median-time-to-failure (MTTF) is the same for all stressing temperatures; the Cu line that is surrounded by more dummy lines has a shorter median failure time, and the Cu line without any dummy lines has the longest lifetime. This finding indicates that the EM failure mechanism is similar among various dummy layouts and another factor causes the variation. The physical analyses of the failed samples by

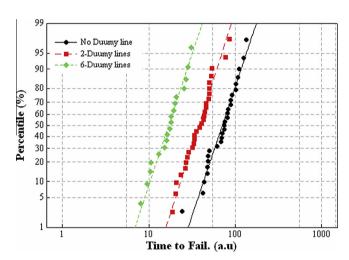


Fig. 4. Failure time distribution for various local dummy layouts for 0.063 μm width Cu metal line.

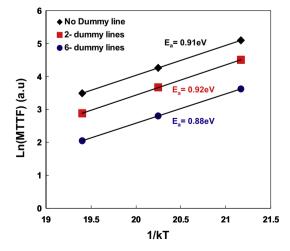


Fig. 5. Activation energy (Ea) using Arrhenius plots for various local dummy layouts for $0.063 \, \mu m$ width Cu metal line.

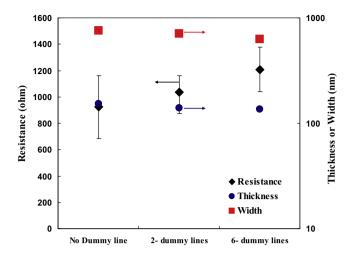


Fig. 6. SEM thickness, width and initial resistance of the stressed Cu lines for various local dummy layouts for 0.063 μm width Cu metal line.

scan-electron-microscopy (SEM) technology support this conclusion. As expected, the location of EM failure is the Cu/capping dielectrics interface in the various dummy layouts, and is independent of the dummy layout. However, the SEM analysis of the physical dimensions indicates that the thickness and the width of the tested Cu lines decrease as the number of dummy lines increases. This finding is consistent with the initial resistance of the un-tested Cu lines presented in Fig. 6. Reducing the width of the Cu lines or the thickness increases the current density in Cu tested lines, therein, reducing EM lifetime. Normalizing the stress current density according to the real cross-sectional area of Cu line leaves differences in EM lifetime among the various local dummy line structures as shown in Table. 1. Additionally, this EM gap can be reduced by increasing the global dummy line density. Hence, the EM lifetime is reduced as the number of more local dummy increases, because the dimensions of Cu lines are reduced. On the other hand, EM performance is also a strong function of the global dummy layout.

3.1.2. Effect of the global dummy layout

To study further the effect of the global dummy layout on electromigration, the Cu tested lines with two local dummy lines: various global dummy metal densities with a 50 $\mu m \times 50~\mu m$ area were used and to the EM behaviors compared. Fig. 7 plots the cumulative lognormal distribution of the EM failure times. Similarly, the slope of the EM cumulative failure time distribution is almost parallel, indicating that the failure mechanisms are similar. Additionally, the EM failure time for Cu lines with the higher global dummy metal density is about double that of those with the lower global dummy metal density. This trend differs from that determined from the local dummy line effect, suggesting that the global dummy and local dummy layouts influence EM characteristics by

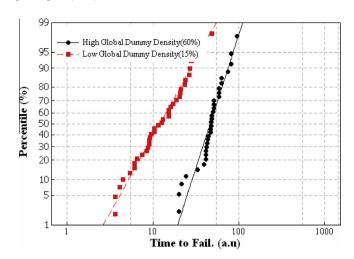


Fig. 7. Failure time distribution for various global dummy layouts for $0.063~\mu m$ width Cu metal line.

different mechanisms. Grain size analysis by TEM in Fig. 8 reveals that the metal line with the lower global dummy metal density has a lower mean grain size (~46 nm) and a higher percentage of nonbamboo grain structure (\sim 42%) as shown in Fig. 8(b). However, the Cu line with the higher global dummy metal density had a larger mean grain size (~66 nm) and less non-bamboo grain structure $(\sim 22\%)$, indicating that the global dummy layout density affects the size of grains in Cu lines. Cu lines with a larger global dummy metal density have larger grains and higher percentages of bamboo structure, resulting in longer EM failure times because of less grain boundary diffusion. Additionally, the thermal-coefficientresistance (TCR) value of the tested Cu line is proportional to the mean grain size. In a layout with a higher global dummy metal density, the tested Cu line has a larger mean TCR value (0.262 $^{\circ}$ C⁻¹), suggesting larger grains. A Cu line in a layout with a lower global dummy metal density exhibits a lower TCR value (0.220 $^{\circ}$ C⁻¹). Accordingly, the thermal-coefficient-resistance (TCR) value of the tested Cu line is an index of Cu the mean size of the Cu grains. To elucidate the proposed mechanism, electro-chemical-plating (ECP) process with a reduced deposition current is used to increase the Cu grains size in Cu lines. The mean TCR value for the layout with the lower global dummy metal density increased from 0.220 °C⁻¹ to 0.252 °C⁻¹, indicating that a modified ECP process with a reduced deposition current increases the Cu grain size. Furthermore, as expected, an increased EM failure time was observed under both global dummy densities in the reduced deposition current ECP process, as shown in Fig. 9. This result indicates that the Cu grain size affects EM performance at various global dummy metal densities. However, a modified ECP process with a reduced deposition current markedly improves EM performance, and a difference between EM lifetimes obtained using higher and lower global dummy density layouts remains. Therefore, the dummy

Table 1Normalized MTTFs at constant stress current density based on real Cu line dimensions for various local and global dummy line layouts.

MTTF (a.u)	Global dummy density = 15%		Global dummy density = 60%	
	MTTF (same stress current density based on drawn Cu dimensions)	Normalized MTTF (same stress current density based on real Cu dimensions)	MTTF (same stress current density based on drawn Cu dimensions)	Normalized MTTF (same stress current density based on real Cu dimensions)
No local dummy lines	71.16	71.16	124.25	124.25
2-local dummy lines	40.98	52.45	92.36	118.42
6-local dummy lines	18.80	30.02	67.33	107.50





Fig. 8. Dark-field TEM image of Cu lines; (a) global dummy density: 60%; (b) global dummy density: 15%.

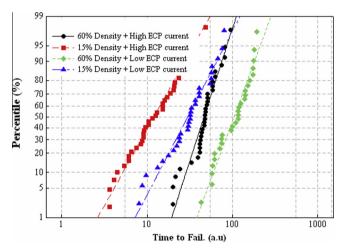


Fig. 9. Failure time distribution for various global dummy layouts with various ECP deposition currents for 0.063 μm width Cu metal line.

layouts must be considered in evaluating the EM reliability in 40 nm and below technologies.

3.2. Mechanism by which dummy layout effects electromigration

In a local dummy layout, the low-k dielectrics etching micro loading effect becomes obvious as the width of the metal line is reduced. For a 0.063 µm-wide Cu line with more dummy lines, the etching rate of the low-k film becomes lower because less etchant has difficulty in diffusing into smaller Cu holes and more etching byproduct has difficulty in diffusing out of the condensed structures. Consequently, the width and thickness of the Cu line is reduced as the number of the local dummy lines increases, as presented in Fig. 10. With respect to the effect of the global dummy layout, a structure with a larger dummy metal density includes more current dispersion paths during the Cu ECP deposition process, resulting in a larger Cu grains associated with a lower Cu deposition rate. In a structure with a lower dummy metal density, a higher current is implemented on the Cu EM tested lines during the Cu ECP deposition process because fewer current dispersion sites are resent, as shown in Fig. 11. This higher ECP current results

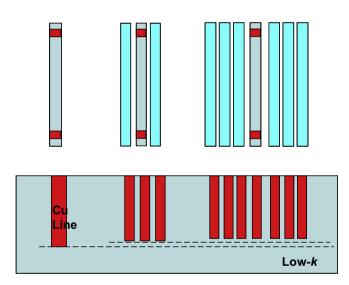
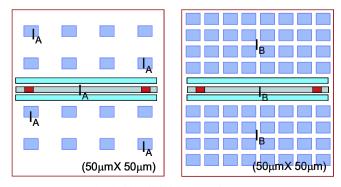


Fig. 10. Mechanism of etching micro-loading effect by local dummy lines for 0.063 μm width Cu metal line.



 $I_A > I_B$ ($I_{total}(ECP)$ =constant)

Fig. 11. Mechanism of ECP process current dispersion effect by global dummy lines; a higher current through the stressed line with a low global dummy density results in a smaller grain size and a shorter EM failure time.

in smaller Cu gains in the Cu lines because insufficient time is available to grow larger Cu grains in constrained Cu lines.

4. Conclusions

The electromigration characteristics associated with various surrounding dummy layouts in the copper interconnect with different metal widths were explicated in this study. As metal width is below 0.1 μm , the electromigration performance of dual damascene Cu lines was greatly affected by the layout that surrounded the tested EM lines. The EM failure time decreased as the number of local dummy lines increased and the global dummy line density decreased, when the width of the Cu line was below 0.063 μm . Mechanisms of Cu line etching loading and ECP dispersion effects were proposed to explain the EM behaviors. Modifying the ECP process by reducing the deposition current effectively way to weakened this effect. Based on this investigation, any assessment of EM reliability in a real IC circuit should take into account the stressed Cu line and the surrounding layout in 40 nm or below technologies.

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References

- [1] S. Yokogawa, H. Tsuchiya, Jpn. J. Appl. Phys. 44 (2005) 1717.
- [2] M.A. Hussein, J. He, IEEE Trans. Semicond. Manuf. 18 (2005) 69.
- [3] S. Thrasher, M. Gall, C. Capasso, P. Justison, R. Hernandez, T. Nguyen, H. Kawasaki, AIP Conf. Proc. 741 (2004) 165.
- [4] C.S. Hau-Riege, A.P. Harathe, V. Pham, in: 41th Annual International Reliability Physics Symposium, (2003) 173.
- [5] I.A. Blech, Jpn. J. Appl. Phys. 47 (1976) 1203.
- [6] P.C. Wang, R.G. Filippi, Appl. Phys. Lett. 78 (2001) 3598.
- [7] J.J. Clement, Trans. Device Mater. Reliab. 1 (2001) 33.
- [8] S. Yokogawa, Jpn. J. Appl. Phys. 43 (2004) 5990.
- [9] C.W. Kaanta, S.G. Bombardier, W.J. Cote, W.R. Hill, G. Kerszykowski, H.S. Landis, D.J. Poindexter, C.W. Pollard, G.H. Ross, J.G. Ryan, S. Wolff, J.E. Cronin, in: Proc. of IEEE VLSI Multilevel Interconnect Conference, IEEE (1999), p. 144.
- [10] K. Abe, H. Onoda, J. Vac. Sci. Technol. B21 (2003) 1161.