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Amorphous bilayer TiO_2–InGaZnO thin film transistors with low drive voltage

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ABSTRACT

This paper describes a high-performance thin-film transistor (TFT) fabricated using TiO_2 and InGaZnO semiconducting layers. Favorable transistor characteristics, including a low threshold voltage of 0.45 V, a small subthreshold swing of 174 mV/decade, and a high field effect mobility of 19 cm^2/V s at a low drive voltage of <2 V, were achieved. This favorable performance mainly resulted from the combined effect of the high-dielectric-constant gate dielectric and the TiO_2–InGaZnO active semiconductor bilayer, which reduced the operating voltage, enhanced the device mobility, and improved the transistor gate swing. This TiO_2–InGaZnO TFT exhibits great potential for future high-speed and high-resolution display applications.

1. Introduction

Low-temperature indium–gallium–zinc oxide (IGZO) thin-film transistor (TFT) devices have attracted a substantial amount of attention because they require a low process temperature and feature high mobility and a high drive current. Compared with poly-Si TFTs, which require a high thermal budget, IGZO TFTs can achieve high-performance transistor characteristics at low process temperatures, ensuring greater performance uniformity and device reliability. Furthermore, studies have been demonstrated that low-temperature IGZO TFTs fabricated using high-dielectric-constant (κ) gate dielectrics [1–7] can be integrated with high-resolution organic light-emitting diodes (OLEDs) to develop high-quality display technologies that are large in area and feature low power consumption.

IGZO-TFT-driven active-matrix OLEDs (AMOLEDs) have been applied to high-resolution displays [8–10], but such applications have been hindered by critical problems regarding transistor characteristics, such as a large subthreshold swing (*SS*) and low device mobility, which must urgently be addressed to enable them to be applied in high-resolution displays. Although increasing the gate dielectric thickness can suppress gate leakage, the high operating voltage necessary to increase the driving current is unavoidable. In addition, the low device mobility and high-voltage operation of IGZO TFTs are unsuitable for driving OLEDs, which require a high current and low power consumption.

A TFT using a TiO_2 semiconducting channel was recently reported. This TiO_2-channel TFT exhibited a high electron mobility of >16 cm^2/V s and a large on–off ratio of >10^6, but a high operating voltage of 40 V [11]. In our recent work, we used Ti-doped IGZO as channel capping layer to improve the transfer characteristics of TFT devices based on an oxygen gettering scheme with a thermal budget of 300 °C [12]. This experimental work exhibited promise for future application. However, the composition control of IGZO:Ti was difficult, and also the gettering effect could not work efficiently below 300 °C, which limited the application on flexible substrate. In this study, a high-performance bilayer IGZO TFT was fabricated by integrating with a room-temperature TiO_2 channel capping layer. The high transmittance in visible-light range, room temperature process and simple composition of TiO_2 layer make it very attractive for channel application of flexible electronics. The TiO_2–IGZO TFT achieved favorable transistor characteristics, namely a low threshold voltage (V_T) of 0.45 V, a small *SS* of 174 mV/decade, and a high field effect mobility (μ_{FE}) of 19 cm^2/V s under a low drive voltage (V_G–V_T) of <2 V. This improvement in performance is attributable to the stacked channel structure enabled by the incorporation of the room-temperature TiO_2 semiconductor, which not only lowers the *SS* and the off-current V_T but also enhances the I_{on}/I_{off} ratio and device mobility.

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2. Experimental details

A bottom-gate TFT was fabricated on a 200-nm-thick insulating SiO_2 substrate. A 35-nm-thick bottom TaN gate electrode was deposited using a sputtering system. Subsequently, a 25-nm-thick TiO_2 layer and a 30-nm-thick HfO_2 layer (bilayer HfO_2–TiO_2 gate dielectric) were deposited using electron beam evaporation and annealed at a low temperature, 300 °C, to initiate dielectric activation. Afterward, 15-nm IGZO was deposited in a gas mixture of 30% O_2 in an Ar ambient, and 8.5-nm-thick and 15-nm-thick TiO_2 layers were deposited at room temperature to form bilayer TiO_2–IGZO structures. The control single-layer IGZO channel was fabricated to facilitate performance comparison. Finally, a 300-nm-thick Al film was evaporated and patterned to form source and drain contacts. The patterned channel size was 530 μm × 45 μm. The electrical characteristics of the IGZO TFT devices were characterized using current–voltage (I–V) and capacitance–voltage (C–V) measurements that were acquired using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

3. Results and discussion

First, the metal-insulator-metal (MIM) capacitor of the Al/HfO_2/TiO_2/TaN was measured to evaluate the film quality of the gate dielectric. The measured capacitance density of the MIM capacitor was approximately 0.34 μF/cm^2 at 100 kHz (not shown), yielding an acceptable dielectric constant (κ value) of 20. A TiO_2 dielectric with high crystallinity can be activated at a low temperature of 300 °C [12] and can reach a high capacitance density because of its extremely high κ values of 40–60 [13,14]. A high capacitance density and small capacitance equivalent thickness have the benefit of reducing the operating voltage (V_{OP}) and V_T. However, amorphous TiO_2 with a narrow bandgap of 3.05 eV and a small conduction band offset (ΔE_C) of only 0.05 eV [15,16] may induce a large gate leakage current, especially when the gate voltage is increased to achieve a high driving current. Furthermore, the Ti-terminated surface or weak Ti–O bond between the gate dielectric and channel interface generates shallow traps that degrade device mobility following an incomplete oxidation process. Notably, the gate leakage of a TiO_2 dielectric becomes less temperature dependent when the annealed temperature is processed below 300 °C [13], enabling a high capacitance density to be reached by using a low-temperature TFT process. To prevent interface defects, a bilayer HfO_2–TiO_2 dielectric structure was adopted. The HfO_2 layer features a large bandgap of >6 eV and a high ΔE_C of >2.3 eV [17] in contact with IGZO channel; thus, it serves as an effective buffer layer and reduces trap-induced leakage paths near the interface. High-κ TiO_2, which can be activated at a low temperature, is also a potential candidate for low-temperature flexible display applications [18–20].

Fig. 1(a) and (b) shows the output I_d–V_d and transfer I_d–V_g characteristics of a conventional single-layer (SL) IGZO TFT, respectively. The SL-IGZO TFT device exhibited an SS of 331 mV/decade, a mobility of 3 cm^2/V s, and a V_T of 0.63 V at a drive voltage of 3 V. The SS was linked to the interface trap states (D_{it}) and interface charge capacitance ($C_{it} = qD_{it}$), which were calculated based on the equation $SS = kT/q \times ln10 \times [1 + (C_b + C_{it})/C_{ox}]$, where C_{ox}, C_b, and C_{it} are the gate oxide capacitance, bulk capacitance, and interface charge capacitance, respectively. Therefore, to achieve a low SS, C_{it} must be minimized and a high gate capacitance must be ensured. Based on the transistor characteristics, the low device mobility and large SS cannot meet the basic requirements for AMOLED application and must to be improved urgently. The

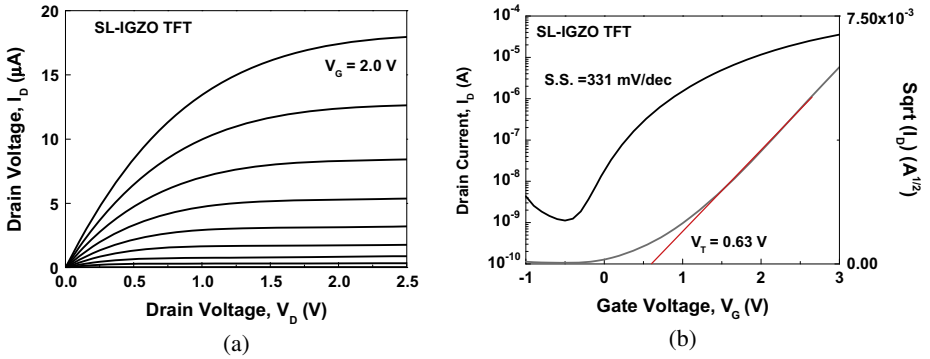

Fig. 1. (a) I_d–V_d and (b) I_d–V_g characteristics of conventional SL-IGZO TFT device. V_T can be extracted by linear extrapolation from the square root of drain current as a function of gate voltage.

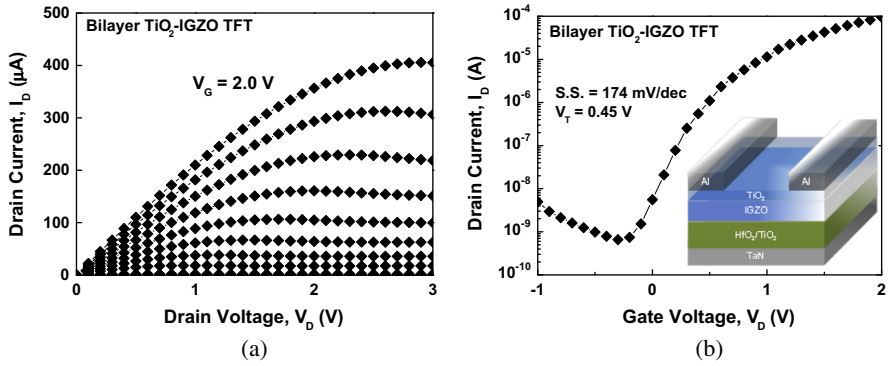

Fig. 2. (a) I_d–V_d and (b) I_d–V_g characteristics of TiO_2(15 nm)–IGZO TFT device. V_T can be extracted by linear extrapolation from the square root of drain current as a function of gate voltage. The inset of (b) is the schematic structure of TFT device.

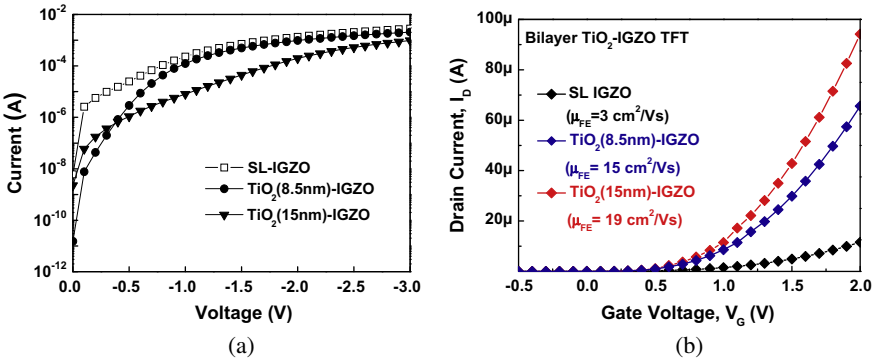

Fig. 3. (a) I–V curves of SL-IGZO and bilayer TiO_2–IGZO. (b) I_d–V_g characteristics of SL-IGZO and TiO_2–IGZO TFT devices, respectively.

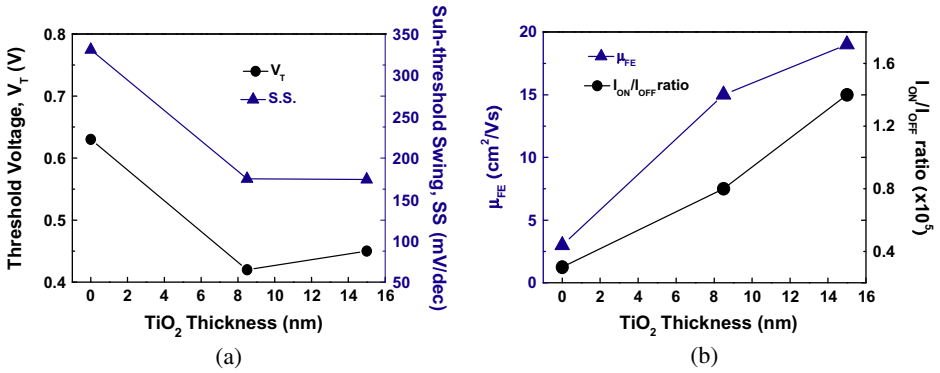

Fig. 4. (a) Threshold voltage, sub-threshold swing, (b) field-effect mobility, and I_{on}/I_{off} ratio as a function of TiO_2 thickness for TiO_2–IGZO TFT devices.

channel carriers are dominated by oxygen vacancies in the IGZO active layer and the reaction equation can be expressed as follows: $IGZ\text{-}O_x + V^{2+}_{IGZ\text{-}Ox} + 2e^- \rightarrow IGZ\text{-}O^*_x$. Here, $V^{2+}_{IGZ\text{-}Ox}$ are the oxygen vacancies in IGZO that influence the channel mobility and off current. Although oxygen vacancies can be controlled through appropriate in situ annealing or post-deposition annealing, modifying the compound ratio and oxygen concentration accurately is difficult, especially in the fabrication of a low-temperature and multi-element thin films.

Fig. 2(a) and (b) shows the I_d–V_d and I_d–V_g characteristics of the bilayer TiO_2(15 nm)–IGZO TFT. The inset of Fig. 2(b) shows the schematic structure of the bilayer TiO_2–IGZO TFT device. Favorable I_d–V_d transistor output characteristics were observed at an even bias and a low V_{OP} of 2 V. Compared with the control SL-IGZO TFT, the bilayer TiO_2–IGZO TFT exhibited a low SS of 174 mV/decade, which was much lower than the 331 mV/decade of the control SL-IGZO TFT. This small SS is supported by the low V_{OP} of 2 V and the V_T of 0.45 V. To realize the goal of a low-power green transistor, both the dc power and ac switching power ($C_S V_D{}^2 f/2$) must be reduced [21,22]. Here, C_S, V_D, and f are the switching capacitance, drain voltage, and operation frequency, respectively. The transistor must be operated using a low V_D and V_T to lower the AC switching power. Therefore, improving V_T and V_{OP} is critical for applying this transistor in large-area displays.

Fig. 3(a) and (b) shows the I–V curves and I_d–V_g characteristics of the SL-IGZO TFT and the bilayer TiO_2(15 nm)–IGZO TFT, respectively. The TiO_2(15 nm)–IGZO TFT exhibited a considerably lower leakage current than did the SL-IGZO TFT; this result is attributable to the TiO_2 semiconductor layer with a high κ value, which modified the local field effect near the source/drain sides, thereby lowering the channel leakage. By effectively controlling the channel leakage, the off-current and SS can be greatly improved. Furthermore, the μ_{FE} was further improved from 3 cm^2/V s to 19 cm^2/V s by using TiO_2 layers of various thicknesses.

The transistor parameters of TiO_2–IGZO TFT devices, including the V_T, SS, μ_{FE}, and I_{on}/I_{off} ratio, are shown in Fig. 4(a) and (b) as a function of TiO_2 thickness. Compared with the control SL-IGZO TFT, the TiO_2–IGZO TFT featured considerably enhanced performance, with a low V_T of 0.45 V, a small SS of 174 mV/decade, a large μ_{FE} of 19 cm^2/V s, and an I_{on}/I_{off} ratio of 1.4×10^5. Therefore, the use of a TiO_2 semiconductor layer was proved to improve the transistor characteristics, especially device mobility and gate swing, that are essential to high-speed and high-resolution display applications.

4. Conclusion

A high-performance TiO_2–IGZO TFT incorporating a TiO_2 semiconductor layer was demonstrated. The TiO_2–IGZO TFT exhibited favorable device integrity, and achieved a low V_T of 0.45 V, a small SS of 174 mV/decade, and a high μ_{FE} of 19 cm^2/V s at a low drive voltage of <2 V. Depositing TiO_2 at a low temperature to improve transistor characteristics differs from other channel modulation approaches such as plasma treatment, which requires a high thermal budget, and may be useful in potential applications for high-resolution flexible displays that require a low-temperature process.

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