Microsyst Technol (2014) 20:1583–1595
DOI 10.1007/s00542-014-2179-7

TECHNICAL PAPER

Design and realization of a high resolution (640 × 480) SWIR image acquisition system

Jian-Ruei Chen · Paul C.-P. Chao · Che-Hung Tsai · Wei-Dar Chen

Received: 30 October 2013 / Accepted: 10 April 2014 / Published online: 3 May 2014

Abstract A new image acquisition system module for extracting signals of high-resolution short wave infrared (SWIR) from a focal plane array (FPA) is presented in this study. The short wave infrared (SWIR—with wavelength about 900–1,700 nm) images have been proven its unique values in many applications such as military, semiconductor inspection and aviation security. The designs for the SWIR data acquisition system module consists of digitization and acquisition of FPA signals, design of synchronous dynamic random access memory controller and real-time image signal transformation and display. Three major steps involved towards a successful SWIR module—(1) Selection of hardware ICs according to specification for the FPA; (2) Design of a timing generator for the image acquisition system to control FPA and other ICs by Verilog HDL programming; (3) Integrate the individual modules on a PCB. The SWIR image output signals are successfully generated in the format of National Television System Committee (NSTC), which can be displayed on a common NTSC monitor, flat panel displays with an AV input terminal or a CRT display in a favorable speed of frame rate at 30 per second.

1 Introduction

Imaging technology has been investigated in revolutionary progresses for decades (Li et al. 2013; Wang et al. 2013) with well-developed semiconductor and memory industries. Silicon sensors are used in most of cameras and digital video-recorders (DVs), since silicon is the best material for visible light imaging (wavelength from 400 ~ 700 nm). Short wave infrared (SWIR) imaging however requires indium gallium arsenide (InGaAs), which is composed of chemical compounds including indium arsenide (InAs) and gallium arsenide (GaAs), to cover SWIR spectrum. Wavelength of typical SWIR is defined between 0.7 and 2.5 μm. Typical SWIR cameras focus on the wavelengths between 0.9 ~ 1.7 μm ($In_{0.53}Ga_{0.47}As$). Unlike mid-wave IR and long-wave IR, SWIR is reflected and absorbed by objects, which advantages SWIR imaging in higher resolution due to better contrast. SWIR also has excellent imaging quality in low illumination environment, like when moon or star lights are good outdoor emitters at night. Another primary characteristic of SWIR is high penetration, providing effective imaging under hazy conditions. An example for night vision between SWIR and visible imaging is shown in Fig. 1 (Hansen and Malchow 2008), where it is obvious that an SWIR camera can see much more than a visible imaging camera.

The SWIR array imagers are usually not available for academic research. Among previous researches, no documents revealed the design of an SWIR image acquisition system. Most of the studies, focusing on image acquisition, CCD/COMS sensor modules were applied. Owing to well-developed semiconductor techniques, productions of CCD/CMOS can be provided with excellent quality at reasonable price. The image sensor modules are also available and highly-reliable. In early-2000's, researches about image acquisition were usually based on DSP-based platform. Engineers of Texas Instruments, Illgner et al. (1999) brought out DSP-based digital camera. The camera captured a frame of million-pixel CCD image in 1.5 ms, in which image compression function was also added. Lehtoranta et al. (2002) used four DSP systems

J.-R. Chen · P. C.-P. Chao (✉) · C.-H. Tsai · W.-D. Chen
Department of Electrical Engineering,
National Chiao Tung University, Hsinchu 300, Taiwan
e-mail: pchao@mail.nctu.edu.tw

Fig. 1 SWIR and visible imagings (Hansen and Malchow 2008)

and achieved parallel processing. The image data was encoded by the system and transmitted by wireless techniques. Chen (2004) realized a CCD image acquisition system with a CMOS sensor module (ICM-105B, A/D converter embedded), an image buffer (AL422B) and a DSP platform (TMS320 C6713DSK). It takes 505.295 ms for acquiring an image resulted from R/W redundant delay of AL422B. As it approached 2010, high-end FPGAs made real-time image acquisition feasible, where the main purpose of the adopted DSP is to perform image processing algorithms. Some DSPs had embedded functions, deriving real-time images from camera (or DV) for the convenience of digital image process (DIP). Hang (2010) accomplished image acquisition (from camera) and DIP algorithm, such as image threshold segmentation and edge detection. Yan et al. (2011) designed an acquisition system for camera with camera link data interface. The system was capable of acquiring 1.3 million-pixel image (from camera) at the speed of 25 frames/s. To achieve higher data transmission rate, the USB2.0 was used as the interface between FPGA and PC. Huang et al. (2009) proposed a system design for the CMOS sensor, which was most similar to the objective of our study (acquiring raw data directly from image sensor module/chip, but not from camera). However, the design was incomplete and only simulation result by ModelSim was presented.

In our study, a new and complete 640 × 480 SWIR real-time image acquisition system module is designed and realized based on the 640 × 512 FPA and an FPGA platform. Real-time image acquisition and display up to frame rate of 30 s are successfully accomplished without image distortion and delays. This paper is organized as follows. Section 2 describes the hardware system and modules. Section 3 states the integration between individual modules to a system. Section 4 gives the details in control software, algorithm and operations. Section 4 presents the experimental results.

2 Designed SWIR image acquisition system

A module of 640 × 512 SWIR FPA is chosen as a core imaging device for this SWIR image acquisition system. To operate this FPA, an FPGA platform for designing a timing generator is pre-requisite, which is also used for other devices in the system. As signals must be digitized for data acquisition, a high sampling rate ADC is utilized for FPA output. In this SWIR system, a chip-scale video encoder is implemented to perform data conversion from CCIR656 to NTSC format. A buffer module including a synchronous dynamic random access memory (SDRAM) and FIFO is used to integrate front-end and back-end devices. The entire structure of the designed SWIR image acquisition is shown in Fig. 2.

2.1 640 × 512 Focal plane array and analog to digital converter

The high-performance 640 × 512 InGaAs FPA is considered for this academic research work. InGaAs sensors are fabricated with capacitive trans-impedance amplifier (CTIA) as the readout circuit in the size of unit cell as 25 × 25 μm. Primary features of this FPA include 640(H) × 512(V) array format, spectral range 0.9–1.7 μm,

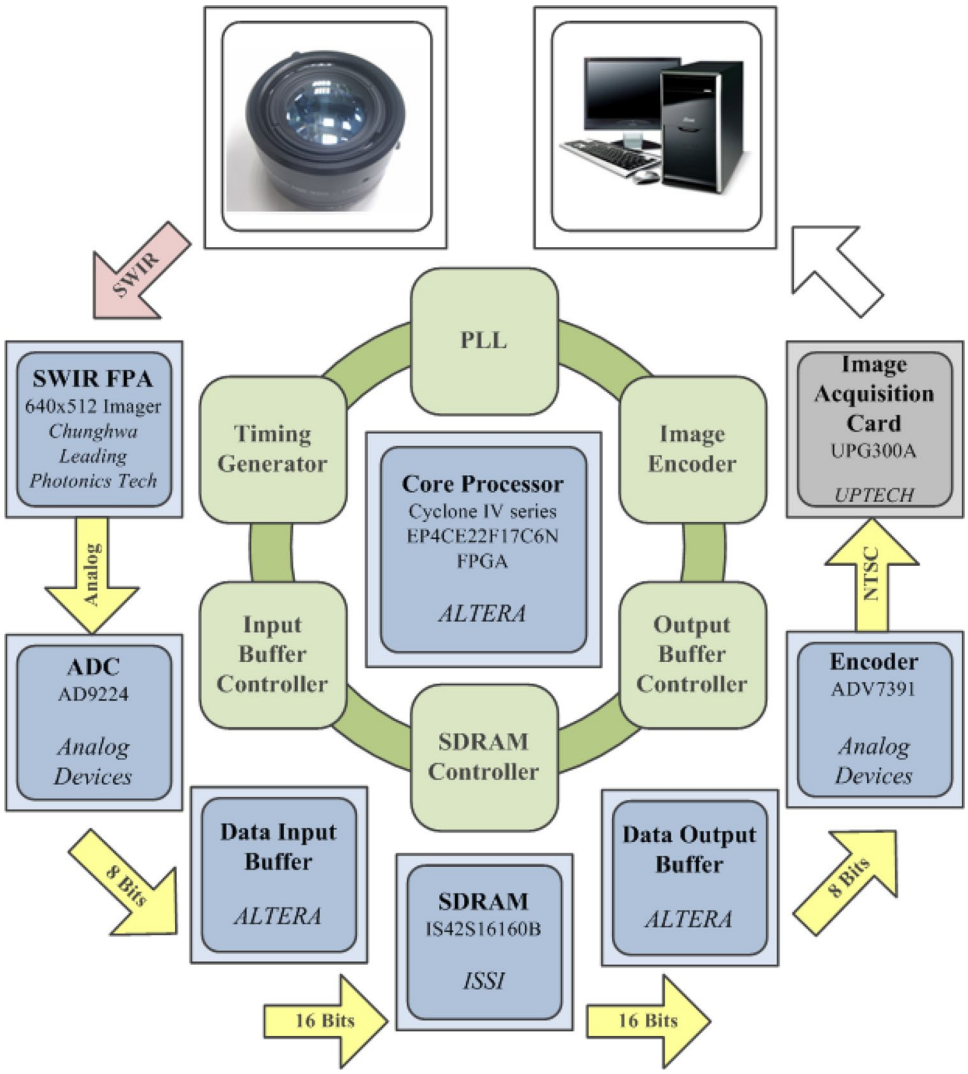

Fig. 2 Structure of the proposed 640 × 512 SWIR image acquisition system

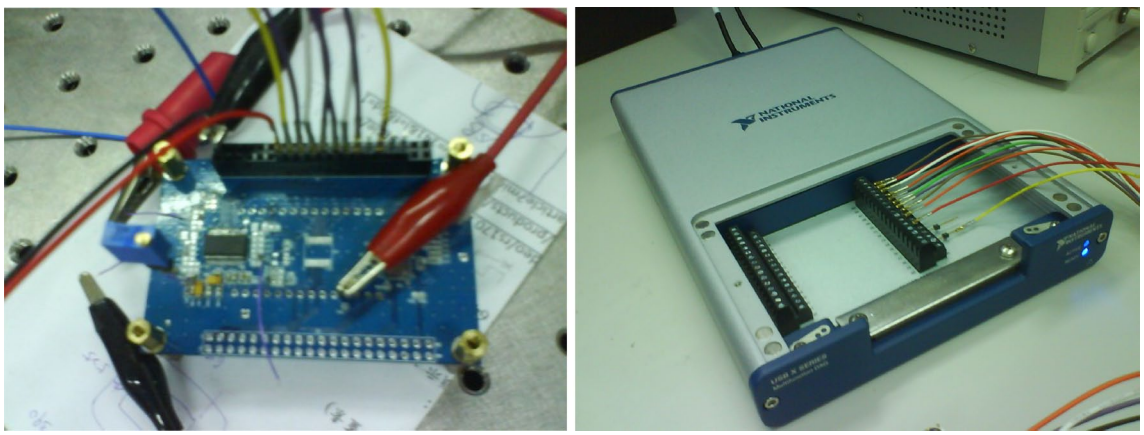

Fig. 3 The ADC and DAQ used in the reliability test experiment

a 28-pin metal DIP package, an embedded thermoelectric cooler, typical pixel operability >99.5 % and quantum efficiency >70 %. This sensor array module is designed for industrial purposes, covering NIR-infrared imaging, covert surveillance, semiconductor inspection, medical science/biology, astronomy and moisture mapping.

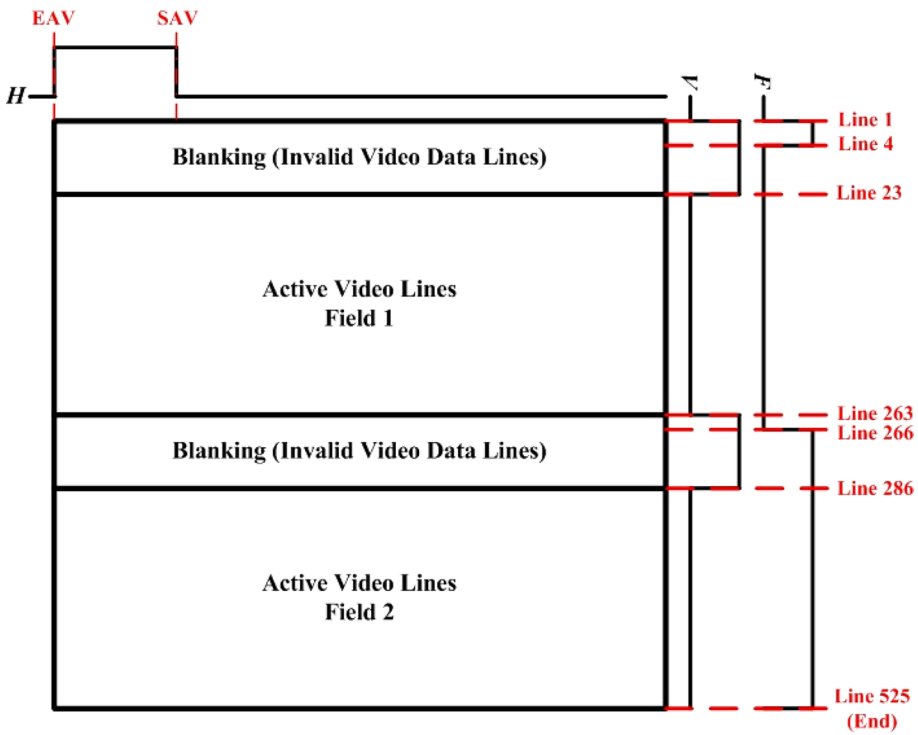

Fig. 4 A frame in the CCIR656 525: line standard and signals of H, F and V

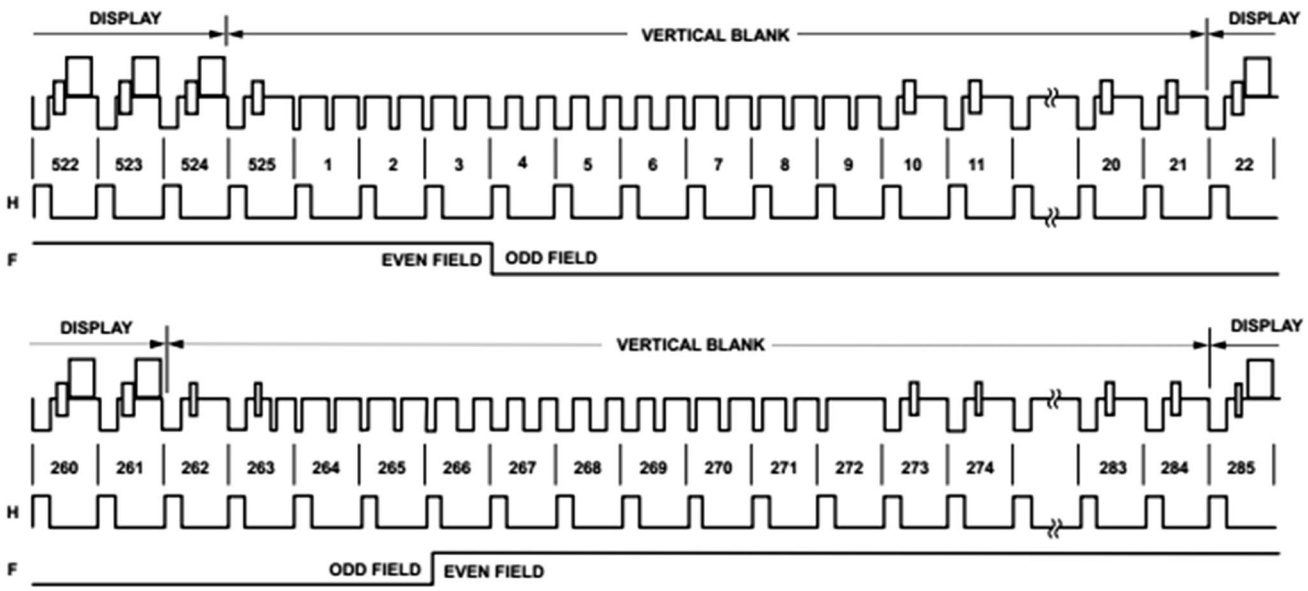

Fig. 5 Video lines and vertical blank of the CCIR656 format (Analog Devices, Inc. 2013)

AD9224 is selected as AD converter in the system, which is capable for 10 MHz (up to 40 MHz) sampling rate to match output speed of FPA. The 28-pin SSOP package ADC has 12-bit resolution (most significant 8 bits are used in our design) and multistage differential pipelined architecture featuring error correction logic. A variety of input ranges can be applied for input of AD9224; for above reasons, this ADC is very suitable for imaging applications. In this study, a small experiment for testing ADC's reliability is presented. A data acquisition card (DAQ) is used to design the acquisition procedure via LabVIEW (Ver. 8.6) programming. A function generator is analog voltage source in this experiment. The testing waves including sine, square and ramp are digitized by ADC and the digital

outputs are acquired by DAQ. In the same time, function of LabVIEW recovers captured digital data to continuous waveform, which should be complete and smooth. Spikes are not acceptable since they might be judged as bed pixels in back-end DIP. To reduce noise, the ADC is implemented on a PCB (Fig. 3) with biases and structure mentioned above.

2.2 Memory module and image encoder

Since the pixel rates of the FPA and NTSC encoder are different, a memory module composed of an SDRAM (Integrated Silicon Solution, Inc. 2008) and FIFO is adopted to keep digitized data available and intact for the image encoder. An SDRAM has shorter read/write period than a DRAM, on account of memory interleaving and multi-pipeline technique. The complete operations of the SDRAM are set into action by numerous commands along with address to locate read/write positions. Nowadays, SDRAM advantages in cost, size, memory volume and speed, usually being the best choice in portable device. Unlike SDRAM, FIFO buffers can read/write data under different frequencies. For example, data from ADC is written to FIFO_IN at speed of pixel rate (10 MHz) and read by SDRAM (108 MHz). Generally, an SDRAM operate at million hertz and need a FIFO to make it efficient, which means SDRAM do not perform read/write command in most of time.

ADV7391 is selected as a high-speed, digital-to-analog converter in the system, which is applied to transform the digital pixel data from CCIR656 format to NTSC image signals. The 32-pin lead frame chip scale package (LFCSP) of an image encoder features minimal footprint (5 × 5 mm), low-power consumption and few external components required. Either by standard definition (SD) or high definition (HD) video formats, this device is capable of analog image outputs, including composite (CVBS), S-Video (Y-C), and component (YPrPb/RGB). ADV7391 also supports embedded end/start of active video (EAV/SAV) codes and I^2C communication protocol, applied in our design.

2.3 CCIR656 image format

According to Rec. ITU-R BT.656-4 (DE0-Nano User Manual 2011), namely CCIR656, this recommendation supports both 525-line and 625-line systems with YC_BC_R–4:2:2 color space. Based on the gray level and 512-line image data of the FPA, 525-line standard and a fixed value for C_B and C_R are applied in the design. The 480 active lines and 45 blanking lines compose a complete frame. A frame (line 1 ~ 525) is divided into two fields, where field1 starts from line 4 to 265 and other lines are defined as in field 2. Besides, two blanking intervals (namely vertical blanking) cover line 1–22 and line 263–286. The *F* synchronization signal for field identification should be 0 in field 1, and 1 in field 2. The *V* synchronization signal for field blanking identification turns to high during blanking lines. The afore-definitions are illustrated by Fig. 4. Active and non-valid data lines of the CCIR656 format are illustrated in Fig. 5. A typical image frame is composed of 480 active video lines (240 lines/per field). In the designed system, there are 512 lines in the focal plane array (256 lines/per field). Thus, to match the format between FPA and CCIR656, some of valid lines of the FPA must be seen as non-valid video lines (16 lines/per field). Both fields of an FPA image, the first 16 lines are chosen as non-valid lines in CCIR656 standards, and 17th ~ 252th lines should fit in with 240 active video lines (22th ~ 261th lines for the odd field and 285th ~ 524th lines for the even field in CCIR656 image frame, respectively). Note that the number of default blank lines of the FPA is five and they are added to nine to match CCIR656 standard.

The coding characteristics of a line focus on timing codes in horizontal blanking and composition of a pixel data, as illustrated in Fig. 6. A pixel data at 13.5 MHz includes two pieces of 8-bit data. The stream of active data starts with red color reference, CB. The sequence of video data is defined in the following order, CB, Y, CR, Y, CB, Y, CR,…, etc., which is an image word containing a Y (luminance) and a C (color-difference), either CB or CR. Above co-cited pixel data—CB, Y and CR reveals that both CB and CR are shared with adjacent luminance in horizontal direction. Horizontal blanking in a line occupies 138-pixel periods (276 8-bit data words), where the H synchronization signal for horizontal blanking identification turns to high; Also, the first/last two words carry the timing codes of end/start of active video (EAV/SAV). Both EAV and SAV are in the sequence of 8'hFF, 8'h00, 8 h'00 and 8'hXY. The 8-bit status word XY is shown in Table 1 ($\oplus$: Exclusive-OR operator). The synchronization signals mentioned above are essential information in EAV and SAV that are also used to generate protection bits, enabling most 2-bit errors to be detected. Between EAV and SAV are ancillary data for non-video information such as audio data, teletext and captioning. Without those functions in our system, data in the sequence of 8'h80, 8'h10 are filled in repeatedly. Owing to EAV and SAV, no external synchronization signal is needed for operations of the image encoder.

3 Hardware integration of SWIR image acquisition system

The core processor and SDRAM are included in the DE0-Nano board (2011). The DE0-Nano board is a compact-sized development platform with a USB blaster for FPGA

programming. To integrate selected sub systems to be an independent system, a printed circuit board (PCB) is designed. Two 40-pin connectors (pitch 2.54 mm) via PCB DIP solders are built on the board to match two 40-pin GPIO headers of the DE0-Nano board, providing channels between core processor and components on PCB. Besides, another 40-pin connector on PCB is used as the system is under test by another development platform, called DE2-115 (core processor: Cyclone IV EP4CE115F29C7N). One push button is used to reset the image encoder ADV7391. Primary power sources with biases of 5.0 and 3.3 V are supplied by the DE0-Nano board. Other biases, such as 1.8 V for pin *PVDD*, *VDD0* and *VDD1* of ADV7391 and 1.6 V for pin VOUTREF and VOS of FPA, are provided by low-dropout linear regulators [LDO, TPS79318D-BVR (Ultralow-Noise 2004) and TPS72216 (Low Input Voltage 2002)]. Besides, two trimming potentiometers are applied, determining the cross voltage of the InGaAs sensor (*VREF*: 2.5 V and *VDETCOM*: 3.0 V, reverse bias: 0.5 V). Note that pull-up resistors are essential for both pin *SCL* and pin *SDA* of ADV7391. The layouts of this PCB is shown in Fig. 7.

The finished hardware of the designed PCB is shown in Fig. 8. All components, including FPA, ADC, octal transceiver, image encoder and passive elements are well integrated with the PCB. DE0-Nano and DE2-115 can be connected with this PCB as well. In addition, the system can operate with each of them. The DE2-115 is applied during debug and modification stages, providing larger memory size as the embedded logic analyzer –SignalTap II is under operations (Altera Corporation 2012). Each part of the system module has been checked if in normal functions by the experiments performed above, including output of FPA, reliability of ADC, artificial image acquisition and display NTSC coding.

4 FPA (640 × 480) SWIR image acquisition and display (NTSC)

The finished image acquisition system is presented in previous sections. For imagining, an optical IR lens is added along with the camera. In this section, the designed SWIR image acquisition system module is used to shoot images.

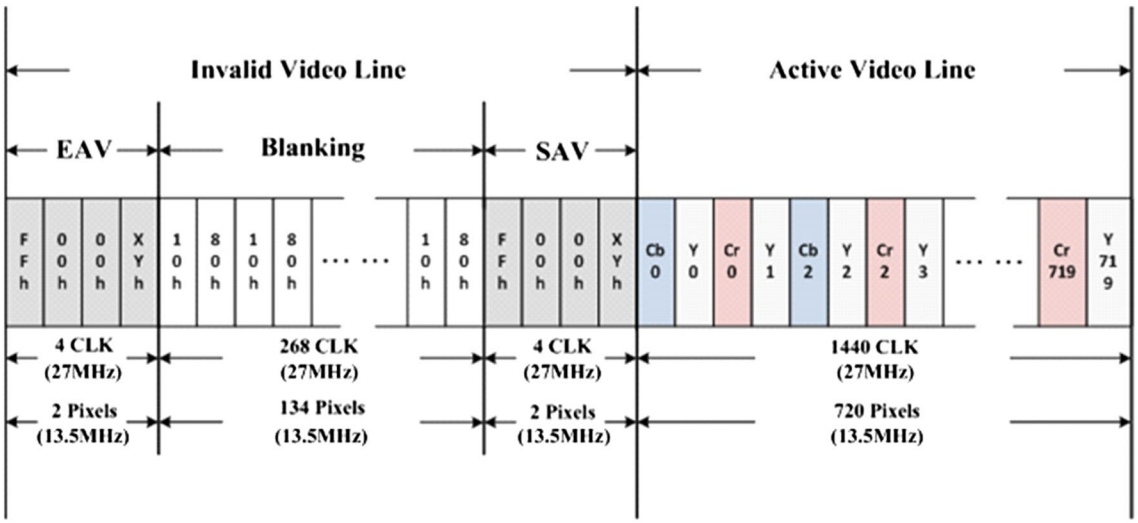

Fig. 6 Coding characteristics of a line in the CCIR656 format

Table 1 Status words of the CCIR656 EAV and SAV codes

	8-bit Data							
	Bit-7 (MSB)	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0 (LSB)
Status word (XY) of (EAV/SAV code)	1	F	V	H	P3	P2	P1	P0
P3	V ⊕ H							
P2	F ⊕ H							
P1	F ⊕ V							
P0	F ⊕ V ⊕ H							

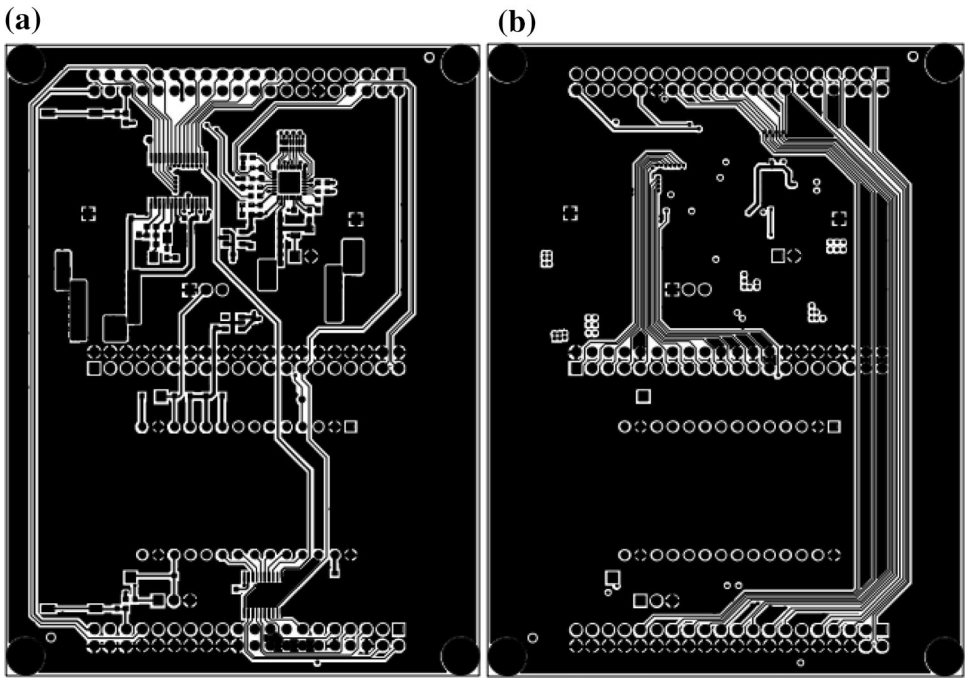

Fig. 7 PCB layout **a** *top view*; **b** *bottom view*

Resulted videos are coded in NTSC format and displayed by a PC with the UPG300A module or an independent monitor with an analog video signal input terminal.

4.1 Additional characteristics of FPA

4.1.1 Quantum efficiency (QE) of InGaAs sensors

The 640 × 512 SWIR FPA detects the spectrum from 0.9 ~ 1.7 μm, where quantum efficiency is shown in Fig. 9. However, without appropriate light source, temperature of an object should be larger than 150 °C to radiate enough short wave IR for detection. Thus, welding torches are selected for evaluating the quality of captured SWIR pictures. Sunlight is also considered as an ideal light source since it covers a wide range of infrared spectrum.

4.1.2 Bad pixels and non-uniform gain of amplifier

Bad pixels are those on FPA that are not shown in normal functions as expected. They could be always saturated (2.1 V output) without illumination or always shows darkness (4.7 V output). Pixels, including sensors and attached circuits, may be damaged during semiconductor processes or scratched by accidents. Bad pixels can be fixed by some post digital image process (DIP) methods, known as bad pixel removal (BPR). The BPR usually detects locations of bad pixels, and then replaces them with the surrounding ones. Since the algorithm for BPR only focus on bad pixels, it can be executed without too much calculation.

In a column of the 640 × 512 FPA, electric signals output from sensors are amplified by the same amplifier. It is impossible that each amplifier has exact gain as designed. As a result, when sensors are illuminated under light with an even intensity, slight variations in gray levels could be observed column by column in captured results. To be compared with bad pixels, non-uniform gain is not considered as a severe problem. To acquire image with higher quality, some solutions for non-uniformity correction (NUC) could be applied.

Both bad pixels and non-uniform gains of amplifiers could be seen in Fig. 10, captured by our designed SWIR image acquisition system (without lens) under illumination and darkness, respectively. Therefore, BPR and NUC are two essential functions to improve our system as additional features. The two images in Fig. 10 also show that the full range of FPA output could be transformed to NTSC video successfully. Wu (2011) and Peng (2012) develop the algorithms for BPR and NUC. In general, the algorithms for digital image processing are realized by a digital signal processor (DSP) to be an independent sub-module. The functions of DIP are integrated to our designed system module, after accomplishments of BPR and NUC.

4.2 SWIR image acquisition and display with IR lens

The designed image acquisition system operates with an optical IR lens (LINOS Photonics) in which spectral range of the lens is 800 ~ 1400 nm, providing outstanding transmission up to 90 % in most of the wavelength ranges. Transmission rate of the selected lens is shown in Fig. 11 (inspec.x

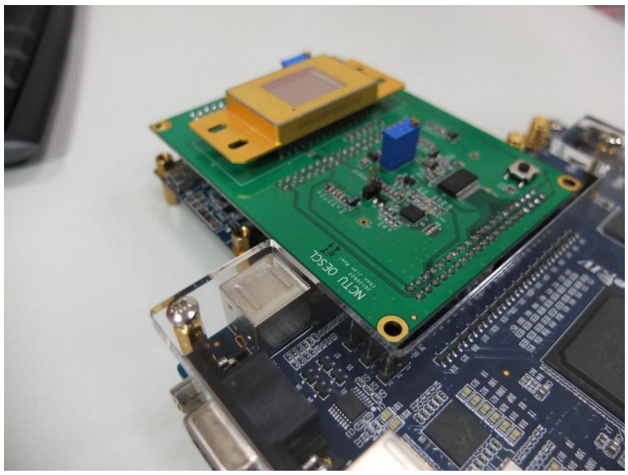

Fig. 8 The finished PCB with all selected components

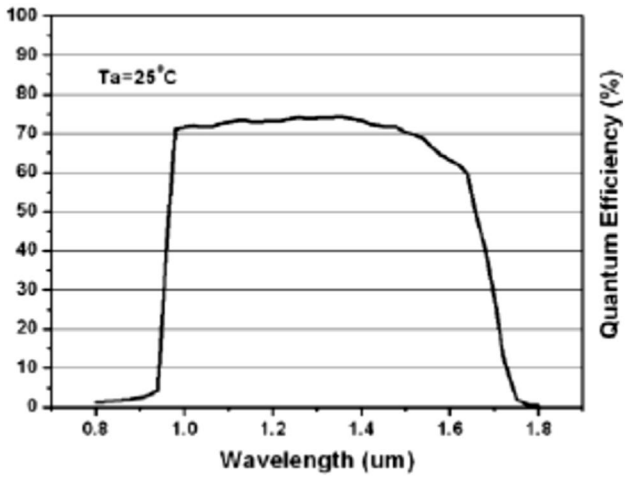

Fig. 9 The quantum efficiency of the 640 × 512 FPA (FPA-640×512 2010)

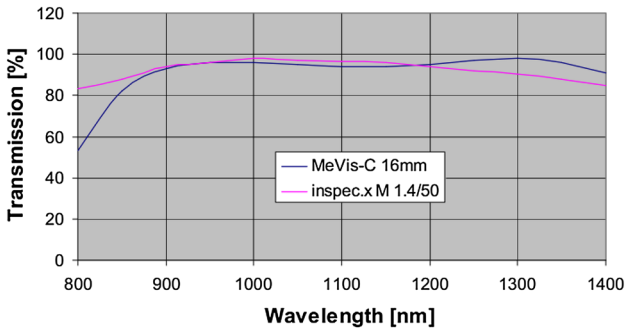

Fig. 11 Transmission of the LINOS Lion Photonics, Ltd. (2010)

M 1.4/50). Besides, the focal length is 46.5 mm and maximum aperture is 1.6. Owing to wilder sensitization region of the 640 × 512 FPA, an F-mount lens is a suitable choice for our system. According to experiment result of the lens (with a 320 × 256 SWIR image acquisition system), SWIR radiating from objects could not be detected without any illumination. To radiate enough SWIR by objects, their temperature should be higher than 150 °C. An auxiliary illumination, such as a halogens light source, is necessary to be supplied as a light source for distinct images under varied room temperatures. A simple mechanism and module is designed and manufactured by high-density foam cotton to integrate the image acquisition system and optical lens, as shown in Fig. 12. For firm and cooling reasons, it is usually metallic and some ventilation openings are orchestrated.

5 Image acquisition results

Images captured by the proposed acquisition system are presented in this section. They are in fact screenshots of

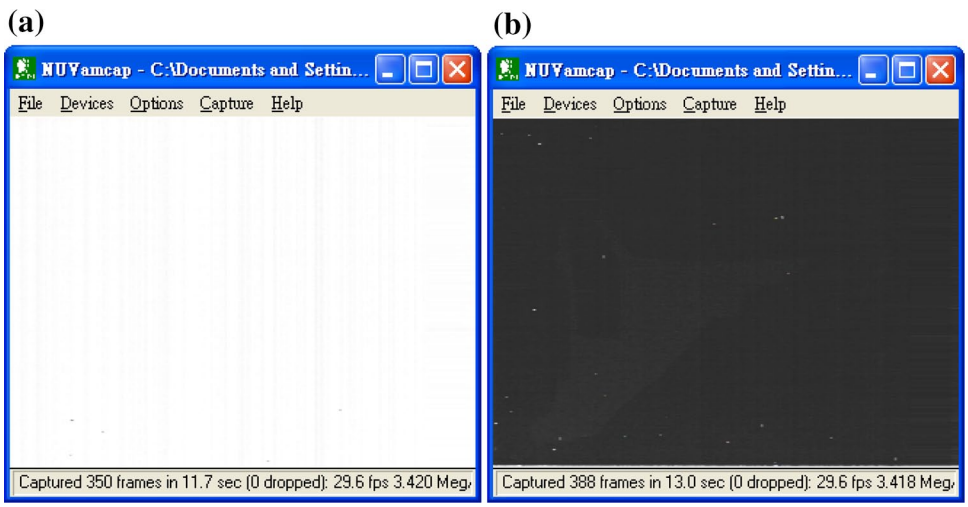

Fig. 10 Bad pixels and non-uniform gain of the amplifier in **a** *light image*; **b** *dark image*

real-time NTSC video codes in the UPG300A interface module. The images could be divided into two parts: (1) image acquisition under appropriate illumination, and (2) low illumination. Note that the integration time of the FPA is about 4.14 ms.

5.1 Image acquisition under appropriate illumination

The spectral range of sunlight covers wavelengths in SWIR. As sunlight is reflected by objects, it could be detected by FPA and then transformed into NTSC video codes through our proposed system. In processing captured results, the most interesting one is that water is black (corresponding to very low gray level) in SWIR image, shown in Fig. 13. The phenomenon results from IR absorption spectrum of liquid water, meaning that most IR energy is absorbed by water. For the same reason, the white regions of the eye is seen as black in the SWIR image as well. Other images are collected and shown in Fig. 14.

5.2 Image acquisition under low illumination

Without sunlight as background light source, objects are imaged by SWIR radiated from them. A welding torch in the environment with room temperature approximately equal to 230 °C is considered and resulted images for different temperatures are shown in Fig. 15, as from high to low temperatures. It is obvious that when the welding torch is heated up, higher intensity of SWIR is detected. To be compared with the images under sunlight illumination, acquisition results under illumination are shown at left side while the images without sunlight are at right side of Fig. 15. It is seen from this figure that as the welding torch displays its clear geometry even without sunlight, owing to greatly high intensity of IR radiating.

5.3 Elimination of motion blur with single SDRAM

According to previous image acquisition results, the motionless objects can well be imaged and displayed. With PRE_READ state machine, each row of the images are encoded by FPA output and no defects are observed. However, as objects move quickly, severe motion blurs appear, resulting from the masked WRITE operation of SDRAM. That is because the speed of updating FPA data (writing image data of FPA into SDRAM) is not fast enough to track the motion of objects. To eliminate motion blurs with a single SDRAM, the conflicts between READ and WRITE must be prevented. Since the CCIR656 encoding processes is difficult to be altered, the modification of the FPA output format is carried out. The original idea of our design starts form flexible settings for FPA, including pixel rate, number of pixels in a row and number of rows in a frame, which means the READ and WRITE operations are totally independent. To divide the R/W timings apart, a modification is described as follows.

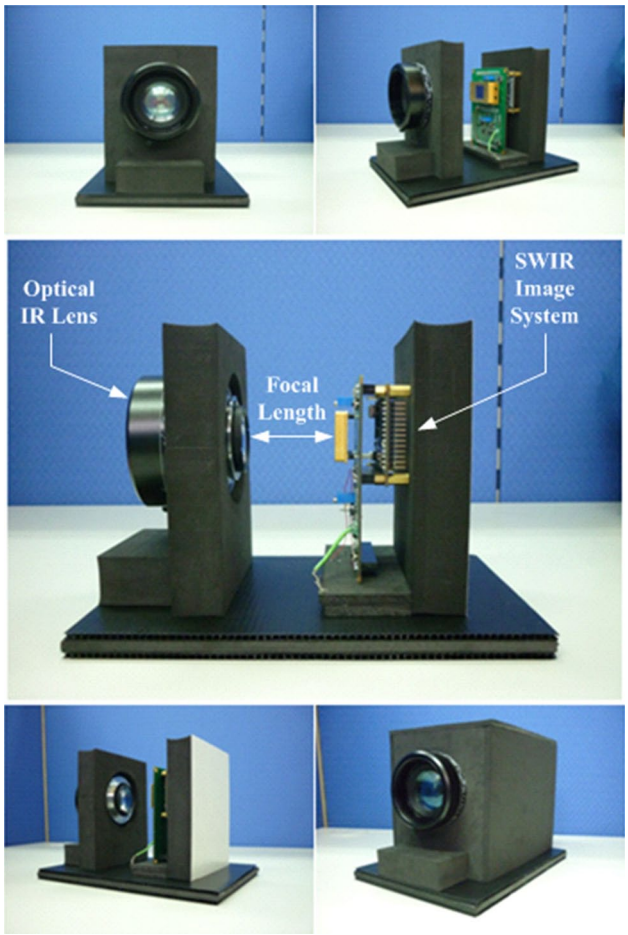

Fig. 12 The proposed SWIR system module and its optical lens

Fig. 13 Acquisition result for face and water

Fig. 14 Image acquisition results under illumination

1. The R/W timings in a row are remained the same setting. The READ operations are executed at the first pixel (earlier part) of a CCIR656 encoded row, and WRITE operations are triggered at the 646th pixel (posterior part) of an FPA data row. The R/W requests sent to SDRAM are generated by this study as original designs.
2. Each FPA row is synchronous with an encoding row. A FPA row is controlled by *LSYNC*, where it is ended by the period and reset by corresponding pixel counter originally. In the modification version, the *LSYNC* is truncated by the READ request (*oSDRAM_read*) from Image_Buffer_OUT.v. Combined with operations (1) as stated above, the R/W timings are divided apart, as illustrated in Fig. 16. Thus the period of *LSYNC* is determined by *oSDRAM_read,* where the number of pixels in a FPA row is settled by pixel rate (the master clock of the FPA). The pixel rate should be at an appropriate value to provide the analog setup enough time for SDRAM WRITE. Besides, it should be lower

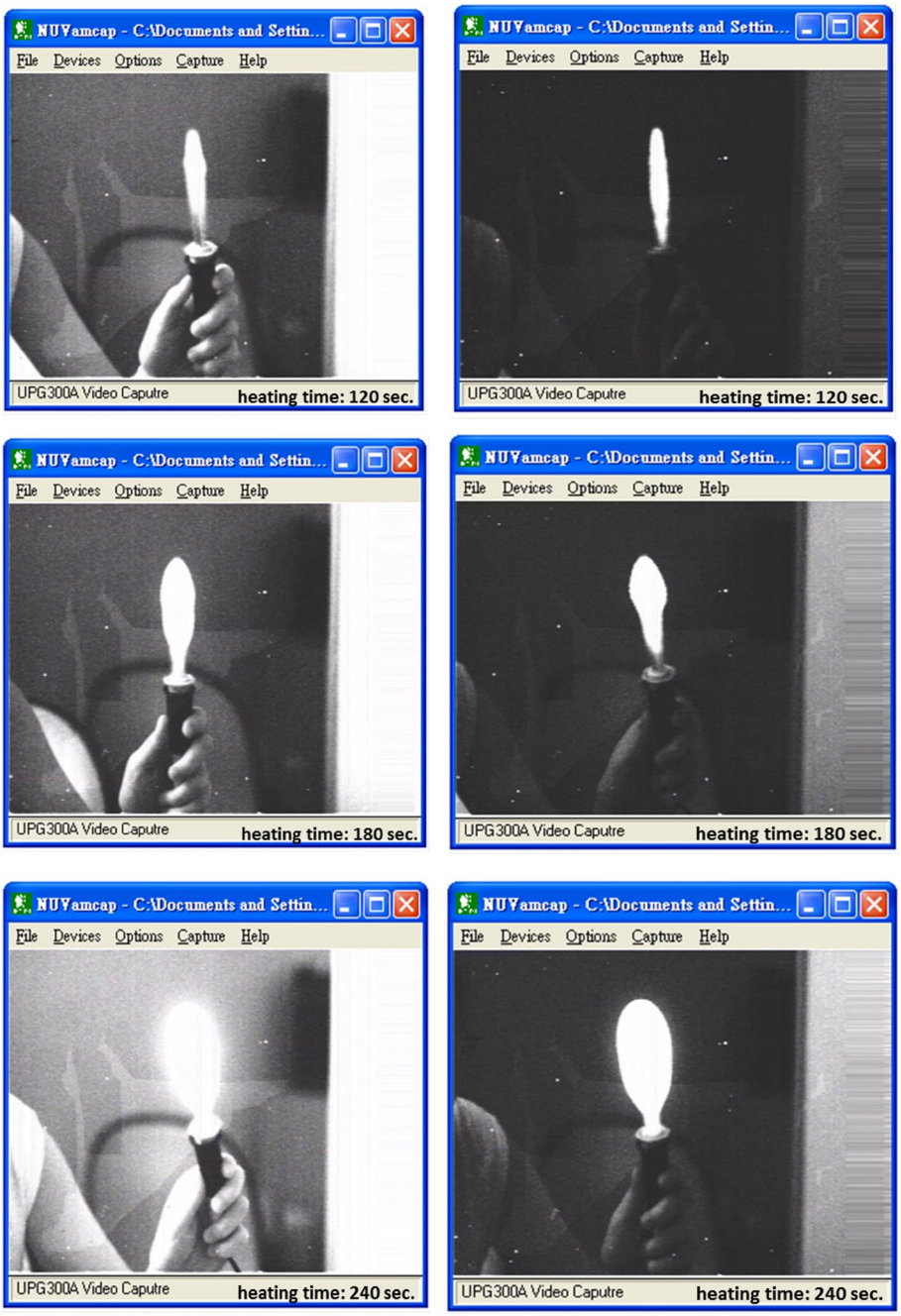

Fig. 15 Acquisition results for welding torch

than 12.6 MHz to ensure the performance of the FPA. The pixel rate is set as 11.25 MHz and corresponding period of *LSYNC* is 715 pixels for final settings.

3. Independency of frames between FPA and CCIR656 format. Although the rows of the FPA and CCIR656 standard share the same period, image frames between them are independent. The number of FPA rows is 521, smaller than that of CCIR656 format, meaning that the frame rate of FPA is slightly faster than NTSC video.

The aforementioned descriptions shows how to divide R/W timings, to realize image encoding application with a single SDRAM by simple modification. The image acquisition results show perfect motion tracking, in which no motion blur is observed. Also, since the conflicts between R/W of SDRAM have been eliminated, the PRE_READ state machine could be removed. The final version of the 640 × 480 SWIR image acquisition system is accomplished with a simpler FSM of SDRAM operations.

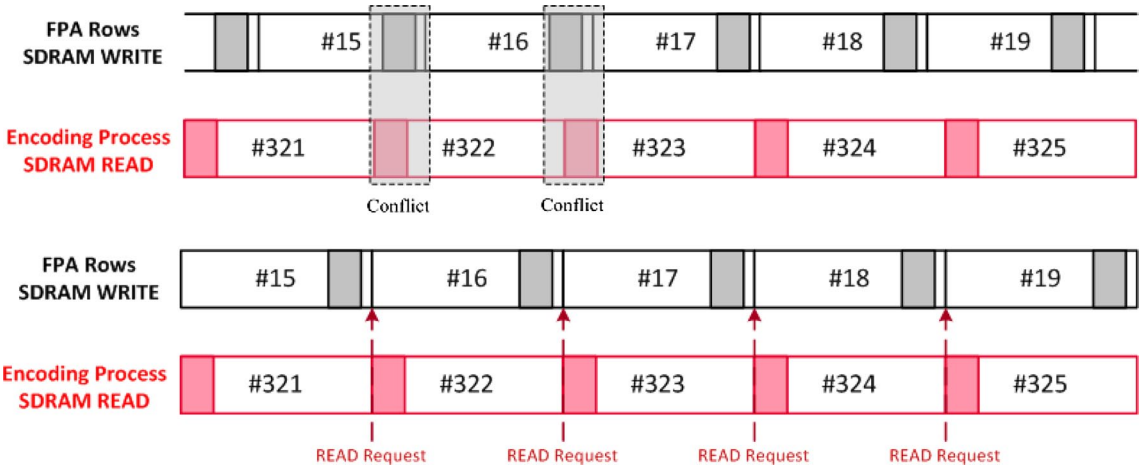

Fig. 16 The relationships between R/W timings of SDRAM operations: (*Up*) Original design–R/W may conflict each other; (*Down*) Modified version–divided apart

Table 2 Specifications of the designed image acquisition system

Spec.	Description
Focal plane array format	640 × 512 pixels
Spectral range	0.9 ~ 1.7 μm
Quantum efficiency	>70 %
Pixel pitch	25 μm
Exposure time	18.5 μs ~ frame time
Analog output format	NTSC, 30 fps
Resolution	8-Bit
Module size	75 × 10 × 2 mm
DC voltage supply	5.2 V
Typical power	1.77 W
Lens mount	F

6 Conclusion

The high resolution (640 × 480) SWIR image acquisition system is proposed and realized in this study. This system features a 640 × 512 array level SWIR (900 ~ 1,700 nm) FPA, 8-bit analog to digital conversion to transform the full range of gray levels, an image encoder for CCIR656 data format to NTSC video transformation, and a 32 Mb SDRAM to coordinate front end data conversion (FPA and ADC) and back-end image data encoding. Based on the FPGA development platform, all of the timing signals for data processes and hardware control are designed in HDL Verilog programming. Having accomplished artificial image data transformation test, an experimental SWIR camera with optical lens is integrated for FPA imaging. In experiments, SWIR images are successfully acquired and displayed in NTSC format, where frame rate is about 29.8. Besides, the primary proposes for SWIR detecting and imaging are presented. The specifications of the designed image acquisition system are listed in Table 2.

Acknowledgments The authors appreciate the support from Ministry of National Defense and National Science Council of R.O.C under the Grant No. NSC 100-2623-E-009-006-D. This work was also supported in part by the UST-UCSD International Center of Excellence in Advanced Bio-Engineering sponsored by the Taiwan National Science Council I-RiCE Program under Grant NSC-101- 2911-I-009-101.

References

Analog Devices, Inc. (2013) ADV7391 data sheet Rev. G
Chen JY (2004) The development and study of DSP-based image acquisition system, National Cheng Kung University
DE0-Nano User Manual, Terasic (2011)
Design debugging using the signaltap II logic analyzer, Altera Corporation (2012)
FPA-640x512 InGaAs imager, near infrared (0.9 ~ 1.7 μm) image sensor, Chunghwa leading photonics tech (2010)
Hang K (2010) Real-time image acquisition and processing system design based on DSP, computer and automation engineering (ICCAE). In: 2010 The 2nd IEEE international conference, vol 4, pp 492–496
Hansen MP, Malchow DS (2008) Overview of SWIR detectors, cameras, and applications. Proc Soc Photo-Optical Instrum Eng (SPIE) 6939:U82–U92
Huang ZH, Li HL (2009) CMOS sensor sequences designing of high-speed image acquisition system based on FPGA, computational intelligence and software engineering, 2009. CiSE 2009. In: IEEE international conference, pp 1–4
Illgner K, Gruber HG, Gelabert P, Liang J, Yoo Y, Rabadi W, Ralluri R (1999) Programmable DSP platform for digital still cameras. In: Proceedings of IEEE international conference on acoustics, speech, signal processing ICASSP'99, vol 4, pp 2235–2238
Integrated Silicon Solution, Inc. (2008) IS42S83200B, IS42S16160B device overview
Lehtoranta O, Hamalainen T, Lappalainen V, Mustonen J (2002) Parallel implementation of video encoder on quad DSP system. Microprocess Microsyst 26:1–15

Li S, Sun D, Yu Y, Csiszar I, Stefanidis A, Goldberg MD (2013) A new short-wave infrared (SWIR) method for quantitative water fraction derivation and evaluation with EOS/MODIS and Landsat/TM data. IEEE Trans Geosci Remote Sens 51(3):1852–1862

Low input voltage, cap free 50-mA low-dropout linear regulators, Texas Instruments (2002)

Lion Photonics, Ltd. (2010) NIR-Lenses spectral range of the lens is 800nm–1400nm datasheet. http://www.qioptiq-shop.com/out/Graphics/de/Pic5/00001660_0.pdf

Peng YK (2012) Non-uniformity and bad pixel correction for NIR image. Mater Thesis, Inst of Electrical and Control Eng, National Chiao Tung University, Taiwan

Ultralow-noise, high PSRR, fast RF 200-mA low-dropout linear regulators in NANOSTARTM wafer chip scale and SOT23, Texas Instruments (2004)

Wang CC, Hsu TH, Ting SF, Cheng HY, Chen CY, Chiang WC, Liu JC, Wuu SG (2013) CMOS image sensor technology development for system-level optimization. In: 2013 international symposium on VLSI technology, systems, and applications, pp 1–2

Wu YF (2011) Edge detection based SWIR image bad pixel detection and correction. Mater Thesis, Inst of Electrical and Control Eng, National Chiao Tung University, Taiwan

Yan B, Sun YF, Ding FF, Yuan HW (2011) Design of CMOS image acquisition system based on FPGA, industrial electronics and applications (ICIEA). In: 2011 6th IEEE conference, pp 1726–1730