InAs-based heterostructure field-effect transistor using $AlAs_{0.16}Sb_{0.84}$ double barriers

Yue-Min Lin, Kun-Ping Lin, Ting-Chi Lee, Meng-Ying Li and Chien-Ping Lee

An InAs-channel heterostructure field-effect transistor on GaAs substrates is presented. The conduction channel was formed by the InAs/$AlAs_{0.16}Sb_{0.84}$/AlSb quantum well. With the addition of the $AlAs_{0.16}Sb_{0.84}$ layer, holes that are generated by impact ionisation at high voltages are effectively confined in the InAs channel because of the large ΔEv in this type-I heterostructure. By suppressing the hole injection into and accumulation in the buffer layer, the feedback through the back gate is eliminated and excellent output characteristics were obtained. The fabricated devices had a threshold voltage of about −0.6 V with a channel mobility of 18 100 cm^2/V-s and a sheet carrier density of 1.2×10^{12} cm^{-2}.

Introduction: In(As,Sb)/(Al,Ga,In)Sb-based heterostructures have attracted much attention owing to their potential applications in high-speed, low-power electronic devices [1] and long-wavelength lasers and detectors. Heterostructure field-effect transistors (FETs) built with the InAs/AlSb material system have been widely studied because of the high electron mobility and easily obtainable high sheet electron densities. However, almost all devices reported in the literature show very poor DC characteristics, with high drain conductance, which increases rapidly with drain voltage [2–4]. Owing to the narrow energy gap, ~0.36 eV for InAs, impact ionisation occurs easily when the drain bias exceeds the energy gap in the channel. Furthermore, because of the staggered band lineup in the InAs/AlSb-based system, where the valence band edge of the AlSb barriers lies above that of the InAs channel [5, 6], the holes generated by impact ionisation are not confined in the InAs channel. Some of them are swept to the negatively biased gate, resulting in a gate leakage current, and others escape into the AlSb buffer layer. The accumulated positive charges in the buffer layer act like a positively biased back gate, giving rise to an increased electron current flow in the channel by the feedback mechanism [2].

One of the most effective ways [2, 4, 7, 8] to solve the problem mentioned above is to add a barrier beside the channel to block the hole injection into the buffer layer. However, to fabricate a type-I heterostructure using InAs as the channel is not trivial. Sb-based compounds, which have a similar lattice constant as InAs, usually have a staggered band alignment with InAs with a negative ΔEv. Replacing the InAs channel with $InAs_{0.8}Sb_{0.2}$, a hole blocking barrier with $\Delta Ev \sim 0.1$ eV can be obtained using AlSb as the barrier [6]. Owing to the small barrier height, Lin *et al.* [4] adopted the idea of using an additional planar n-type-doped layer in the buffer to boost the barrier height and the hole confinement [8]. However, this may potentially cause subthreshold leakage and soft pinch-off problems due to the parallel conduction of this doped layer. Besides, the electron mobility is usually reduced in the $InAs_{0.8}Sb_{0.2}$ channel because of the additional alloy scattering. To increase quantum confinement for holes and at the same time maintain high electron mobility, in this Letter we incorporate an additional confining layer, $AlAs_{0.16}Sb_{0.84}$, between the InAs channel and the AlSb barriers. This layer forms type-I band alignment with the channel layer and very effectively confines the holes in the channel. In this way, we successfully removed the feedback path caused by the holes leaking into the buffer/substrate, thus resulting in much improved DC characteristics and a wider usable drain voltage range. Devices with the InAs channel and InAs/$InAs_{0.8}Sb_{0.2}$ channels have been fabricated. The effect of the additional $AlAs_{0.16}Sb_{0.84}$ barrier layer is clearly seen.

Materials growth and device fabrication: The samples for this Letter were grown by a solid-source molecular beam epitaxy system on (001) semi-insulating GaAs substrates. The layer structure used in this Letter is shown in Fig. 1. First, a GaAs buffer layer of 100 nm was grown at 580°C to obtain a smooth surface. A 1.3 μm relaxed metamorphic AlSb buffer layer grown at 520°C followed to accommodate the lattice mismatch between the channel layer and the GaAs substrate. The active region consisting of $AlAs_{0.16}Sb_{0.84}$ /InAs/$AlAs_{0.16}Sb_{0.84}$ (4 nm/13 nm/4 nm) was then grown on top of the buffer layers. The $AlAs_{0.16}Sb_{0.84}$ layer, which forms a type-I heterojunction with the InAs channel ($\Delta Ev \sim 0.3$ eV) [5], serves as a barrier for the holes generated by the impact ionisation in the channel. A 6 nm-thick AlSb top barrier and a 4 nm-thick highly lattice-mismatched $In_{0.5}Al_{0.5}As$ cap layer were then grown. The $In_{0.5}Al_{0.5}As$ layer keeps the underlying layers from oxidation and forms a good Schottky barrier with the metal gate. All of them were grown at 500°C except the InAs channel, which was grown at 470°C. The growth rate was 0.65 ML/s for the AlSb and $AlAs_{0.16}Sb_{0.84}$ layers. The InAs channel was grown at 0.2 ML/s and the $In_{0.5}Al_{0.5}As$ cap layer was grown at 0.45 ML/s. An InSb-like interfacial layer was inserted at the InAs/$AlAs_{0.16}Sb_{0.84}$ interface to enhance the electron mobility in the channel. The carriers in the channel were provided by a Te delta-doped layer at the upper $AlAs_{0.16}Sb_{0.84}$/AlSb interface. Owing to the large ΔEv in our structure, no additional doped layer was used in the buffer to boost the hole confinement. The band diagram of the InAs/$AlAs_{0.16}Sb_{0.84}$/AlSb quantum well is shown in Fig. 2. Both electrons and holes are confined in the InAs channel. With this added $AlAs_{0.16}Sb_{0.84}$ barrier, a hole confining barrier of $\Delta Ev \sim 0.3$ eV is obtained. We have also prepared FETs with InAs/$InAs_{0.8}Sb_{0.2}$ composite channels with and without the $AlAs_{0.16}Sb_{0.84}$ barriers for comparison. The layer structure and the growth procedure were the same except the channel.

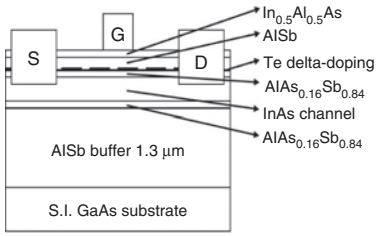

Fig. 1 *Complete structure used in this Letter*

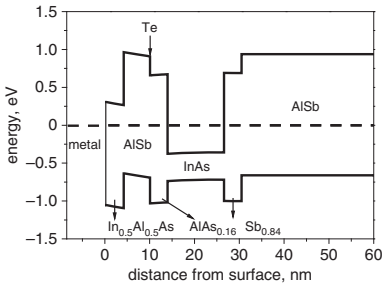

Fig. 2 *Band diagram of InAs/$AlAs_{0.16}Sb_{0.84}$/AlSb quantum well*

The devices were fabricated using a conventional planar process. First, the source and drain ohmic contacts were fabricated. Pd/Ti/Pd/Au was used as the ohmic metal. Then, device mesas were defined by a dry etching process using $Ar/SiCl_4$ for device isolation. The etch stopped at the AlSb buffer layer, which was then covered by a 400 nm-thick Si_3N_4 layer to prevent AlSb from oxidation [9]. The Ti/Au Schottky gates and bonding pads were then defined to complete the process.

Results and discussion: The surface of the grown samples was very smooth. The surface roughness measured by atomic force microscopy had a root mean square of ~0.5 nm. For the FETs with the InAs channels, the contact resistance and sheet resistance, measured by the transmission line method, were typically 0.2 Ω mm and ~300 Ω/sq, respectively. The room temperature electron mobility and the sheet carrier density in the channel, determined by the Hall measurement, were 18 100 cm^2/V-s and 1.2×10^{12} cm^{-2}, respectively. The source/drain series resistances, *Rs*/*Rd*, were estimated to be 0.3 Ω mm in the case of 1 μm source-to-gate spacing. Fig. 3*a* shows the typical room temperature *I–V* characteristics of our devices with a 2 μm-long gate. The device was in depletion mode with a threshold voltage of about −0.6 V. Compared with the devices made with the InAs/AlSb-based system [2–4], our devices had much improved saturation behaviour. Owing to the elimination of the feedback route that brings about the deleterious enhancement of the drain current during impact ionisation, dramatic improvements in the output characteristics were obtained. Fig. 3*b* shows the drain current and transconductance against gate

voltage at drain biases of 0.4 and 0.7 V. A peak transconductance of 340 mS/mm was obtained.

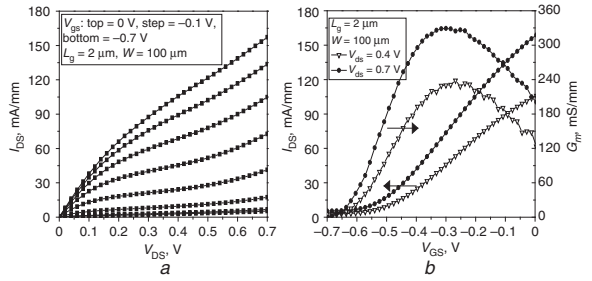

Fig. 3 *Typical room temperature I–V characteristics of our devices with 2-μm long gate (Fig. 3a), and drain current and transconductance against gate voltage at drain biases of 0.4 and 0.7 V (Fig. 3b)*

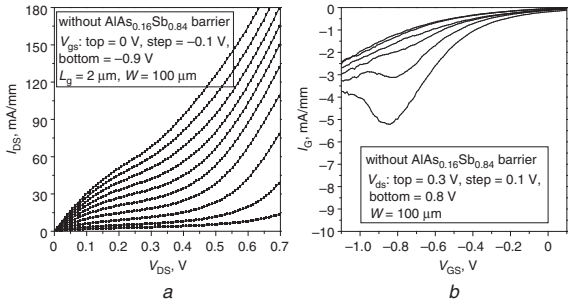

Fig. 4 *I–V characteristics of composite channel device without $AlAs_{0.16}Sb_{0.84}$ double barriers (Fig. 4a), and gate leakage current against gate voltage at different drain voltages for same device (Fig. 4b)*

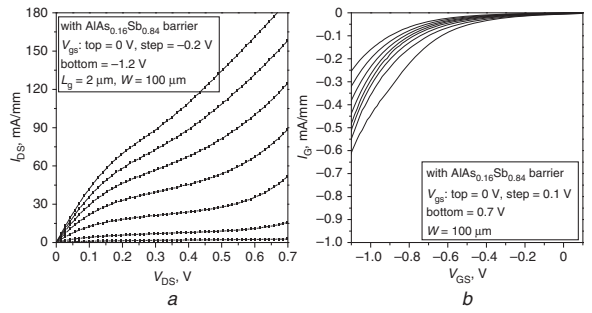

Fig. 5 *I–V characteristics of composite channel device with $AlAs_{0.16}Sb_{0.84}$ double barriers (Fig. 5a), and gate leakage current against gate voltage at different drain voltages for same device (Fig. 5b)*

For devices with a composite ($InAs_{0.8}Sb_{0.2}$/InAs/$InAs_{0.8}Sb_{0.2}$) channel, we have compared the ones with and without the $AlAs_{0.16}Sb_{0.84}$ barriers beside the channels. Figs. 4*a* and *b* are the *I–V* curves and the gate leakage plot for the device without the barriers and Figs. 5*a* and *b* are the ones from the device with the $AlAs_{0.16}Sb_{0.84}$ barriers. Comparing the gate leakage characteristics of Figs. 4*b* and 5*b*, we can clearly see the difference between the two devices. The one without the blocking barriers shows bell-shaped curves. This is a clear indication of hot hole injection into the gate from the channel due to impact ionisation. Moreover, for the device with the $AlAs_{0.16}Sb_{0.84}$ barriers, the gate leakage shows a normal monotonically increasing behaviour and the leakage is much lower. This is a direct result of the hole blocking barrier above the channel. It is also noticed, by comparing Figs. 4*a* and 5*a*, that the output conductance of the device with the barriers is better than that of the device without the barriers. So even for the composite channel devices, the additional barrier at the bottom of the channel provides a better blocking for the holes that may otherwise go into the buffer layer causing a positive feedback for the channel current to raise the output conductance.

Conclusion: To improve the output characteristics of InAs-based FETs and to overcome the poor confinement for holes in the InAs channel, we have adopted an InAs/$AlAs_{0.16}Sb_{0.84}$/AlSb quantum well design for the channel. The type-I quantum well has a hole barrier of $\Delta Ev \sim 0.3$ eV to suppress the hole injection into the buffer layer. With the reduction of the feedback loop, the output *I–V* characteristics and the usable drain voltage range are greatly improved.

Acknowledgments: This work was supported in part by the National Science Council of Taiwan under contract no. NSC99-2221-E-009-079-MY3, in part by the Center for Nano Science and Technology of National Chiao Tung University and in part by the Nano Facility Center of National Chiao Tung University, Hsinchu 30010, Taiwan.

21 February 2014
doi: 10.1049/el.2014.0629

Yue-Min Lin, Ting-Chi Lee, Meng-Ying Li and Chien-Ping Lee (*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan*)

E-mail: ymlin.ee97g@g2.nctu.edu.tw

Kun-Ping Lin (*Department of Electronic Engineering, National Changhua University of Education, Changhua 500, Taiwan*)

References

1 Datta, S.: 'III-V field-effect transistors for low power digital logic applications', *Microelectron. Eng.*, 2007, **84**
2 Brar, B., and Kroemer, H.: 'Influence of impact ionization on the drain conductance in InAs/AlSb quantum well heterostructure field-effect transistors', *Electron Device Lett.*, 1995, **16**, (12)
3 Kanji, Y., Toshiaki, M., and Masataka, I.: 'An InAs channel heterojunction field-effect transistor with high transconductance', *Electron Device Lett.*, 1990, **11**, (11)
4 Lin, H.K., Lin, Y.C., Huang, F.H., Fan, T.W., Chiu, P.C., Chyi, J.I., Ko, C.H., Kuan, T.M., Hsieh, M.K., Lee, W.C., and Wann, C.H.: 'Gate leakage lowering and kink current suppression for antimonide-based field-effect transistors', *Solid-State Electron.*, 2010, **54**
5 Bhargava, S., Blank, H.R., Hall, E., Chin, M.A., Kroemer, H., and Narayanamurti, V.: 'Staggered to straddling band lineups in InAs/Al (As, Sb)', *Appl. Phys. Lett.*, 1999, **74**, (8)
6 Yang, M.J., Bennett, B.R., Fatemi, M., Lin-Chung, P.J., Moore, W.J., and Yang, C.H.: 'Photoluminescence of InAsSb/AlSb single quantum wells: transition from type-II to type-I band alignment', *J. Appl. Phys.*, 2000, **87**, p. 8192
7 Boos, J.B., Yang, M.J., Bennett, B.R., Park, D., Kruppa, W., and Bass, R.: 'Low-voltage, high-speed AlSb/InAsSb HEMTs', *Electron. Lett.*, 1999, **35**, (10)
8 Lin, H.K., Kadow, C., Bae, J.U., Rodwell, M.J.W., Gossard, A.C., Brar, B., Sullivan, G., Nagy, G., and Bergman, J.: 'Design and characteristics of strained InAs/InAlAs composite-channel heterostructure field-effect transistors', *J. Appl. Phys.*, 2005, **97**, p. 024505
9 Shibata, T., Nakata, J., Nanishi, Y., and Fujimoto, M.: 'A Rutherford backscattering spectroscopic study of the aluminium antimonide oxidation process in air', *Jpn. J. Appl. Phys.*, 1994, **33**, pp. 1767–1772