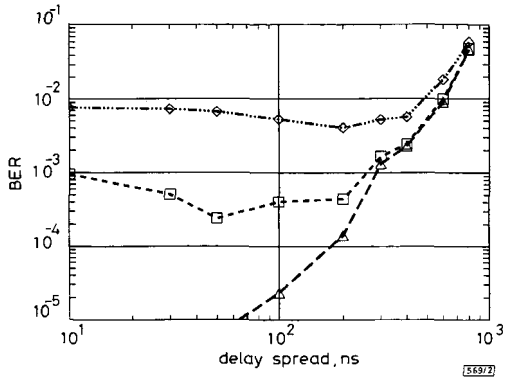

Fig. 2 *BER against delay spread for non-coherent equaliser receiver at different values of E_b/N_o*

◇ E_b/N_o = 20dB
□ E_b/N_o = 30dB
Δ E_b/N_o = 60dB

Performance in fading dispersive channels: Fig. 2 shows a summarised performance indicator for the non-coherent equaliser receiver. A Rayleigh fading two-path channel is used with varying delay spreads and level of E_b/N_o (energy per transmitted bit over noise power). It can be seen that the useful range of operation is extended to delay spreads of ~260ns. This is a significant improvement over a standard DECT receiver (around five times expansion in the useful range of operation at E_b/N_o = 30dB). Simulation results for exponential and Gaussian channels have also shown an acceptable performance over delay spreads of up to 150–200 ns. However the non-coherent structure of the receiver results in some degradation in the performance compared to a coherent equaliser. In fact simulation has shown that a coherent equaliser structure similar to that proposed in [2] (i.e Fig. 1 without the differential detector block) can extend the operating range to more than 600 ns. By analysis and simulations we observed that the performance limits of the basic non-coherent equaliser receiver are mostly due to catastrophic constellation distortion caused by the nonlinearity rather than to equaliser breakdown caused by excessive dispersion.

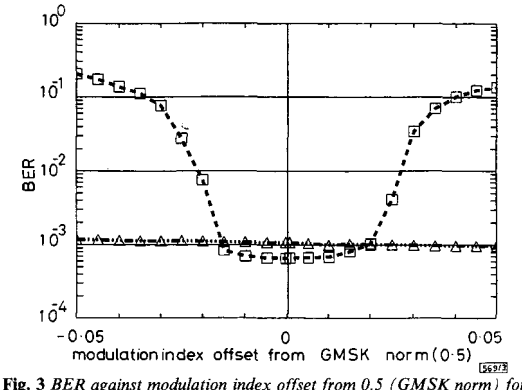

Fig. 3 *BER against modulation index offset from 0.5 (GMSK norm) for coherent and non-coherent equaliser receivers at E_b/N_o = 30dB*

Δ non-coherent equaliser
□ coherent equaliser

Sensitivity to modulation index drifts and frequency offsets: Tests using different modulation indices and local oscillator frequency offsets were also performed for the new receiver as well as the coherent equaliser structure. Fig. 3 compares the performances of the two receivers over the entire range of modulation indices allowed in the DECT specifications (0.45–0.55). It is apparent that the non-coherent receiver stays almost unaffected by the modulation index drifts. On the other hand, the coherent equaliser shows a very sensitive behaviour and breaks down with small offsets from the GMSK norm (much less than the maximum defined in the specifications). Simulations have also shown that the coherent structure can only tolerate frequency offsets of no more than 300 Hz while this range can be expanded by two orders of magnitude (around 30kHz) when the non-coherent equaliser receiver is employed.

Conclusions: We briefly introduced a non-coherent equaliser receiver structure suitable for DECT-type systems. It uses a simple correlative channel estimation procedure. A differential operation is performed prior to equalisation in order to cancel the effect of phase drift. An MLSE process is then performed using a simple two-state Viterbi equaliser.

The simulation results presented suggest that this receiver could be an attractive compromise, achieving a useful extension of dispersive channel operation range (up to 260ns) while remaining largely insensitive to both modulation index drifts and frequency offsets.

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Use of radius weighted mean to cluster two-class data

C.-Y. Yang and J.-C. Lin

Indexing terms: Block codes, Pattern Recognition, Vector quantisation

A new method using the radius weighted mean to cluster two-class data is proposed. Experiments show that the clustering results are good, the computation is fast, and the method is easy to implement. The method can be applied to block truncation coding, codebook generation, and decision tree construction.

Introduction: Data clustering plays an important role in pattern recognition and many other fields, such as image processing, vector quantisation (VQ), and artificial intelligence. In particular, many practical applications are related to two-class clustering problems [1]; examples include BTC for image compression, divisive clustering for hierarchical clustering, and binary decision tree construction. In this Letter we attempt to develop a new method for clustering two-class data. To achieve this goal, we employ the idea of the radius weighted mean, a special kind of point originally introduced to register shapes [2, 3]. More specifically, we will use the radius weighted mean of the given data to create a decision boundary to cluster the given data.

Clustering method: Without loss of generality, we illustrate our ideas using two-dimensional data. Let $S = \{(x_i, y_i) \mid i = 1, 2, ..., n\}$ be the given data set to be partitioned, and let the centroid of S be denoted by $(\bar{x}, \bar{y})$ with $\bar{x} = (\Sigma_{i=1}^{n} x_i)/n$ and $\bar{y} = (\Sigma_{i=1}^{n} y_i)/n$. The

radius weighted mean (x', y') of S is defined by $x' = (\Sigma_{i=1}^{n} r_i x_i)/R$ and $y' = (\Sigma_{i=1}^{n} r_i x_i)/R$ with R defined by

$$R = \sum_{i=1}^{n} r_i = \sum_{i=1}^{n} [(x_i - \bar{x})^2 + (y_i - \bar{y})^2]^{1/2}$$

Note that r_i is the distance between the centroid $(\bar{x}, \bar{y})$ and the point (x_i, y_i). The proposed decision boundary that splits the given set S into two clusters is then taken to be the straight line passing through the radius weighted mean (x', y') and perpendicular to the principal axis [4] of S.

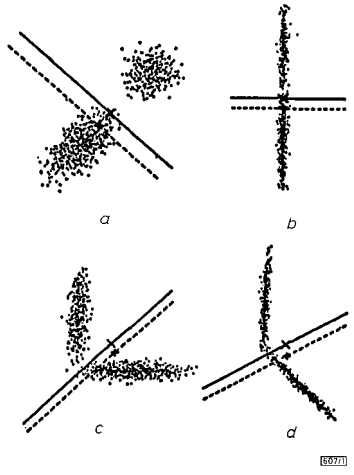

Fig. 1 *Some clustering results*

Experimental results: Four examples are given in Fig. 1 to illustrate the performance of the proposed method. There are 2 100 points in each example. The proposed decision boundary, which passes through the radius weighted mean (represented by '×') and is perpendicular to the principal axis, is indicated by a solid line. For comparison, we also sketch in each example a dashed line representing another apparently plausible decision boundary, the line passing through the centroid (represented by '+') and perpendicular to the principal axis. It can be seen that passing through the radius weighted mean usually produces a more valid clustering result than passing through the centroid. Fig. 2 illustrates the robustness of the proposed method to noise. 200 noise points appear in the Figure, but the detected decision boundary is still good (a similar result holds for the dashed line running through the centroid). Another interesting fact is that very little time is needed for clustering using the proposed method. Experiments showed that it takes only ~0.10s to cluster a set of 2100 points when an IBM PC with an 80486 processor is used.

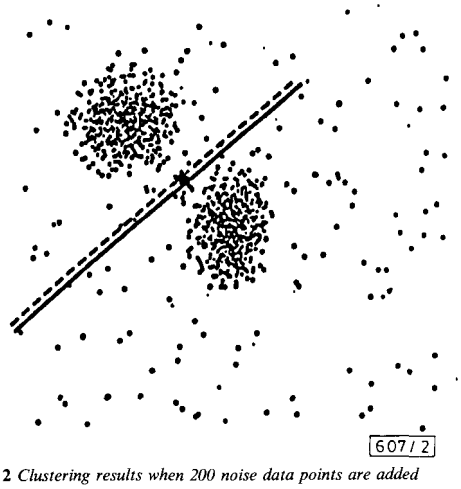

Fig. 2 *Clustering results when 200 noise data points are added*

Results of BTC image coding using the one-dimensional version of the proposed method are illustrated in Fig. 3. The original images are 512 × 512pixels with 8bit grey level resolution. The monochrome images are partitioned into a series of nonoverlapping blocks of 4 × 4pixels. The resulting bit rate is 2bit/pixel, and the compression ratio is 4:1. Table 1 shows that the mean-square errors (MSE) for three typical input images using the proposed method are smaller than that for the modified BTC [6] when both methods use 2bit/pixel. Note that the decision boundary used in the modified BTC [6] is through the centroid instead of the radius weighted mean.

Table 1: Comparison of proposed method and modified BTC [6]

Image	MSE Proposed method	MSE Modified BTC [6]
Lena	23.65	26.80
Jet	29.97	35.29
Pepper	22.26	25.55

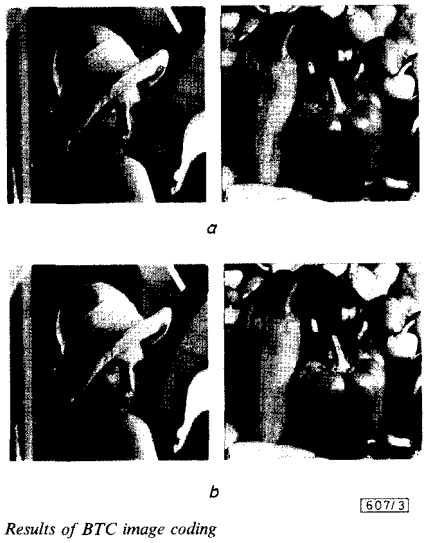

Fig. 3 *Results of BTC image coding*

a Original images
b Coded images using proposed method (2bit/pixel)

Comparison with median-cut method: Heckbert [5] proposed a two-class clustering method, called the median-cut method, to quantise colour images. He projected all data onto the co-ordinate axis with the largest variance. This method is not good in the sense that the decision boundary is always perpendicular to one of the co-ordinate axes, and thus might be improper for data sets in which the distribution of every co-ordinate has a unique peak (making the set non-separable). Even if the projections are made on the principal axis instead of on a co-ordinate axis, the median-cut method is still not competitive with our method, as illustrated in Fig. 4. The bold dotted line in that Figure runs through the middle point of the n projected points lying on the principal axis. Obviously, this decision boundary is poorer than ours (the solid line).

Conclusions: In this Letter, we have combined the idea of the radius weighted mean with that of clustering to obtain a new method of clustering two-class data. Experimental results show that the proposed method is better than either the median-cut method or the method using the line passing through the centroid and perpendicular to the principal axis. The proposed method is time-saving, noise-insensitive, deterministic, and uses no initial values. It can thus be easily applied in BTC, automatic decision supporting system, the hierarchical divisive design of a VQ codebook, and so on.

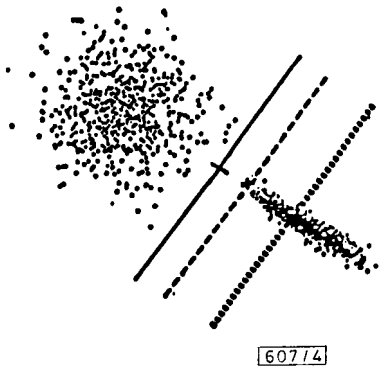

Fig. 4 *Comparison with median-cut method*

The bold dotted line passing through the middle point of the principal axis is not a good decision boundary

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300ps 4K read-only memory implemented with AlGaAs/GaAs HBT technology

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Indexing terms: Heterojunction bipolar transistors, Read-only storage

A low-power mask-programmable 4 Kbit read-only memory with 300ps access time is reported. The circuit is implemented in AlGaAs/GaAs HBT technology based on 1.4μm emitter width. Power dissipation for the circuit is less than 1.2W, which has been minimised through the use of capacitively-coupled active pull-down circuitry.

Introduction: Read-only memories (ROMs) are extensively used to implement finite-state machines, to store micro-code control programs, and to implement direct-map look-up tables. Particularly for look-up tables, it is desirable to have ROMs with ultrafast access time. For example, in direct digital frequency synthesis (DDS), sinusoidal signals of precisely tuned frequencies are generated by means of a digital phase accumulator feeding a sine function look-up table used in conjunction with an output digital-to-analogue convertor [1]. In high performance DDS systems, the ROM is often the speed-limiting element, because it has to support clock rates of the order of two-and-half times the synthesised frequency. We report an ultrahigh speed ROM that can generate outputs at a data rate of 3Gbyte/s, faster by a factor of 3 than the fastest previously reported for a ROM of similar capacity [2]. The circuit employs AlGaAs/GaAs HBT technology, featuring emitter-up *npn* transistors with cutoff frequency f_t and maximum frequency of operation f_{max} in the 55GHz range [3]. Despite the large number of transistors in the circuit (more than 5000), a respectable yield of the order of 50% was obtained with this technology. To minimise power without too great a sacrifice of speed, low static power active pull-down circuitry was used.

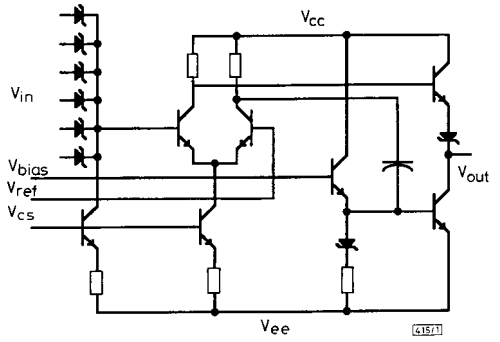

Fig. 1 *Circuit schematic diagram of row decoder and row driver circuit*

Circuit design: The ROM is organised as a 512 × 8 bit memory block. The circuit approach is based primarily on current-mode logic (CML), modified as appropriate in different subcircuit configurations to achieve high speed and low power. The memory elements are arranged as a 64 row by 64 column array, with each block of 8 columns holding 8 bit words. Six *X*-inputs together with three *Y*-inputs select the addressed word. These single-ended inputs are buffered by differential push-pull drivers, and Schottky diode decoders are employed to address the selected row and columns, as illustrated in Fig. 1. Schottky diodes can easily be implemented in HBT technology, with active dimensions down to 1.4 × 2.0 μm², and input capacitances below 5 fF. The row drivers, also shown in Fig. 1, use emitter-follower output stages in conjunction with capacitively-coupled active pull-down circuitry to rapidly charge and discharge row-line capacitances. The drivers consume low static power, but can deliver high dynamic drive during switching. Fig. 2 illustrates the active currents during high-speed transients. From the simulated plot, it can be seen that the driver can source or sink over 4mA of current during switching, while drawing less than 0.5mA in the standby state. Internal voltage swings are designed to be 0.5V. The three *Y*-address inputs are similarly decoded through similar circuitry. Simulation showed that the active pull-down circuitry maintained stable bias currents over a wide range of temperature (25–125°C) and supply voltage (±10%). The memory cells consist of one transistor per cell, with collector grounded. Programming is carried out through a VIA connecting the emitter metal to the output bit line. The sense amplifiers are implemented using parallel HBT OR gates, and the outputs drive emitter-follower output buffers directly. Table 1 shows the simulated delay contributions to read access times for both *X* and *Y* address changes.

Table 1: Simulated contributions of various subcircuits to the read access time for row and column address changes

Row-select timing characteristics	
Circuit	Delay
	ps
Input buffer + row decoder	50
Row driver	140
Sense amp + output buffer	100
Total address access time	290
Column-select timing characteristics	
Circuit	Delay
	ps
Input buffer + bit decoder	40
Column driver	110
Sense amp + output buffer	140
Total address access time	290