#### Published in IET Nanobiotechnology Received on 11th December 2012 Revised on 10th July 2013 Accepted on 16th July 2013 doi: 10.1049/iet-nbt.2012.0043

# www.ietdl.org



#### ISSN 1751-8741

# Field-programmable lab-on-a-chip based on microelectrode dot array architecture

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Abstract: The fundamentals of electrowetting-on-dielectric (EWOD) digital microfluidics are very strong: advantageous capability in the manipulation of fluids, small test volumes, precise dynamic control and detection, and microscale systems. These advantages are very important for future biochip developments, but the development of EWOD microfluidics has been hindered by the absence of: integrated detector technology, standard commercial components, on-chip sample preparation, standard manufacturing technology and end-to-end system integration. A field-programmable lab-on-a-chip (FPLOC) system based on microelectrode dot array (MEDA) architecture is presented in this research. The MEDA architecture proposes a standard EWOD microfluidic component called 'microelectrode cell', which can be dynamically configured into microfluidic components to perform microfluidic operations of the biochip. A proof-of-concept prototype FPLOC, containing a  $30 \times 30$  MEDA, was developed by using generic integrated circuits computer aided design tools, and it was manufactured with standard low-voltage complementary metal-oxide-semiconductor technology, which allows smooth on-chip integration of microfluidics and microelectrode cells, the FPLOC has achieved large-scale integration of microfluidics and microelectronics. By integrating 900 droplet detection circuits into microelectrode cells, the FPLOC has achieved large-scale integration of microfluidics and microelectronics. Compared to the full-custom and bottom-up design methods, the FPLOC provides hierarchical top-down design approach, field-programmability and dynamic manipulations of droplets for advanced microfluidic operations.

#### 1 Introduction

Electrowetting-on-dielectric (EWOD) refers to physics describing the electric forces caused by an electric field on the interface between a droplet and an electrode separated by a dielectric layer. By applying the electric field to only one side of the droplet, an imbalance of the EWOD actuation force on the droplet is formed. If this actuation force gradient is strong enough, it causes the droplet to move. In the literature, various physical descriptions of how a droplet translates by an asymmetric EWOD actuation have been discussed: based on unbalanced electrostatic forces, surface tension forces or hydrostatic pressures [1]. EWOD is a versatile tool in microfluidics because it enables control over fluid shape and flow by electrical signals alone [2, 3]. For their simplicity and reconfigurability, EWOD microfluidic biochips have been implemented in a wide range of lab-on-a-chip (LOC) applications [4-6]. EWOD microfluidics gains high attention because of its highly flexible and reconfigurable nature, and its capability to perform all the fundamental microfluidic operations on-chip using an array of electrodes. The increasing interest of EWOD microfluidics is clearly reflected in the growing number of publications [7]. Early work in EWOD microfluidics has demonstrated promising results in transforming the biochip industry, but further developments are surely required [4, 8]. The development of EWOD microfluidics has been hindered by the absence of: integrated detector technology, standard commercial components, on-chip sample preparation, standard manufacturing technology and end-to-end system integration [4, 7, 9, 10].

Integration of microelectronics and microfluidics through the complementary metal-oxide-semiconductor (CMOS) technology provides one of the best ways to integrate advanced detection technologies into EWOD microfluidic systems [11, 12]. To move beyond the limit of current high-voltage-only EWOD microfluidic fabrication technologies, this paper demonstrates the feasibility of the first EWOD microfluidic chip fabricated by the standard TSMC  $0.35 \mu$  3.3 V CMOS technology. The goal is to position the well-established and commonly available low-voltage CMOS technology as a good candidate for the mass production of future fully integrated EWOD microfluidic biochips. In addition, the field-programmable LOC (FPLOC) prototype demonstrates the integration of detection circuit on the chip. Totally, there are 900

CMOS-based capacitive detectors integrated into the FPLOC. Therefore it is also a demonstration of a large-scale integration of microelectronics and microfluidics.

Traditionally, developments of EWOD microfluidic devices have been taking a bottom up approach that discrete microfluidic components are designed and integrated together to perform a particular microfluidic application. Therefore current EWOD microfluidic devices are typically developed by custom approaches instead of standard fabrication components and processes. The design complexity of future EWOD microfluidic devices will increase dramatically because of more concurrent bioassays, higher system integration and more sophisticated system control. For example, a programmable large area digital microfluidic array has been successfully demonstrated [13, 14]. In addition, droplet routing for EWOD devices has been generating a lot of interest recently because it is very complex and has direct impacts on the biochip performance [15–17]. Current approaches in designing and fabricating EWOD microfluidic devices cannot scale well for these challenges. To improve the design efficiency of traditional bottom up design methods, top-down design methods have been proposed [9, 18-21]. It is an anticipated goal to leverage the architectural designs to cover as many applications as possible. The concept is that the wide varieties of biomedical applications need to be mapped into a set of microfluidic operations to manage the design complexity. Consequently, this set of microfluidic operations are then performed by dedicated microfluidic components [9]. Hierarchical top-down design methods so far are still based on a set of microfluidic components which are varied greatly in sizes or shapes. The lack of standard EWOD building elements hinders the development of the top-down design methods. Microelectrode dot array (MEDA) architecture adds one layer to the hierarchical structure to convert EWOD microfluidic components into standard EWOD building elements [22, 23]. Unlike other digital microfluidic systems, which use fix-patterned and fix-sized electrodes to perform predefined bioassays, the MEDA architecture is based on the concept that bioassay functions can be implemented by dynamic configurations of a sea-of-microelectrode array. In this configuration, an array of identical building elements called 'microelectrode cells' are dynamically configured and activated to define microfluidic components, operations and applications of the biochip. The electrode configured from microelectrodes is called 'configured microelectrode array', or CMA, to distinguish it from a conventional (solid) electrode. Fig. 1 shows the basic concept of the MEDA architecture that a LOC could be built through the configuration of microelectrodes into CMAs. Fig. 1*c* illustrates an example of a reservoir CMA and associated square CMAs configured from square microelectrodes.

The idea of the FPLOC came from the field-programmable gate array (FPGA). The FPGA is an electrical programmable logic device that has the ability to configure the logic function by a designer after the fabrication process, therefore 'field-programmable'. From the function point of view, FPGAs work much like application-specific integrated circuits (ASICs) and can be programmed to implement all ASIC logical functions. FPGAs have become one of the key digital circuit implementation tools based on their flexible field-programmability, fast turnaround time and low non-recurring engineering costs [24, 25]. FPLOC works similarly as FPGA. Pre-manufactured FPLOCs can be configured and programmed into biochips with different applications. For example, before any programming or configuration, a blank FPLOC looks like what shown in Fig. 1a. It has an array of unrelated microelectrodes. The first design step for the FPLOC is to do the configuration of physical locations, sizes and shapes of all microfluidic components such as reservoirs, mixing areas, detection areas and transportation paths and the overall layout of the FPLOC. Fig. 1b illustrates a blank FPLOC has been programmed into a LOC design. Then, the second step is to program the desired microfluidic operations. In this way, an FPLOC is converted into a functioning biochip.

The remainder of this paper is organised as follows. In Section 2, system block diagram of the FPLOC is presented. Designs of key function blocks are then discussed in the subsequent sections. The droplet actuation driver is discussed in Section 3, and droplet detection is covered in Section 4. Section 5 covers the design of chip and microelectrode layout including chip packaging. The chip layout map is discussed in Section 6, and the microfluidic operation manager is covered in Section 7. Section 8 shows FPLOC chip characterisation. Then, the concluding remark is given in Section 9.

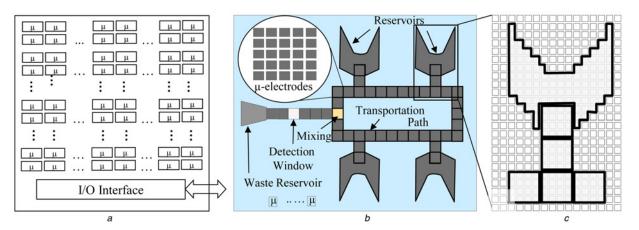


Fig. 1 FPLOC based on the MEDA architecture can be configured into a biochip

a Blank FPLOC before programming

b Example of the configured FPLOC

c Illustration of an enlarged portion of the configured FPLOC [23]

# 2 FPLOC system block diagram based on MEDA architecture

The FPLOC is based on the MEDA architecture and its system block diagram is illustrated in Fig. 2. The FPLOC chip includes 900 microelectrode cells and an interface circuit, which provides the connection to the system control block. A PC and a NI PCIe-6537 interface card were used to form the hardware for the system control block. Microelectrode cells are daisy-chained together to simplify the wiring and to maximise the scalability. The activation of individual microelectrodes is controlled by serially shifting control data into the one-bit control register of each microelectrode cell. Using this highly scalable daisy-chained control structure, the FPLOC can achieve 100% individual controllability of each microelectrode with a minimum number of control pads, which could be only three, that is, IN, CLK (clock) and OUT. Also, the same

scan-chain is used to read out the one-bit droplet detection result of each microelectrode. All logic values of droplet detection are first clocked into the daisy-chained registers and then serially shifted out. The designs of main functional blocks of the FPLOC are discussed in the subsequent sections.

#### 3 Droplet actuation driver

Conventionally, the EWOD microfluidic system requires high-voltage electrodes to perform the droplet actuation. Typically, the top plate is used as the electric potential reference (ground), and the high-voltage potentials are applied to electrodes on the bottom plate to perform EWOD actuations. The polarity of the droplet actuation voltage is not a concern in actuating droplets. By moving high-voltage potentials to the top plate and implementing the bi-state-switch drivers in the microelectrode on the bottom

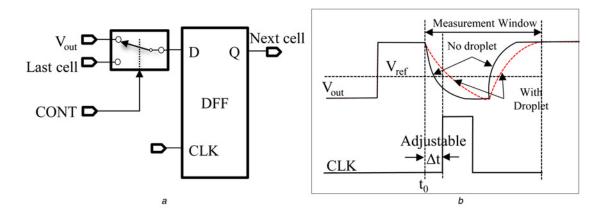


Fig. 2 Block diagram of FPLOC based on MEDA architecture and CMOS fabrication technologies

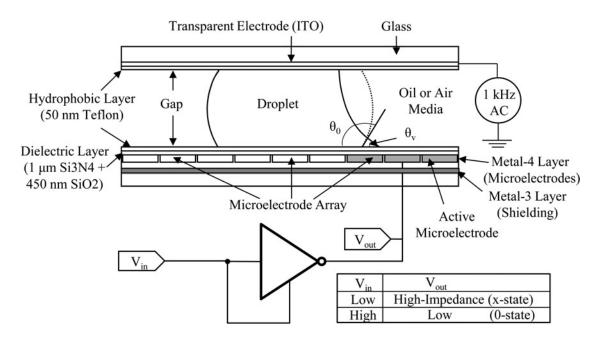


Fig. 3 Bi-state-switch driver allows the EWOD droplet actuation by the low-voltage CMOS fabrication technology

plate, the low-voltage CMOS fabrication technology can be used for EWOD actuations. Fig. 3 illustrates the bi-state-switch driver. In this design, the high voltage is applied to the top plate, and the microelectrode is activated when it is grounded (0-state). The high-impedance mode (x-state) deactivates the microelectrode. In this arrangement, when the bottom microelectrode is activated (ground), the electric field still accumulates electric charges at the interface between the droplet and the insulating dielectric layer, causing the EWOD effect to transport the droplet. Although the polarity change of the actuation voltage might cause some degree of changes of the accumulation of electric charges at the droplet/insulator interface [26], the overall droplet actuations can be still reliably performed.

#### 4 Droplet detection

The design of the one-bit droplet detection is illustrated in Fig. 4a. Sensing control signal CONT switches the input of D flip-flop (DFF) from the output of the last scan cell to Vout which is its own physical microelectrode and forms a droplet detection test loop. As shown in Fig. 4b, the microelectrode is charged to 3.3 V first and at  $t_0$  it is discharged for the measurement of discharging speed. After a pre-calculated time from  $t_0$ ,  $V_{out}$  is charged again for the measurement of charging speed. The RC time constant of the microelectrode determines discharging/charging speeds. To detect the droplet, the CLK signal clocks the DFF as the logic latched comparator at the pre-calculated delay  $\Delta t$  from  $t_0$ . At the moment the CLK triggering edge comes in, if  $V_{\rm out}$  is falling below  $V_{\rm ref.}$  then the logic value 'zero' is latched onto the DFF, as indicated by the solid discharging curve. In this case, the droplet detection senses a time constant less than  $\Delta t$ , so no droplet is present. When the droplet is present, as shown by the dashed discharging curve, the detector latches a 'one' at the rising edge of the CLK. Both discharging and charging curves can be used to detect the droplet by adjusting  $\Delta t$ . After the droplet detection is performed, the CONT signal is disabled and the scan chain is restored to shift out the 900-bit droplet detection results.

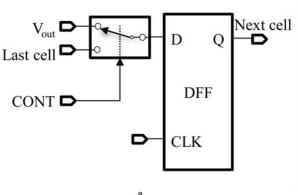
In addition to the functional importance of the droplet detection, the implementation of the circuit is also a demonstration of integration of microfluidics and microelectronics. Since the droplet detection is included in the microelectrode cell, the microelectronic circuit becomes a part of the microfluidic component. This represents true on-chip integration. In addition, a total of 900 CMOS-based capacitive detectors are built into the FPLOC, which demonstrates large-scale integration than integration of a single but more complex detector.

#### 5 Design of chip and microelectrode layout

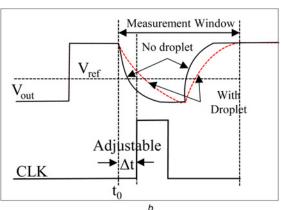
Fig. 5*a* shows the chip layout of the FPLOC. A  $30 \times 30$  microelectrode array is implemented to form a working area of of  $1.142 \,\mu\text{m} \times 1.142 \,\mu\text{m}$ . Each microelectrode is  $37.1 \,\mu\text{m} \times 37.1 \,\mu\text{m}$  with  $1 \,\mu\text{m}$  spacing between microelectrodes. The square microelectrode with wall-brick layout was chosen as the balance of design complexity and actuation capability. Also, the metal 4 layer was used for the physical microelectrode, and the metal 3 layer was used as the shielding layer (Fig. 3).

The passivation layer from standard CMOS fabrication process is used as the dielectric layer. The passivation layer consists of a 1  $\mu$ m Si<sub>3</sub>N<sub>4</sub> layer and a 450 nm SiO<sub>2</sub>. A 55 nm hydrophobic layer was then spin coated (1 wt% Teflon AF1600, 30 s at 3000 RPM and 150°C bake for 30 min) on top of the dielectric layer, and an identical hydrophobic layer was also applied to the ITO glass (top plate). The hydrophobic layer was spin-coated to the biochip after wire bonding and packaging of the chip. A chip carrier, which has an IC socket to house the chip on one side and a smooth surface to connect to the spinner on the other side, was created for spin-coating the chip. Also, extra surface space of the chip was reserved between the microelectrode array and the chip IO ring (including bonding wires) as shown in (b) to prevent obstacles for the spin-coating.

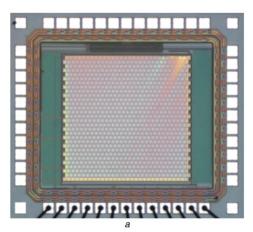
The 48-pin ceramic dual in-line package (CerDIP) is chosen as the package of the FPLOC. The CerDIP is a rectangular ceramic package that has dual in-line leads on its longer sides. The package has a wide selection of available cavity sizes to accommodate the needs of different die sizes. The sealing glass of the 48-pin CerDIP is replaced by the special top plate, which also provides the bridging function for delivering the droplet onto the FPLOC. The die attachment is manually adjusted to have a 20  $\mu$ m gap between the die surface (the bottom plate) and the cavity window frame. Therefore the gap is 20  $\mu$ m when the top plate was pressed against the cavity window frame.



**Fig. 4** Diagrams of the one-bit droplet detection circuit *a* Schematic of the time constant capacitive detector *b* Timing diagram



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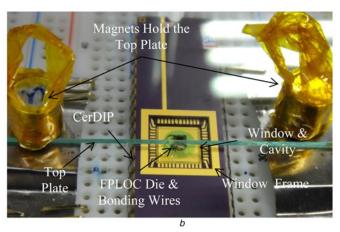


Fig. 5Microelectrode cells of FPLOC

*a* Wall-brick layout of the microelectrode array *b* FPLOC in the 48-pin CerDIP and the top plate supporting structure

Other gap sizes are achieved by adding spacers and adjusting the top plate supporting structure.

Peak heights of bonding wires are about 200  $\mu$ m above the die, and bonding wires would touch the top plate if the gap height is < 200  $\mu$ m. Therefore all bonding wires are limited to one side of the die in order to free up the other three sides for the top plate. Fig. 5*b* shows a picture of the FPLOC in the 48-pin CerDIP package as well as the glass top plate and its supporting structure.

#### 6 Chip layout map

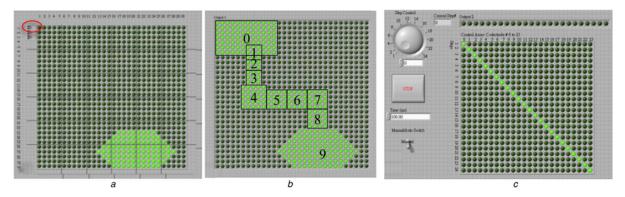
The chip layout map stores configuration data of the layout of the chip and the designs of microfluidic components. The FPLOC has a hierarchical architecture. At the top level, applications are scaled to a micro fluidic platform. The second level describes the microfluidic operations, and the third level describes the components to perform the operations. Then at the bottom level components are mapped to microelectrodes. The identical microelectrode cells work as the building elements and hierarchically form the foundation of building the entire FPLOC. The chip layout map (Fig. 2) is implemented as the graphical configuration tool for the third (microfluidic component) layer.

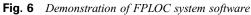
National Instrument's Graphical programming language LabVIEW is leveraged to implement the chip layout map

function. At the microfluidic component layer, all necessary microfluidic components for microfluidic operations are defined and geometry-level graphical interface is used to create physical representations of the microfluidic components and the final chip layout of the FPLOC. Fig. 6 illustrates an example of using Chip Layout Map to configure microfluidic components. Fig. 6a shows a physical configuration of #9 CMA. Each CMA configuration has a page  $(30 \times 30)$  of blank microelectrodes (shown as dark green) to work on. Through the graphical interface, CMA configuration is a matter of pointing and selecting. CMA #9 is configured into a hexagon shape as an example. Although doing the configuration of individual CMA, a real-time summary page shows all CMA configurations and the overall layout of the chip as depicted in Fig. 6b. In this summary figure, 10 CMAs, numbered from 0 to 9, form an electrode path from CMA #0 to CMA #9. CMA #0 and CMA #1 also demonstrate that overlapped CMAs are allowed in the FPLOC configuration.

#### 7 Microfluidic Operation Manager

The Microfluidic Operation Manager handles the sequences and actuation timing for the droplet manipulations. Hierarchically, it is the second level which describes the microfluidic operations. The programming of the control





a Configuration of CMA #9 under the chip layout map

*b* Summary page of the chip layout map (numbers and boarder lines are added for explanations) *c* Microfluidic Operation Manager

window is in two simple steps: (i) defining CMAs that would be activated in each step and (ii) assigning appropriate actuation timing between steps. The control window shown in Fig. 6c demonstrates the droplet actuations by sequencing from steps 1 to 23 which defines the droplet actuation from CMA #0 to CMA #23 with 100 ms between steps. The control widow can be operated in manual mode or auto mode with predefined timing between steps. After programming of microfluidic operations is done, it can be tested and saved for later use. A batch file containing a sequence of predefined microfluidic operations can achieve rather complex FPLOC programming and microfluidic operations.

#### 8 FPLOC chip characterisation

This section covers the validations and analyses of the FPLOC. There are two main validations for the FPLOC: (i) droplet actuation validations and (ii) droplet detection validations.

#### 8.1 FPLOC droplet actuation

DI-water in silicon oil with 300-20 µm gaps (Fig. 3) were tested for the actuations of droplets of FPLOC. Droplets could be actuated through the control by the microfluidic operation manager to move around the chip. The droplet actuation has been successfully achieved by the bi-state-switch driver with the help of the electrode-column actuation, and Figs. 7a and b show the pictures of the movement by activating CMAs. droplet The electrode-column actuation is an advanced microfluidic operation of the MEDA architecture. It actuates the droplet one column at a time to maximise the effective length of the contact line through the actuation. This actuation technique provides smooth and steady droplet actuation especially for marginal driving capability situations [23]. The original contact angel was 107° and the actuated

contact angel was  $87^{\circ}$ . The attempt of three-electrodecutting was not successful because of the limited actuation forces. The only cutting (as well as droplet creating) operation successfully performed was an electrode-column cutting of a droplet, which was pinned at two sticky spots, as shown in Figs. 7c-e. Overall, experimental results of the FPLOC droplet actuation are in line with the expectations that leakage currents of the bi-state-switch driver would reduce the droplet actuation capability. In addition, hierarchical programming of the FPLOC has been very successful. Configurations of CMAs by the chip layout map and microfluidic operations by the microfluidic operation manager were seamlessly executed.

In the test, the high-voltage was applied to the top plate and the bi-state-switch drivers were grounded (0-state) to activate CMA. The high-impedance mode (x-state) of the bi-state-switch driver deactivated the CMA. In the ideal situation, the high impedance mode should result a zero potential between the high-voltage top plate and the deactivated CMAs. In reality, leakage currents did exist and the induced voltage on deactivated microelectrode was not able to follow the applied potential on the top plate. Measurements of the induced voltages were performed in FPLOC droplet actuation test. The results are shown in Fig. 8*a* where the applied potential is  $V_{\text{DDH}}$  and the induced potential on the microelectrode is  $V_{ind}$ . For low potentials (< 10.3 V), the relation between the induced voltage  $V_{\text{ind}}$ and the applied potentials  $V_{\rm DDH}$  on the top plate shows a linear dependence. When the applied voltage is greater than 10.3 V, the induced voltage is not increasing as fast as the applied voltage. The induced voltage  $V_{ind}$  has a saturation asymptote at 14.5 V.

Fig. 8b shows the schematic of the bi-state-switch driver which consists of an inverter and five transistors.  $V_{DDH}$  is the applied voltage on the top plate. When  $V_{in}$  transits from high to low it turns off  $M_{N1}$ ,  $M_{N2}$  and the path NMOS gate  $M_{NPG}$ . This puts the bi-state-switch driver into x-state (high-impedance mode). In x-state,  $V_{ind}$  is expected to be induced to high voltage  $V_{DDH}$ . However, subthreshold

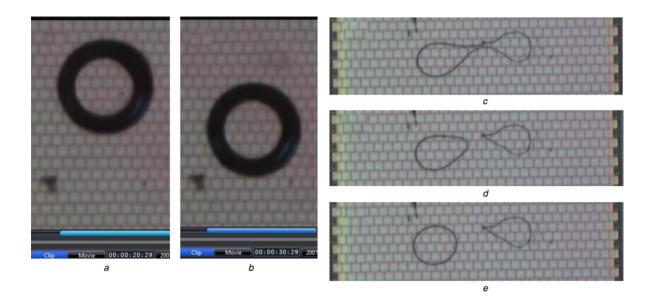


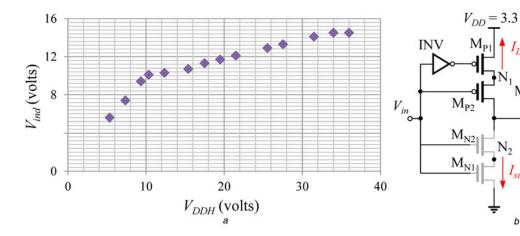
Fig. 7 FPLOC droplet actuations

a and b Droplet movement by EWOD actuations with 220 µm gap height

c Electrode-column droplet cutting is pulling a small droplet from a pinned droplet; the gap height is  $20 \,\mu m$ 

- d Droplet pinched off
- e Droplet is actuated away

DDH



**Fig. 8** Induced voltages and leakage currents *a* Measured induced voltages vs. applied voltages of the FPLOC microelectrode *b* Leakage currents of the bi-state-switch driver in the high-impedance mode

leakage current  $I_{\text{sub,NPG}}$  discharges the induced potential  $V_{\text{ind}}$  of  $C_L$  and  $C_p$ , which consequently degrades the performance of the driver.  $I_{\text{sub,NPG}}$  is then divided into two current paths: one is the reverse current  $I_{D,P}$ , and the other is the sub-threshold leakage current  $I_{\text{sub,N}}$ . For those leakage currents affecting  $V_{\text{ind}}$ , the primary source is the sub-threshold leakage current  $I_{\text{sub,NPG}}$ , which is caused by a large voltage drop on  $M_{\text{NPG}}$ . The subthreshold leakage current can be expressed as [27, 28]

$$I_{\text{sub}} = \mu C_{\text{dep}} \frac{W}{L} V_{\text{T}}^2 \exp\left(\frac{V_{\text{GS}} - V_{\text{th}}}{nV_{\text{T}}}\right) \\ \times \left(1 - \exp\left(\frac{-V_{\text{DS}}}{V_{\text{T}}}\right)\right)$$
(1)

where  $\mu$  denotes the effective mobility;  $C_{dep}$  is the depletion capacitance; W and L are the device width and the effective channel length;  $V_{T}$  denotes the thermal voltage;  $V_{GS}$  represents the gate-to-source voltage;  $V_{th}$  is the threshold voltage; n denotes the subthreshold slope factor; and  $V_{DS}$  represents the drain-to-source voltage.  $V_{ind}$  can be derived as

$$V_{\text{ind}} \simeq \frac{C_L}{C_p + C_L} V_{\text{DDH}} - \frac{1}{C_L} \left( \int_{T_1} \left[ I_{D,P} (V_{\text{DS}}) + I_{\text{sub},N} (V_{\text{DS}}) \right] dt \right)$$
(2)

where  $C_p$  is the parasitic capacitance on the node of  $V_{ind}$ . For  $V_{DDH}$  over 10 V, the reverse leakage current starts to affect the output potential level and when  $V_{DDH}$  keeps increasing to about 35 V, the avalanche breakdown happens. As a result,  $V_{ind}$  maintains constant at about 14.5 V.

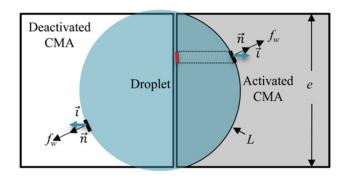
Leakage currents and limited  $V_{ind}$  did have a complicated impact on the droplet actuation of the FPLOC. From Fig. 9, it can be seen that there are two capillary forces acting on the droplet in the unit vector *i* direction. One is the actuated force induced by *V* of the activated electrode, and another is the hindering force induced by the electric potential difference between *V* and  $V_{ind}$  of the deactivated electrode. The hindering force generated by leakage currents reduces the overall droplet actuation force of the FPLOC. Applying equation wetting force of the droplet contact line [29] to both activated and deactivated electrodes and the net *i*-direction capillary force on the droplet is

$$F_{x} = \gamma_{\text{LG}} \cos \theta(V) e - \gamma_{\text{LG}} \cos \theta (V - V_{\text{ind}}) e \qquad (3)$$

$$F_{x} = \gamma_{\text{LG}} \left( \cos \theta(V) - \cos \theta \left( V - V_{\text{ind}} \right) \right) e \tag{4}$$

where  $\gamma_{\text{LG}}$  is the liquid–gas interfacial tension and *e* is the effective length of the contact line.  $\theta(V)$  is the contact angle with the potential, and  $\theta(V-V_{\text{ind}})$  is the contact angle caused by the difference between the applied *V* and the induced voltage  $V_{\text{ind}}$  for the deactivated microelectrode.

Based on the measured  $107^{\circ}$  non-actuated contact angle and the calculated  $31.93 \text{ pF/mm}^2$  capacitance of the dielectric and hydrophobic layers of FPLOC, the Lippmann–Young equation was used to predict the contact angles of different applied voltages. Pairs of V and  $V-V_{\text{ind}}$ were generated from empirical data shown in Fig. 8*a* and then applied into (4) to predict the capillary force  $F_x$ . This exercise predicted the droplet would start to have positive  $F_x$  around applied V=25 V, and then  $F_x$  would peak at about V=30 V. After that, V>30 V,  $F_x$  had no gain but reduced again. Our experiment results were in agreement with the empirical assessments from (4). When the actuation voltage was about 25 V, most droplets started to be actuated. Also, the best working window for EWOD



**Fig. 9** Contact line and the capillary force acting on the droplet in direction of unit vector i

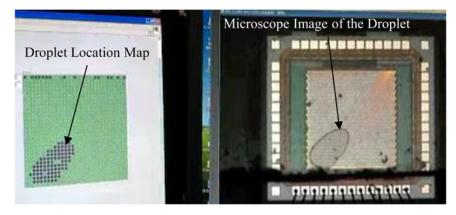


Fig. 10 FPLOC droplet detection: a real-time droplet location map in comparison to the actual droplet image

actuations stayed between 25 and 30 V. Voltages over 30 V did not gain any actuation performance improvement.

#### 8.2 FPLOC droplet detection

The droplet detection function was successfully demonstrated by FPLOC. Fig. 10 shows the real-time comparison between a droplet location map and the actual droplet image. FPLOC Location Map software interpreted the 900-bit OUT pattern into a graphical droplet location map which resembled the actual droplet.

#### 9 Conclusions

The lack of standard EWOD components makes the implementation of the hierarchical top-down design approach difficult. The MEDA architecture offers standard EWOD building elements, microelectrode cells, as a viable solution. The FPLOC based on the MEDA architecture has been demonstrated to show the seamless and simple configuration of microfluidic components and operations by hierarchical software programming of microelectrode cells without sophisticated additional design and packaging techniques. The capability of dynamic configurations and actuations of variable shapes and sizes of digital microfluidic components and their operations opens the possibility of a real field-programmable and reusable biochip platform. This FPLOC was the first EWOD microfluidic device fabricated by 3.3 V CMOS technology. Although the first implementation of the bi-state-switch driver was not perfect, it successfully demonstrated the EWOD droplet actuation capability. This achievement has positioned the well-established and commonly available low-voltage CMOS technology as a good candidate for the mass production of future fully integrated biochips. In addition, by integrating 900 droplet detection circuits into microelectrode cells, the FPLOC also achieved large-scale integration of microfluidics and microelectronics through the CMOS technology.

#### 10 Acknowledgments

The authors are grateful for the support of Department of Electronics Engineering, National Chiao Tung University (NCTU) and 5Y50B project from MOE, Taiwan. All experiments and fabrications for proof of the concept presented in this paper were performed at NCTU.

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