# A GeSi-Buffer Structure for Growth of High-Quality GaAs Epitaxial Layers on a Si Substrate

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A SiGe-buffer structure for growth of high-quality GaAs layers on a Si (100) substrate is proposed. For the growth of this SiGe-buffer structure, a 0.8-μm $Si_{0.1}Ge_{0.9}$ layer was first grown. Because of the large mismatch between this layer and the Si substrate, many dislocations formed near the interface and in the low part of the $Si_{0.1}Ge_{0.9}$ layer. A 0.8-μm $Si_{0.05}Ge_{0.95}$ layer and a 1-μm top Ge layer were subsequently grown. The strained $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces formed can bend and terminate the upward-propagated dislocations very effectively. An in-situ annealing process is also performed for each individual layer. Finally, a 1–3-μm GaAs film was grown by metal-organic chemical vapor deposition (MOCVD) at 600°C. The experimental results show that the dislocation density in the top Ge and GaAs layers can be greatly reduced, and the surface was kept very smooth after growth, while the total thickness of the structure was only 5.1 μm (2.6-μm SiGe-buffer structure + 2.5-μm GaAs layer).

**Key words:** SiGe, GaAs on Si, heterostructure, dislocation, ultrahigh-vacuum chemical vapor deposition (UHV/CVD), metal-organic chemical vapor deposition (MOCVD)

## INTRODUCTION

Heteroepitaxy of III-V compounds on Si substrates is receiving strong interest because of the potential for monolithic integration of III-V and Si devices and opto-electronic integrated circuits.[1] This technology will also provide low-cost, lightweight, and large-area III-V compound substrates with high mechanical strength and excellent thermal conductivity. However, there are two major problems in obtaining high-quality III-V films on Si. One is high density-dislocation generation caused by the large difference of their lattice constants, and another is residual stress caused by the large difference in their thermal expansion coefficients. To grow high-quality GaAs films on Si, the Ge layer can be used as a buffer because Ge and GaAs have similar lattice constants and thermal expansion coefficients.

However, the remaining problem is how to grow a high-quality Ge layer on Si because Ge has a 4.2% lattice mismatch with Si. Various growth techniques and treatments have been developed to solve this problem. It has been reported that the compositionally graded buffer (CGB) layers,[2] low-temperature Si-buffer layers,[3] compliant silicon-on-insulator substrate,[4] two-step procedure,[5] and selective area growth combined with thermal cycle annealing[6] can be used to grow high-quality, strain-relaxed SiGe and Ge layers. Among them, the CGB layers are the most practically and widely used ones today. However, the CGB layers still have two major challenges. First, these CGB layers often suffer from a thickness of approximately 10 μm with a Ge composition ranging from 0 to 1, which makes the integration of devices on the Si-based circuits difficult. Second, the CGB layers often exhibit a crosshatch pattern, which makes the surfaces very rough,[7] and the chemical-mechanical polishing technique has to be employed to solve this problem.

In this paper, we report a new approach to obtaining a high-quality Ge layer, and then report growth of high-quality GaAs on this Ge buffer. The procedure

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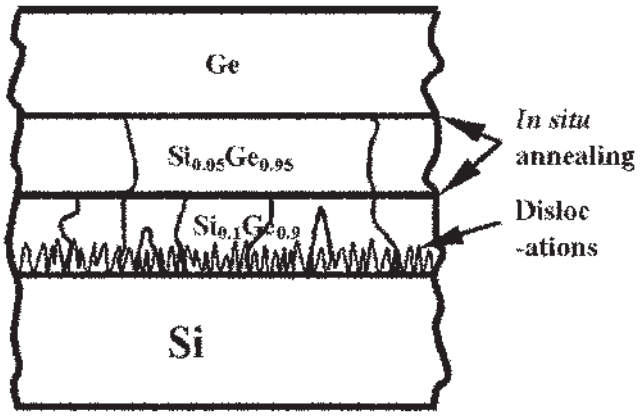


Fig. 1. Mechanism of reducing threading dislocations in the SiGe-buffer structure.

for growth of Ge mainly involves growing three epitaxial layers (Fig. 1). The first layer is the $Si_{0.1}Ge_{0.9}$ layer, the second is the $Si_{0.05}Ge_{0.95}$ layer, and the third is the Ge layer. After the growth of each individual layer, in-situ 750°C annealing for 15 min was performed. Because of the large lattice mismatch at the interface between $Si_{0.1}Ge_{0.9}$ and Si layers, many close small islands are formed during growth at low temperatures. As growth proceeded, these islands quickly coalesced into a continuous film. At the same time, many dislocations generated and interacted with each other to form closed, nonpropagating loops and networks near the interface. A small portion of the dislocations that did not have the chance to pair up continued to propagate upward. A similar technique has been widely used in growing highly mismatched heterostructures, for example, GaN on sapphire.[8] Because of the proper lattice-mismatch strains at the upper interfaces of $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$, the upward-propagated dislocations can be bent sideward and terminated effectively. Details of the behavior of dislocations at the mismatched interfaces can be seen in Refs. 9 and 10. Additionally, the thermal annealing process, which was performed after growing each individual layer, can further reduce dislocation density in the epitaxial layers. The mechanism of threading dislocation reduction employed in this work is shown schematically in Fig. 1.

## EXPERIMENTAL

Growth of SiGe and Ge layers was carried out using an ultrahigh-vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than $2 \times 10^{-8}$ torr.[11] First, a 4-in. Si(100) substrate wafer with a 6° off-cut toward the [110] direction was cleaned by 10% HF dipping and high-temperature baking at 800°C in the growth chamber for 5 min. Then, a 0.8-μm $Si_{0.1}Ge_{0.9}$, a 0.8-μm $Si_{0.05}Ge_{0.95}$, and a 1-μm Ge layer were grown at 400°C in sequence. The growth rate of the Ge layer is 0.8 μm/h. Between successive layers, growth was interrupted for an in-situ, 15-min, 750°C anneal. The GaAs layers were grown by a commercial, (AIXTRON AIX 3000) metal-organic chemical vapor deposition (MOCVD) system on the grown $Ge/Si_{0.05}$ $Ge_{0.95}/Si_{0.1}Ge_{0.9}$ buffer structure at a temperature of 600°C by one step. The growth conditions of GaAs are as follows: growth pressure is 40 torr, V/III ratio is 100, and growth rate is 1.7 μm/h. Transmission electron microscopy (TEM) was used to observe the thickness of the epitaxial layers and the dislocation distribution and to estimate the threading dislocation density. The Ge surface morphology was analyzed by Nanoscope III atomic-force microscopy (AFM) in the contact mode. The x-ray diffraction and photoluminescence (PL) were additionally used to evaluate the crystalline quality of the sample.

## RESULTS AND DISCUSSION

Figure 2 shows the cross-sectional TEM image of the SiGe-buffer structure. There are a large number of dislocations located near the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. The upwardly propagated dislocations are bent sideward and terminated very effectively at the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$ interfaces. Almost no threading dislocation can propagate into the top Ge layer. The image shows that the total thickness of these three epitaxial layers is only approximately 2.6 μm, which is much smaller than that of CGB layers reported earlier. By analyzing several plan-view TEM images, the threading dislocation density is estimated to be about $3 \times 10^6$ $cm^{-2}$. In this study, the Ge composition variation at the two strained interfaces is set at 0.05. We found[12] that, if the Ge composition variation is too large, new dislocations will generate from the interfaces because of the relatively large lattice mismatch. On the contrary, if the Ge composition variation is too small, the mismatch stress formed at the interfaces is not strong enough to terminate the dislocations effectively.

The surface roughness was measured by AFM. Figure 3 presents the AFM images of the surfaces of

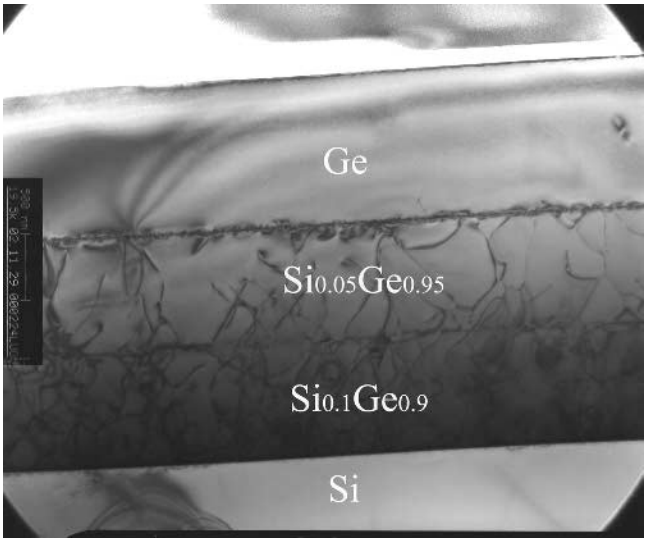


Fig. 2. Cross-sectional TEM image of the SiGe-buffer structure.

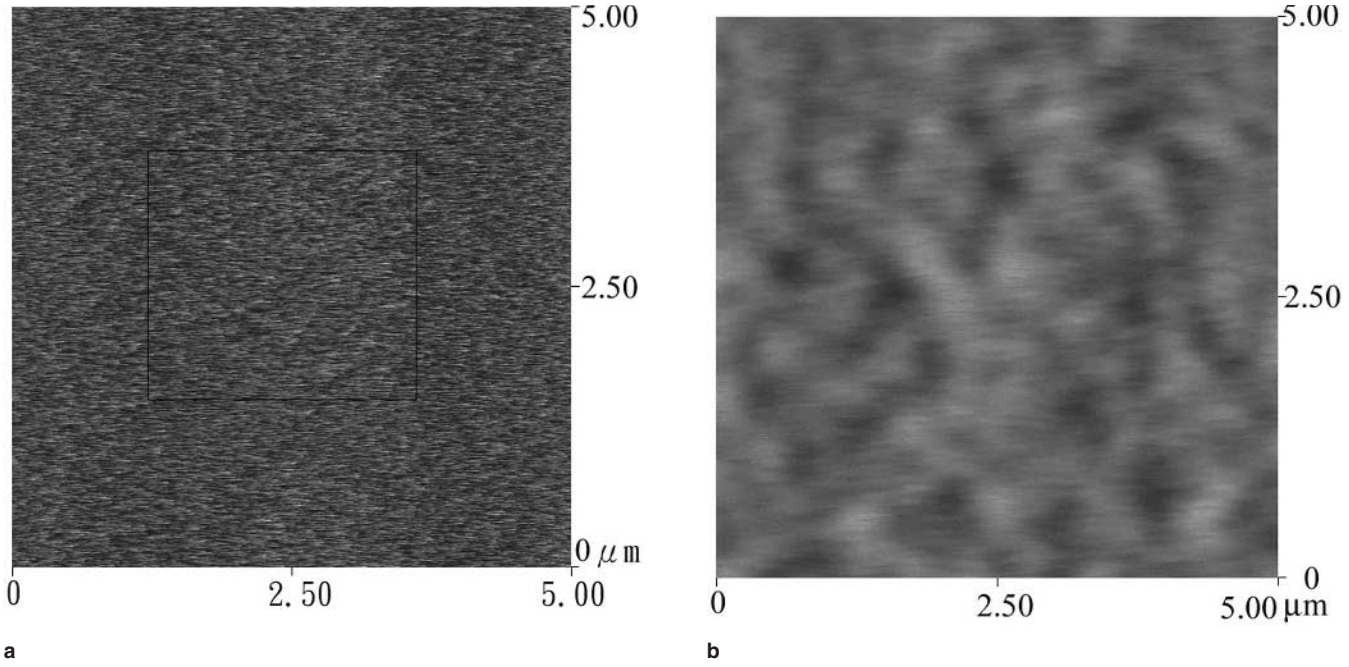


Fig. 3. The AFM images of the surfaces of the (a) Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ sample and (b) GaAs/Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ sample.

the (a) Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ sample and (b) GaAs/Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ sample. No crosshatching pattern on both Ge and GaAs surfaces were observed. The root mean square (RMS) of the Ge surface is only 32 Å, which is much smaller than that of the CGB layers (about 180 Å) reported in Ref. 13. The RMS of the surface for the GaAs/Ge/$Si_{0.05}$ $Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ sample is 61.2 Å, in comparison to an RMS of 11.3 Å for the surface of the GaAs/GaAs sample.

Figure 4 shows the cross-sectional TEM (XTEM) image of the GaAs layer grown on the Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ buffer structure by MOCVD at 600°C. The thickness of the GaAs layer is about 2.5 μm. It can be seen that dislocation density in the GaAs layer appears to be greatly reduced in comparison with the sample of GaAs grown directly on Si, reported in Ref. 14, where the dislocation density shown in the XTEM image is high. Additionally, because the 0.01% lattice mismatch still exists between GaAs and Ge, a weak strain field at the GaAs/Ge interface is induced. The XTEM image also clearly shows this strain field at the GaAs/Ge interface.

Figure 5 is the x-ray diffraction curve of the sample. It also indicates that the crystalline quality of GaAs is quite good. Figure 6 is its PL spectrum measured at 13 K; it can be seen that the PL intensity of GaAs

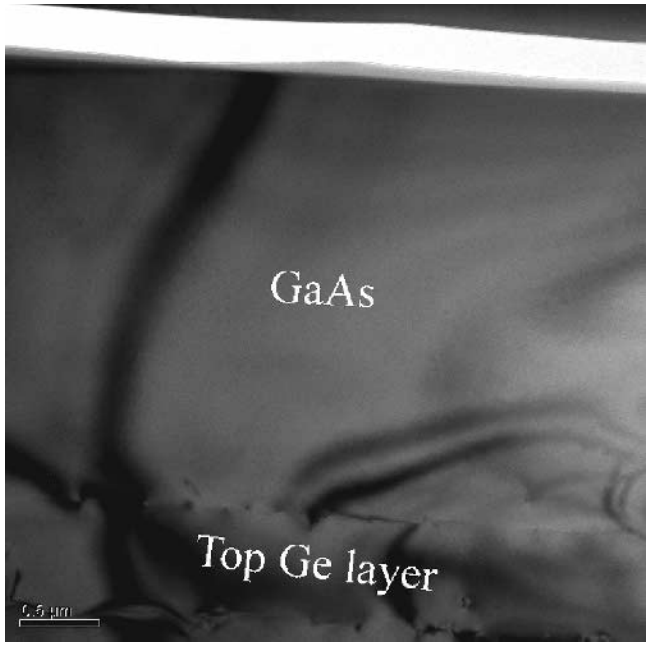


Fig. 4. The 2.5-μm GaAs layer grown on the SiGe-buffer structure by MOCVD.

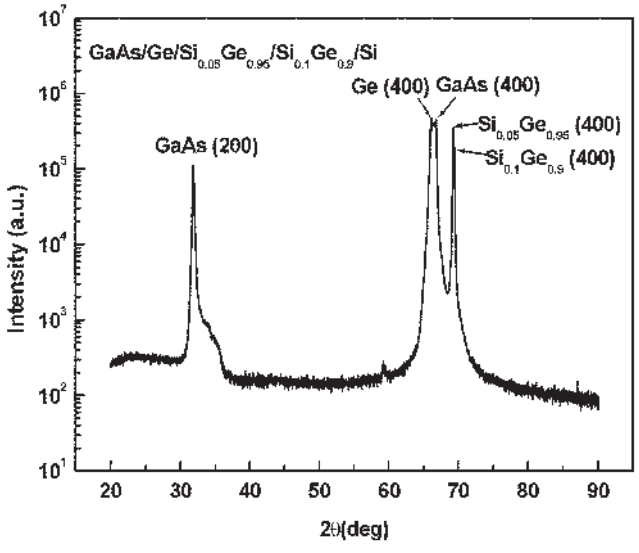


Fig. 5. The x-ray diffraction curve of the sample.

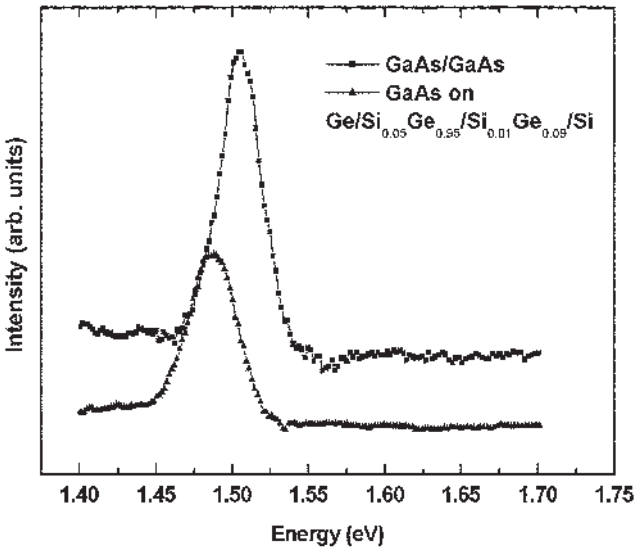


Fig. 6. The PL spectrum of the sample at 13 K.

grown on the proposed SiGe-buffer structure is comparable with that of the homoepitaxial GaAs layer. However, its peak position has a small shift from that of the homoepitaxial GaAs layer. This may be because there is a little stress in this layer.

## CONCLUSIONS

We have designed a novel SiGe-buffer structure for growth of high-quality GaAs on Si substrates. The method mainly involves the following: (1) growth of three layers consisting of a 0.8-μm $Si_{0.1}Ge_{0.9}$ layer, a 0.8-μm $Si_{0.05}Ge_{0.95}$ layer, and a 1-μm top Ge layer; and (2) in-situ, 750°C annealing for 15 min performed on each individual layer. By this procedure, many dislocations were formed at the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. Moreover, the upwardly propagated dislocations can be bent and terminated effectively at the interfaces of $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$. The top Ge layer exhibits a low threading dislocation density and a smooth surface. Finally, using this Ge layer as a buffer, we have grown a high-quality GaAs layer on the Si(100) substrate with a 6° off-cut toward the [110] direction.

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