

# New Observation and the Modeling of Gate and Drain Currents in Off-state P-MOSFET's

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**Abstract**—The work reports new observations concerning the gate and drain currents measured at off-state conditions in buried-type p-channel LDD MOSFET devices. Detailed investigation of the observed phenomena reveals that 1) the drain current can be separated into two distinct components: band-to-band tunneling in the gate-to-drain overlap region and collection of holes generated via impact ionization by electrons inside the oxide; and 2) the gate current can be separated into two distinct components: the hot electron injection into the oxide and the Fowler–Nordheim electron tunneling through the oxide. At low negative drain voltage, the dominant component of the drain current is the hole generation inside the oxide. At high negative drain voltage, the drain current is essentially due to band-to-band tunneling, and it is correlated with the hot-electron injection-induced gate current.

## I. INTRODUCTION

THE gate and drain currents in off-state MOS devices have recently been studied extensively [1]–[15]. An understanding of the mechanisms responsible for these currents as well as their control is very important to device application and to reliability study. In the work of [1]–[14], the drain leakage current has been judged to be dominated by one or more of the mechanisms occurring in the gate-to-drain overlap region: the band-to-band tunneling [1]–[3], [9]–[14], the trap-assisted tunneling [5], and the surface diffusion-limited transport [8]; and the gate current has been interpreted by one or more of the following mechanisms: the hot-carrier injection into the oxide [4], [6], [7], [12] and the electron Fowler–Nordheim (F–N) tunneling through the oxide [4], [6], [11]. In our previous work [15], we measured gate and drain currents in off-state 180 Å gate oxide buried-type LDD p-MOSFET device. It turned out that the gate current is dominated by the F–N tunneling of electrons from the surface beneath the gate and the holes generated via impact ionization by electrons within the oxide constitute the drain leakage current. However, the ability to accurately model the drain current component due to hole generation inside the oxide has not been established in [15]. Since the measurement condition was limited to low negative drain voltages [15], no other currents due to the band-to-band tunneling and hot-carrier injection have been found in

the drain and gate, respectively. However, as we modify this measurement condition by slightly increasing negatively the drain voltage, a dramatically large change in I–V characteristics is observed, which is not reported in [15]. Such experimental observations have been found to be reproducible for devices with gate oxide thickness of 106–185 Å. An investigation of these new I–V characteristics has revealed that 1) both the band-to-band tunneling and the holes generated inside the oxide simultaneously contribute to the drain leakage current; and 2) both the hot-electron injection and the electron F–N tunneling simultaneously contribute to the gate current. In this paper, we will report these observation results along with the detailed analysis and modeling.

## II. EXPERIMENTAL OBSERVATION

The work is based on the n<sup>+</sup>-gate buried-type p-channel LDD MOSFET devices having three gate oxide thicknesses of 106, 146, and 185 Å. The corresponding gate width to length ratios are 50 μm/0.7 μm, 100 μm/1.0 μm, and 100 μm/1.5 μm, respectively. The devices were fabricated by a 0.6-μm twin-well polysilicon CMOS process. The starting material was p-type <100>-oriented wafers with resistivity of 8–12 Ω-cm. Phosphorus (6.0 × 10<sup>12</sup> cm<sup>-2</sup>, 150 KeV) was implanted to form the n-well region. BF<sub>2</sub> (2.6 × 10<sup>12</sup> cm<sup>-2</sup>, 70 KeV) was used as the threshold voltage implant. The gate oxide was grown in dry O<sub>2</sub> at 920 °C. After n<sup>+</sup> gate polysilicon was formed, BF<sub>2</sub> (1.0 × 10<sup>13</sup> cm<sup>-2</sup>, 45° angle rotating, 50 KeV) was implanted to form the low-doped drain region and BF<sub>2</sub> (3.0 × 10<sup>15</sup> cm<sup>-2</sup>, 70 KeV) was implanted to form the highly doped drain region. The junction depth and surface doping concentration of the low-doped drain have been determined to be about 0.25 μm and 3.0 × 10<sup>18</sup> cm<sup>-3</sup>, respectively. The threshold voltage values of the samples are around -0.7 V.

We have found that the experimental observations to be demonstrated later are independent of the gate oxide thickness. Therefore, unless stated otherwise, only the measurement results from the 146 Å gate oxide case are presented. With the source floating and the n-well grounded, each structure with the assigned drain terminal condition has been characterized as shown schematically in Fig. 1. Under this condition, the gate and drain currents have been measured as function of gate voltage ranging from 0 to 20 V. Unless stated otherwise, the measurement results presented in this paper have been performed at room temperature of 27 °C. The drain and gate current measurement results for  $V_D = 0, -3, -5,$  and  $-7$  V are shown in Fig. 2 and 3, respectively. The measured

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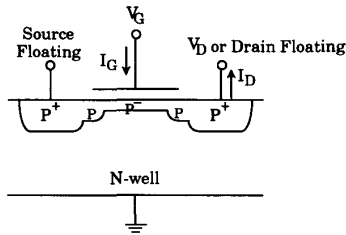


Fig. 1. The terminal connection condition of the buried-type p-MOSFET device for measuring the off-state gate and drain currents.

gate current versus gate voltage for the drain floated is also depicted in Fig. 3. For  $V_D = 0$  and  $-3$  V, 1) both the gate and drain currents are independent of drain voltage; and 2) the gate current  $I_G$  is greater than the drain current  $I_D$  with an  $I_G/I_D$  ratio of about  $1 \times 10^2$  to  $2 \times 10^3$ . Moreover, the gate current is not affected when the drain is floated. These observation results at high gate voltage are indeed in good agreement with those reported in a  $180 \text{ \AA}$  gate oxide p-MOSFET device fabricated by the  $0.8 \text{ \mu m}$  polycide CMOS process [15]. However, as we increase negatively the drain voltage from  $-3$  V to  $-5$  V, a dramatically large change in I-V characteristics occurs. We can observe that a significant drain current at  $V_D = -5$  V appears in a wide range of  $V_G$  between 4 and 17 V while in most of this range (i.e.,  $4 \text{ V} < V_G < 13 \text{ V}$ ) no data of interest except the measurement noise or conventional thermal generation current can be detected in the drain for  $V_D = 0$  and  $-3$  V. Only for high gate voltage greater than about 17 V as shown in Fig. 2, the drain current is becoming independent of  $V_D$  ranging from 0 to  $-5$  V. Since the measurement noise disturbs the low current regime in Fig. 3, no change in the gate current can be accurately detected. This difficulty can be overcome by increasing the measurement temperature. The measurement results of the drain and gate currents at  $V_D = -5$  V for two different temperatures of 27 and  $75^\circ\text{C}$  are shown in Fig. 2 and 3, respectively. The measured drain current shown in Fig. 2 exhibits a positive temperature coefficient, i.e., the drain current increases as the temperature increases. From Fig. 3 we can confidently determine a detectable range of  $V_G$  between 7–11 V for  $V_D = -5$  V at  $75^\circ\text{C}$ , where the gate current can be recognized to be significantly different from the measurement noise or conventional thermal generation as obtained at room temperature. Moreover, this new observation can be demonstrated more clearly by simply changing  $V_D$  from  $-5$  V to  $-7$  V. The corresponding measurement results are shown in Figs. 2 and 3, from which it can be clearly seen that the drain current exponentially increases with increasing  $V_D$ . A dramatic change in the  $I_G$  for  $V_D = -7$  V has also been observed for a wide range of  $V_G$  between 4 and 14 V while for  $V_G$  greater than about 14 V the gate current is becoming independent of drain voltage.

The ratio of the measured gate to drain current is shown in Fig. 4 for  $V_D = 0, -3,$  and  $-7$  V as well as for  $V_D = -5$  V at  $75^\circ\text{C}$ . From Fig. 4 we can observe that the gate to drain current ratio corresponding to  $V_D = 0$  and  $-3$  V ranges from

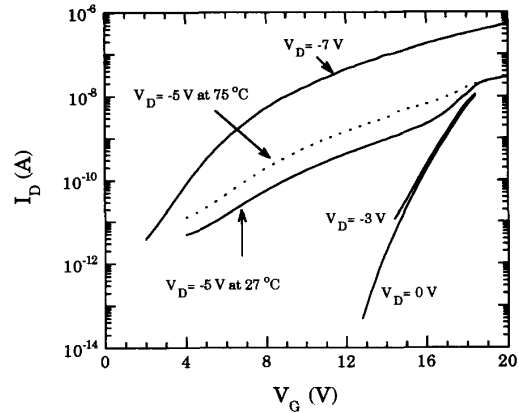


Fig. 2. The measured drain current versus gate voltage characteristics for four different drain voltages of 0,  $-3$ ,  $-5$ , and  $-7$  V. The drain current versus gate voltage characteristic obtained at  $75^\circ\text{C}$  for  $V_D = -5$  V is also shown for comparison. The current components due to the measurement noise and conventional thermal generation have been subtracted for clarity. The gate oxide thickness is  $146 \text{ \AA}$ .

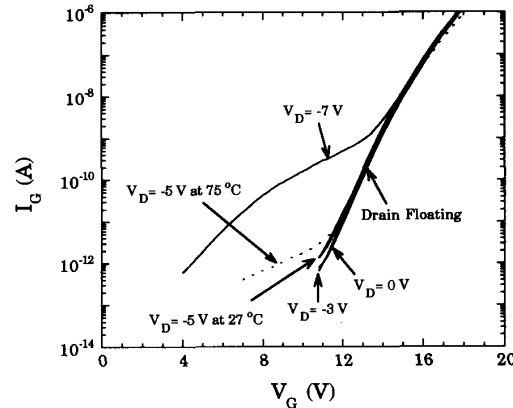


Fig. 3. The measured gate current versus gate voltage characteristics corresponding to Fig. 2. The gate current versus gate voltage characteristic for the drain floated is also shown.

$1 \times 10^2$  and  $2 \times 10^3$  and decreases with increasing gate voltage. It can be seen from Fig. 4 that for  $V_D = -7$  V there exists a wide  $V_G$  range about between 4 and 14 V where the gate to drain current ratio is almost a constant of about  $1 \times 10^{-2}$ ; and from  $V_G = 14$  V this ratio starts to increase exponentially with increasing the gate voltage. The case of  $V_D = -5$  V at  $75^\circ\text{C}$  is similar to that of  $V_D = -7$  V but with two significant differences: 1) there is a relatively small  $V_G$  range of about 7–11 V where the gate to drain current ratio can be reasonably considered constant; and 2) this constant is about  $3 \times 10^{-3}$ , considerably smaller than that at  $V_D = -7$  V.

### III. F-N TUNNELING AND HOLE GENERATION

The measurement results mentioned above show that for small values of  $V_D$  (i.e.,  $V_D = 0$ – $3$  V) 1) the drain current is less than the gate current by about two to three orders

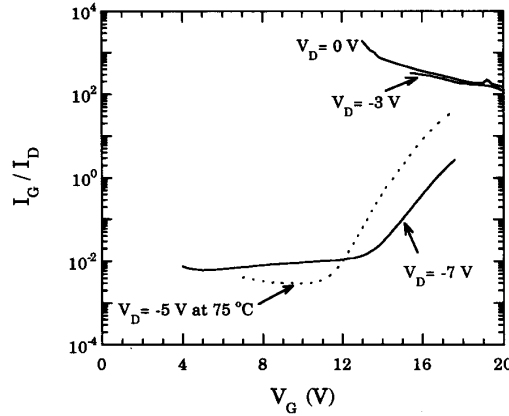


Fig. 4. The gate to drain current ratio as function of gate voltage for  $V_D = 0, -3,$  and  $-7$  V as well as for  $V_D = -5$  V at  $75^\circ\text{C}$ . The drain current is from Fig. 2 and the gate current is from Fig. 3.

of magnitude; 2) both the gate and drain currents are independent of drain voltage; and 3) the gate current is not affected by making the drain floated. Such characteristics appearing primarily at high positive gate voltage can be explained satisfactorily based on the formation of the surface  $n^+$  inversion layer due to the punchthrough of the buried channel to the underlying shallow p-n junction [15]. The electron F-N tunneling from this layer and the collection of the holes generated via impact ionization by electrons inside the oxide have been judged experimentally to contribute the gate and drain currents, respectively [15], [16]. To further judge the validity of this interpretation, we measured gate and drain currents for three different oxide thicknesses (Figs. 5 and 6). Fig. 6 also labels the values of gate voltage for instant oxide breakdown. The F-N tunneling current component  $I_{G1}$  has been calculated using the expression [17]:

$$I_{G1} = A_G \alpha_1 E_{ox}^2 \exp(-\alpha_2/E_{ox}) \quad (1)$$

where  $A_G$  is the oxide area,  $T_{ox}$  is the oxide thickness, and  $E_{ox} (\simeq V_G/T_{ox}$  for large  $V_G$  values) is the oxide field strength. The values of two constants  $\alpha_1 = 1.76 \times 10^{-6} \text{ A/V}^2$  and  $\alpha_2 = 245.5 \text{ MV/cm}$  have been obtained by fitting the measured gate current in Fig. 5. These fitted parameters values have been found to be comparable with those of  $\alpha_1 = 2.3 \times 10^{-6} \text{ A/V}^2$  and  $\alpha_2 = 238.5 \text{ MV/cm}$  as cited in [18]. The calculated results based on our fitted parameter values have been supported by the experimental data in Fig. 5. From Fig. 5 it can be observed that except at the high current level where the effects of the trapped charges dominate, the agreement with experimental I-V data for three different oxide thicknesses has been simultaneously achieved.

According to the work [15], [16], not only the holes generated inside the high-field oxide are linked to the electron tunneling from the  $n^+$  inversion layer surface, but also both are function of only the oxide field. Therefore, the mechanism of the holes generated via impact ionization by electrons within

the oxide is suggested to be the origin of our measured drain hole current. Indeed, in Fig. 6 the drain current density  $J_D$  is independent of the bias  $V_D$ , indicating the role of the drain only for collecting the holes generated. Based on the published impact ionization coefficient model [19], [20], the drain current component  $I_{D1}$  by collecting the holes generated inside the oxide has been calculated [16]:

$$I_{D1} = \alpha_o \exp(-H/E_{ox})(T_{ox} - T_t)I_{G1} \quad (2)$$

where the parameter values of  $\alpha_o = 3.3 \times 10^6 \text{ cm}^{-1}$  and  $H = 80 \text{ MV/cm}$  as cited in [19], [20] are used.  $T_t (= \phi_B/qE_{ox}$  for barrier height  $\phi_B = 3.2 \text{ eV}$ ) is the tunneling distance and the value of  $(T_{ox} - T_t)$  is the effective length for impact ionization. By substituting the experimental data in Fig. 5 into (2), the calculated results are shown in Fig. 6. It can be observed from Fig. 6 that without any parameter adjusting, the agreement with experimental I-V data for three different oxide thicknesses is very good.

The phenomenon of oxide breakdown has been noted in Fig. 6. Here we demonstrate the correlation of the hole generation to oxide breakdown. Based on the hole-trapping-induced breakdown model [16], [19], oxide breakdown occurs when the density of trapped holes reaches some critical value  $Q_{ot}^+$ :

$$Q_{ot}^+ = \theta \int_0^{t_{bd}} J_D dt \quad (3)$$

where  $\theta$  is the trapping efficiency and  $t_{bd}$  is the time necessary for breakdown. To evaluate (3) more easily, a ramp voltage for  $V_G$  with the ramp rate  $R$  (volts per second) has been assumed. As a result, (3) can be written as

$$Q_{ot}^+ = \frac{\theta}{R} \int_0^{V_{GB}} J_D dV_G \quad (4)$$

where  $V_{GB}$  is the gate voltage for instant breakdown. Based on the experimental data in Fig. 6, the values of  $Q_{ot}^+ R/\theta$  have been calculated using (4) to be  $1.03 \times 10^{-2}$ ,  $1.44 \times 10^{-2}$ , and  $1.05 \times 10^{-2} \text{ A} \cdot \text{V/cm}^2$  for  $T_{ox} = 106, 146,$  and  $185 \text{ \AA}$ , respectively. The close agreement between these calculated values supports the hole generation mechanism proposed above for the measured drain current.

#### IV. ANALYSIS AND DISCUSSION

As we increase negatively the drain voltage from  $V_D = -3$  V by a small value, a significant change in I-V characteristics occurs as shown in Fig. 2 and 3 for  $V_D = -5$  and  $-7$  V. We can attribute the increased drain current to one or more of the mechanisms: the band-to-band tunneling [1]–[3], the trap-assisted tunneling [5], and the surface diffusion-limited transport [8]. We favor band-to-band tunneling, by considering several data: 1) the associated drain voltage magnitude (i.e., 5 V and 7 V) is less than our measured drain breakdown voltage of about 13 V; and 2) the drain current has a positive temperature coefficient as shown in Fig. 2. To model the drain

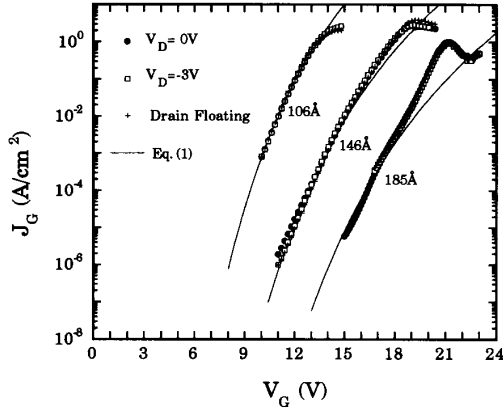


Fig. 5. The gate current density  $J_G$  versus gate voltage  $V_G$  measured under different connection conditions of the drain terminal for three different oxide thicknesses. The calculated results using (1) are also shown for comparison.

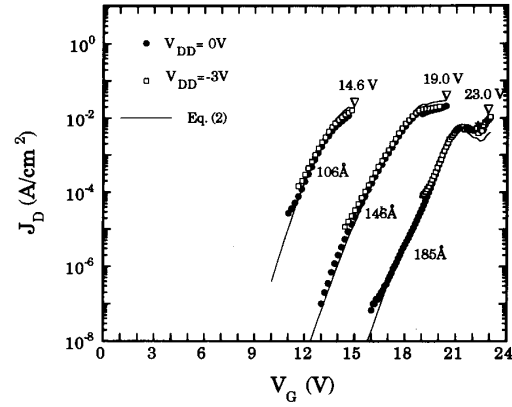


Fig. 6. The drain current density  $J_D$  versus gate voltage  $V_G$  measured under different connection conditions of the drain terminal for three different oxide thicknesses. The gate voltage values for instant oxide breakdown are labeled. The calculated results using (2) with the measured  $J_G$  in Fig. 5 as input parameter are also shown for comparison.

current component  $I_{D2}$  for  $V_D = -7$  V, an analytic model of band-to-band tunneling is considered [1]–[3]:

$$I_{D2} = \beta_1 E_{si} \exp(-\beta_2/E_{si}) \quad (5)$$

where  $\beta_1$  and  $\beta_2$  are two fitting parameters and  $E_{si}$  is the effective field strength. The deep depletion approximation has been utilized for the  $E_{si}$ :

$$V_{si} = (V_G - V_D) + 9qN_A T_{ox}^2 / \epsilon_{si} - ((V_G - V_D + 9qN_A T_{ox}^2 / \epsilon_{si})^2 - (V_G - V_D)^2)^{1/2} \quad (6)$$

$$E_{si} = \frac{1}{2} (2qN_A V_{si} / \epsilon_{si})^{1/2} \quad (7)$$

where  $V_{si}$  is the silicon surface band-bending voltage,  $N_A$  is the effective drain doping concentration, and  $\epsilon_{si}$  is the silicon permittivity. Note that a linear distribution of the vertical electric field as recently reported in [14] has been utilized for (7). Based on (5)–(7) the values of  $\beta_1 = 2.842 \times 10^{-9}$  A-cm/V and  $\beta_2 = 15.16$  MV/cm have been properly extracted for  $V_D = -7$  V. The corresponding calculated drain current is shown in Fig. 7 where the experimental data for  $V_D = -7$  V are also shown for comparison. From Fig. 7 we can observe that a reasonable agreement with experimental data has been achieved, indicating the role of the band-to-band tunneling in this case.

A significant gate current for  $V_D = -7$  V has been detected over the  $V_G$  range from about 4–14 V. This range of  $V_G$  is narrowed to between about 7–11 V for  $V_D = -5$  V at 75°C. In these ranges the gate current cannot be accounted for simply by the F–N tunneling mechanism. We attribute this current to the hot-electron injection into the oxide under the influence of the surface lateral field in the gate-drain overlap region. The reasons are as follows: 1) for the  $V_D$  fixed to  $-7$  V, the gate to drain current ratio is nearly a constant over a wide  $V_G$  range from 4 to 14 V as shown in Fig. 4, indicating the role of the surface lateral field for this ratio; 2) this ratio for  $V_D = -5$  V at 75°C is also a constant over a relatively small  $V_G$  range as shown in Fig. 4; and 3) over the same  $V_G$  range of between

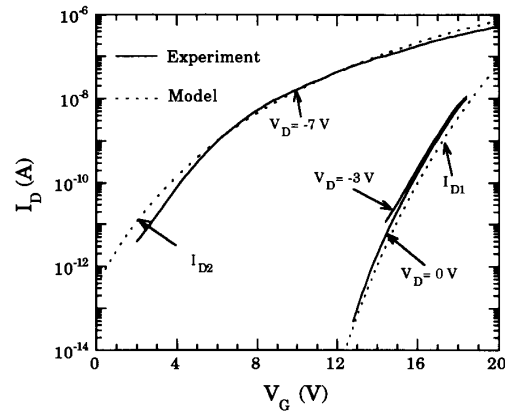


Fig. 7. The calculated drain current as function of gate voltage by the impact ionization generation expression (2) for  $V_D = 0$  and  $-3$  V, and by the band-to-band tunneling expression (5) for  $V_D = -7$  V. The associated experimental data are deduced from Fig. 2 for comparison.

7 and 11 V the gate to drain current ratio for  $V_D = -7$  V is larger than that for  $V_D = -5$  V at 75°C as shown in Fig. 4, in agreement with the lucky electron concept [21], [22] since the lateral field decreases as the reverse-bias drain voltage magnitude decreases. The corresponding gate current component  $I_{G2}$  can be modeled by an empirical expression based on the lucky electron model [21], [22]:

$$I_{G2} = \eta I_{D2} \quad (8)$$

where the coefficient  $\eta$  is a constant for a fixed  $V_D$ . This can be identified by noting from Fig. 4 that the ratio of the gate to drain current for  $V_D = -7$  V has a constant value of about  $1 \times 10^{-2}$  over  $V_G = 4$  to 14 V. To confirm the proposed interpretations, the calculated gate current using (8) with  $\eta = 1 \times 10^{-2}$  for  $V_D = -7$  V is shown in Fig. 8 along with the experimental data. The gate current calculated by summing (1) and (8), i.e.,  $I_G = I_{G1} + I_{G2}$ , is also shown in Fig. 8 for comparison. From Fig. 8, we can observe that close

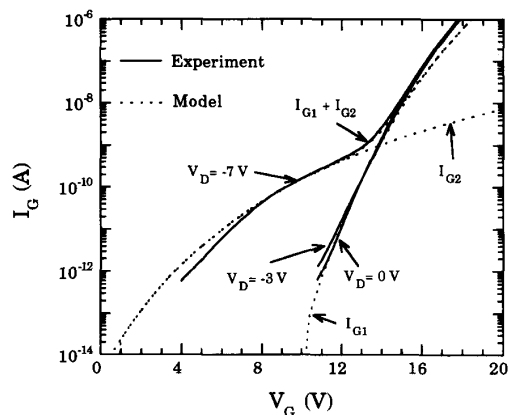


Fig. 8. The calculated gate current as function of gate voltage by the F-N tunneling expression (1) for  $V_D = 0$  and  $-3$  V, and by the hot-electron injection expression (8) with  $\eta = 1 \times 10^{-2}$  for  $V_D = -7$  V. The associated experimental data are deduced from Fig. 3 for comparison. The superposition of the gate current components from (1) and (8) is also demonstrated.

agreements with experimental data have been achieved. Also we have found that for  $V_G < 14$  V we have  $I_{G1} \ll I_{G2}$  while  $I_{G1} \gg I_{G2}$  for  $V_G > 14$  V.

#### V. CONCLUSION

I-V characteristics in the gate and drain have been measured in the off-state buried-type p-MOSFET devices. Two drain current components are witnessed: band-to-band tunneling in the gate-drain overlap region and the collection of the holes generated inside the oxide. The gate current components are hot-electron injection into the oxide and the F-N electron tunneling through the oxide. The correlation between the drain current component due to the band-to-band tunneling and the gate current component due to the hot-electron injection has been successfully modeled. The gate current component due to the F-N tunneling has also been successfully correlated to the drain current component due to the hole generation in oxide without adjusting any parameter.

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