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ELECTROMAGNETIC SIMULATION OF VLSI CIRCUITS BY THE MODIFIED ADI-FDTD METHOD

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ABSTRACT: The alternating direction implicit (ADI) finite-difference time-domain (FDTD) method can be used to simulate very large scale integration (VLSI) circuits efficiently as the time step is not restricted by the Courant–Friedrich–Levy stability condition. When the Berenger’s split-field perfectly matched layer (PML) absorbing boundary condition is used for the ADI-FDTD method for open region simulation, the PML implementation will make this scheme unstable. In this article, the modified PML conductivity profiles are proposed to improve the stability of this scheme. Numerical simulations of the VLSI interconnect and RF inductor in time domain and frequency domain will be demonstrated to show the efficiency and accuracy of this method. © 2014 Wiley Periodicals, Inc. Microwave Opt Technol Lett 56:2530–2534, 2014; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.28643

Key words: alternating-direction implicit; finite-difference time-domain; perfectly matched layer; modified conductivity profile; stability

1. INTRODUCTION

The finite-difference time-domain (FDTD) method is widely used for solving electromagnetic problems [1]. As the FDTD method must satisfy the Courant, Friedrich, and Levy (CFL) condition, the maximum time step size is limited by the minimum cell size. When using the FDTD method to analyze the electromagnetic effects in the very large scale integration (VLSI) circuits, the cell size will be chosen to be micron-scale to accurately model the geometry features. The maximum time step size will be fixed to avoid the numerical instability. Therefore, simulation of the VLSI circuits by FDTD method will be very computational intensive.

Recently, an alternating direction implicit finite-difference time-domain (ADI-FDTD) method is proposed to overcome this problem [2, 3]. The ADI-FDTD method is an attractive method as the time step size is not restricted by the CFL condition. Therefore, this method can model the electromagnetic effects of the VLSI circuits efficiently. To model unbounded region problems, the Berenger’s split-field perfectly matched layer (PML)

[4] was used for the ADI-FDTD method [5]. However, the implementation of Berenger’s PML in the ADI-FDTD method will affect the stability of this scheme. In [6, 7], it is found that the ADI-FDTD method with Berenger’s PML will lead to late-time instability. The frequency domain characteristics of the VLSI circuit can be obtained from the Fourier transform of the transient time domain waveform and it requires a large number of time steps to complete the simulation. This study will be difficult or even impossible due to the late-time instability of ADI-FDTD method with PML absorbing boundary condition (ABC). It is not apparent in the literature that anyone has studied the frequency domain characteristics of the VLSI circuits by the ADI-FDTD method with PML ABC.

In [8], it is found that the PML conductivity profile will affect the stability of the ADI-FDTD method with Berenger’s PML absorber. The modified PML conductivity profile was proposed to improve the stability of this scheme. Based on the study in [8], the modified PML conductivity profile is used in this work to investigate the electromagnetic effects of the VLSI circuits in time domain and frequency domain. From the simulation results, it is found that the instability of this scheme can be improved with the modified conductivity profiles. Numerical simulations of the VLSI interconnect and RF inductor will be performed to show the efficiency and accuracy of the proposed scheme.

2. ADI-FDTD METHOD WITH MODIFIED PML CONDUCTIVITY PROFILE

The formulations of ADI-FDTD method with Berenger’s PML can be written in the spatial spectral domain in matrix form. For simplicity, a 2-D TM wave is studied. This scheme can be split into two updating procedures. For the first updating procedure, the amplification matrix can be shown as [7]

$$M_1 X^{n+\frac{1}{2}} = P_1 X^n \quad (1)$$

where

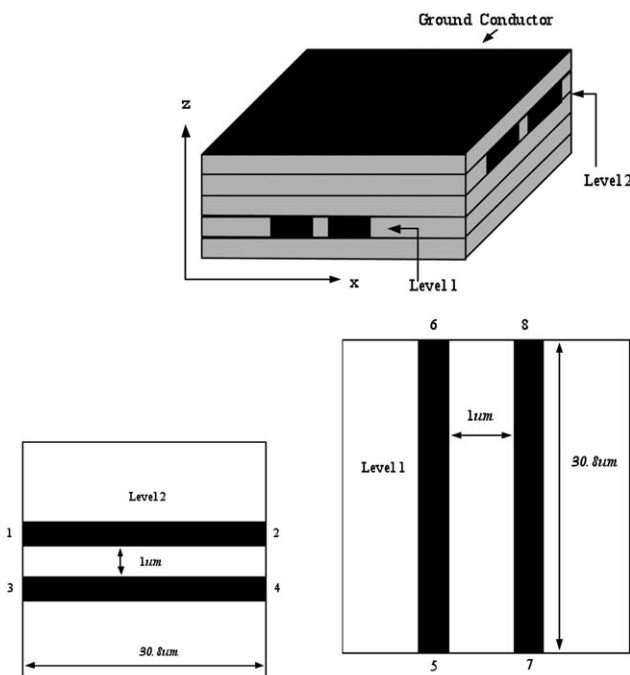


Figure 1 Multilevel crossover

$$\begin{aligned}
\mathbf{X}^n &= \begin{bmatrix} E_{zx}^n & E_{zy}^n & H_x^n & H_y^n \end{bmatrix} \\
M_1 &= \begin{bmatrix} \begin{pmatrix} 1 + C_{bx} \cdot 2j \cdot D_{bx1} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) e^{-j\frac{k_x \Delta x}{2}} \\ -C_{bx} \cdot 2j \cdot D_{bx2} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) e^{j\frac{k_x \Delta x}{2}} \\ 0 \\ 0 \\ 2j \cdot D_{bx,1} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) \end{pmatrix} & \begin{pmatrix} C_{bx} \cdot 2j \cdot D_{bx1} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) e^{-j\frac{k_x \Delta x}{2}} \\ -C_{bx} \cdot 2j \cdot D_{bx2} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) e^{j\frac{k_x \Delta x}{2}} \\ 1 \\ 0 \\ 2j \cdot D_{bx,1} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) \end{pmatrix} & \begin{matrix} 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{matrix} \\
P_1 &= \begin{bmatrix} C_{ax} & 0 & 0 & C_{bx} \cdot \begin{pmatrix} D_{ax1} \cdot e^{-j\frac{k_x \Delta x}{2}} \\ -D_{ax2} \cdot e^{j\frac{k_x \Delta x}{2}} \end{pmatrix} \\ 0 & C_{ay} & 2j \cdot C_{by} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) & 0 \\ 2j \cdot D_{by,1} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) & 2j \cdot D_{by,1} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) & D_{ay,1} & 0 \\ 0 & 0 & 0 & D_{ay,1} \end{bmatrix}
\end{aligned}$$

and

$$\begin{aligned}
C_{as} &= \frac{1 - \frac{\sigma_s \Delta t}{4\epsilon}}{1 + \frac{\sigma_s \Delta t}{4\epsilon}} \quad C_{bs} = \frac{\frac{\Delta t}{2\epsilon \Delta s}}{1 + \frac{\sigma_s \Delta t}{4\epsilon}} \quad D_{as,n} = \frac{1 - \frac{\sigma_{s,n} * \Delta t}{4\mu}}{1 + \frac{\sigma_{s,n} * \Delta t}{4\mu}} \quad D_{bs,n} = \frac{\frac{\Delta t}{2\mu \Delta s}}{1 + \frac{\sigma_{s,n} * \Delta t}{4\mu}} \\
s &= x, y; \quad n = 1, 2 \quad \sigma_{x,1}^* = \sigma_{xi+1/2,j}^*, \quad \sigma_{x,2}^* = \sigma_{xi+1/2,j}^*, \quad \sigma_{y,1}^* = \sigma_{yi,j+1/2}^*, \quad \sigma_{y,2}^* = \sigma_{yi,j+1/2}^*
\end{aligned}$$

For the second updating procedure, the amplification matrix can be expressed as

$$M_2 \mathbf{X}^{n+1} = P_2 \mathbf{X}^{n+\frac{1}{2}} \quad (2)$$

where

$$\begin{aligned}
M_2 &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ \begin{pmatrix} C_{by} \cdot 2j \cdot D_{by1} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) e^{-j\frac{k_y \Delta y}{2}} \\ -C_{by} \cdot 2j \cdot D_{by2} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) e^{j\frac{k_y \Delta y}{2}} \end{pmatrix} & \begin{pmatrix} 1 + C_{by} \cdot 2j \cdot D_{by1} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) e^{-j\frac{k_y \Delta y}{2}} \\ -C_{by} \cdot 2j \cdot D_{by2} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) e^{j\frac{k_y \Delta y}{2}} \end{pmatrix} & 0 & 0 \\ -2j \cdot D_{by,1} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) & -2j \cdot D_{by,1} \cdot \sin\left(\frac{k_y \Delta y}{2}\right) & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
P_2 &= \begin{bmatrix} C_{ax} & 0 & 0 & -2j \cdot C_{bx} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) \\ 0 & C_{ay} & C_{by} \cdot \begin{pmatrix} D_{ay1} \cdot e^{-j\frac{k_y \Delta y}{2}} \\ -D_{ay2} \cdot e^{j\frac{k_y \Delta y}{2}} \end{pmatrix} & 0 \\ 0 & 0 & D_{ay,1} & 0 \\ -2j \cdot D_{bx,1} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) & -2j \cdot D_{bx,1} \cdot \sin\left(\frac{k_x \Delta x}{2}\right) & 0 & D_{ax,1} \end{bmatrix}
\end{aligned}$$

Combing the two half time steps can lead to one time step

$$X^{n+1} = M_2^{-1} P_2 M_1^{-1} P_1 X^n = \Lambda X^n \quad (3)$$

As the electric conductivity σ and magnetic conductivity σ^* within the PML are usually scaled for small reflection, the PML parameters σ and σ^* will be position-dependent. Stability requires that the eigenvalues of Λ lie within or on the unit circle, that is, $|\lambda_\Lambda| \leq 1$. It has been shown in [6, 7] that when the Berenger's PML are used for the ADI-FDTD method, this scheme will lead to late-time instability.

As shown in [8], it is found that the PML conductivity profile will affect the stability of this scheme. Two conditions are proposed to improve the stability inside the PML regions. For the first condition, the electric and magnetic conductivities inside the PML regions should be large enough. For the second condition, the ratio of the successive magnetic conductivity should be small. In the conventional PML conductivity profile, the PML parameters are chosen the same as those in [5]. The conductivity profile of the PML is scaled using polynomial scaling and is expressed as

$$\sigma_{s_{\max}} = \sigma_{opt} \approx \frac{(m+1)}{150\pi\Delta s}$$

$$\sigma_s(s) = \frac{\sigma_{s_{\max}} |s-s_0|^m}{d^m} \quad S=x, y, z \quad (4)$$

where d is the thickness of PML absorber, Δs is the cell size, and s_0 represents the interface. The PML conductivity is increased from the PML interface to the PEC boundary. Based on the study in [8], the larger electric conductivity and smaller scaling factor m are used for the modified conductivity profile to improve the instability of this scheme.

The performance of the PML will be affected by the modified conductivity profile. Although this scheme can be more stable inside the PML regions with the modified conductivity profile, the PML performance with the conventional conductivity profile is better than that with the modified PML conductivity profile. Therefore, there is the trade-off on the stability of this scheme and the PML performance. To avoid the instability of this scheme, the maximum time step size, the total number of time steps, and the desired PML performance should be considered when choosing the scaling factor m and the maximum electric conductivity σ_{\max} for the modified conductivity profile.

3. NUMERICAL SIMULATION

The time step size of the ADI-FDTD method is not restricted by the CFL stability condition, but by the required numerical dispersion of this method. One of the factors that affect the numerical dispersion is the grid size. When using the ADI-FDTD method for VLSI circuits modeling, the grid cell size will be micron-scale, which is much smaller than 1/10th or 1/20th of the smallest wavelength of interest. Therefore, the ADI-FDTD is well suited for VLSI circuits modeling as the numerical error of scheme can be small even large time step size is used. In this section, numerical simulations of the VLSI circuits including the multilevel crossover and RF inductor by ADI-FDTD method are demonstrated.

3.1. Multilevel Crossover in VLSI Interconnects

The coupling effect of the multilevel crossover in VLSI circuit is analyzed. The structure is taken from [9] and is shown in

Figure 1. The two-level crossover has two conductors in each level. The conductors are of copper with width $1 \mu\text{m}$ and thickness $1 \mu\text{m}$, respectively. The five SiO_2 layers are of thickness $1 \mu\text{m}$ and $\epsilon_r = 3.9$ and covered by two ground conductors on the top and bottom. The line lengths and separations are 30.8 and $1 \mu\text{m}$, respectively.

In the ADI-FDTD modeling, the computational domain is meshed with cell sizes $\Delta x = \Delta y = \Delta z = 0.2 \mu\text{m}$. The maximum time step size for CFL condition is 0.38 fs. The PML medium with 10 layers is used to truncate the computational domain. The total computational domain is $174 \times 174 \times 45$. For the ADI-FDTD simulation, the CFLN = 10 and CFLN = 20 are used and the corresponding time step size are 3.8 and 7.6 fs, respectively.

The simulation results are shown in Figure 2. First, the conventional ADI-FDTD with Berenger's PML is studied. As shown in Figure 2(a), it can be found that the numerical results will become unstable after running 4800 time step. Using the modified PML conductivity profile with $m = 1.5$ and $\sigma_{\max} = 21.22$ S/m for this scheme, the instability of this scheme can be improved, as shown in Figure 2(b). We have also extended the running time to 10,000 time steps and no instability is observed.

The coupling effect of the multilevel crossover is investigated by using the ADI-FDTD method with modified PML conductivity profile. The excitation pulse is trapezoidal with rise time and fall time $\tau_r = \tau_f = 380$ fs and on-time $\tau_{on} = 380$ fs. The simulation result is shown in Figure 3. The numerical result

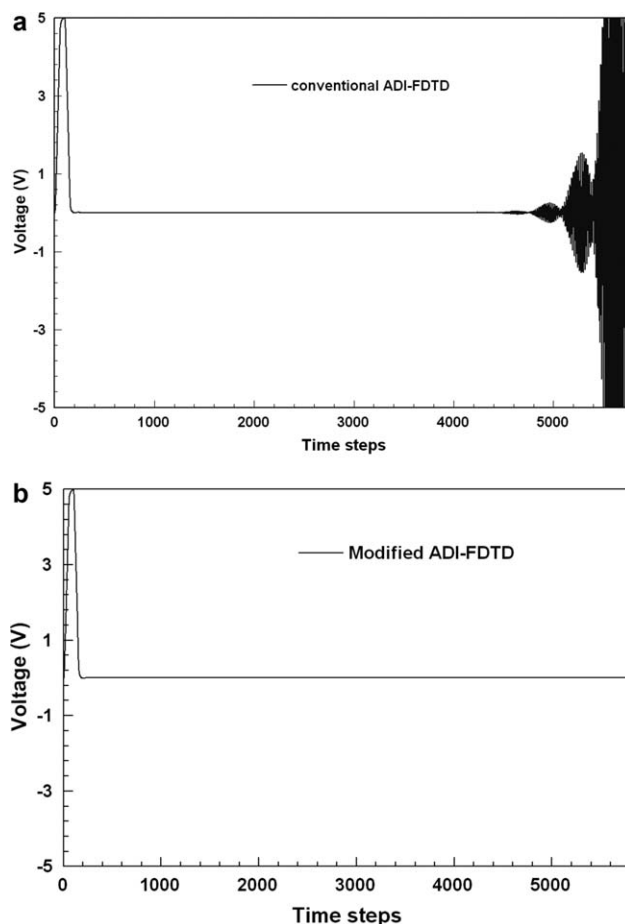


Figure 2 (a) Voltage at Port 1 with the conventional PML conductivity profile. (b) Voltage at Port 1 with the modified conductivity profile

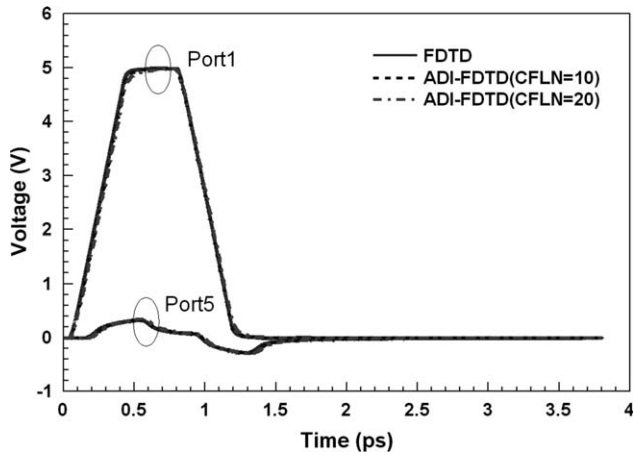


Figure 3 Voltages at different ports of the multilevel crossover

TABLE 1 Multilevel Crossover Simulation

	Δt (fs)	Steps	CPU Time Ratio
FDTD	0.38	10,000	1.000
ADI-FDTD ($10\Delta t_{\max}$)	3.8	1000	0.561
ADI-FDTD ($20\Delta t_{\max}$)	7.6	500	0.269

of the ADI-FDTD method is similar to that of the FDTD method even CFLN = 20. It is found that there is considerable coupling between the lines in the same level and different levels. The coupled signal amplitudes are near 10% of that of the incident pulse. This shows good match between our result and the result in [9].

The time step size, total time steps, and the CPU time ratio are shown in Table 1. As the time step size is set 10 and 20 times as larger as that of the FDTD method, the total time steps can be reduced. The require memory for the ADI-FDTD method is about 1.9 times as large as that for the conventional FDTD method because of the extra electromagnetic components for two updating steps. Compared to the FDTD method, the CPU time can be reduced to 56.1 and 26.9% for CFLN = 10 and CFLN = 20, respectively.

3.2. RF Inductor

Simulations of the VLSI circuit by ADI-FDTD method are performed. A five-turn spiral inductor [10] is studied by the ADI-FDTD method. A cross-sectional view of a portion of the structure is illustrated in Figure 4. The outer dimension is 250 μm , the top conductor microstrip is 8 μm wide, and the spacing between conductors is 2.8 μm . The inner space between coupled lines is 150 μm .

For single-ended excitation, Port 2 is grounded. The frequency domain characteristic of the RF inductor can be obtained from the Fourier transform of the time domain transient waveform. The quality factor of the inductor is defined by

$$Q = \frac{2\pi fL}{\text{Re}[Z_{\text{input}}]} \quad (5)$$

where Z_{input} is the series equivalent input impedance.

In the ADI-FDTD simulation, the cell sizes in the x - and y -directions are $\Delta x = \Delta y = 1.35 \mu\text{m}$. We use the nonuniform cells in the z -direction to reduce the computational domain and model the fine geometry. The nonuniform cell sizes in z -direction are 3.0, 1.5, and 1.2 μm , respectively. The CFL stability condition is $\Delta t_{\max} 2.5$ fs. We choose CFLN = 20 and the corresponding time step size $\Delta t = 50$ fs.

As we will study the Q -factor in frequency domain, the total number of the time steps for ADI-FDTD simulation is around 25,000 time steps when CFLN = 20 is used. If the conventional FDTD method is used to analyze this inductor, the total time steps will be and it will be difficult to complete the simulation. When the conventional PML conductivity profile is used for ADI-FDTD method, the numerical results will be unstable after running 1000 time steps. In Section 2, we find that the ratio of the successive magnetic conductivity should be small to prevent the instability. To validate this viewpoint, the homogeneous PML medium $\sigma_x = \sigma_y = \sigma_{\max}$ is used for the ADI-FDTD to analyze the spiral inductor. The simulation result shows that no instability is observed after running 25,000 time steps and the time-domain waveforms are Fourier transformed to obtain the frequency domain result. Comparisons between the experimental measurement and simulation result for Q -factor are shown in Figure 5. At frequencies below 2.5 GHz, the simulation results of the Q -factor between measurement and simulation result are matched well. From the measurement result, the peak Q -factor

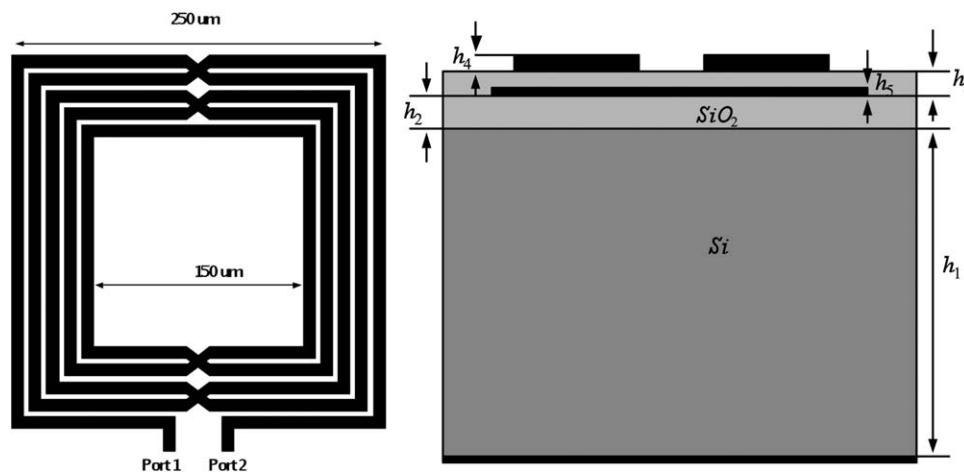


Figure 4 Cross-section view and layout of the spiral inductor with h_3 – $h_5 = 1.3 \mu\text{m}$, $h_2 = 3.6 \mu\text{m}$, $h_1 = 200 \mu\text{m}$, $h_4 = 2.07 \mu\text{m}$, and $h_5 = 0.84 \mu\text{m}$

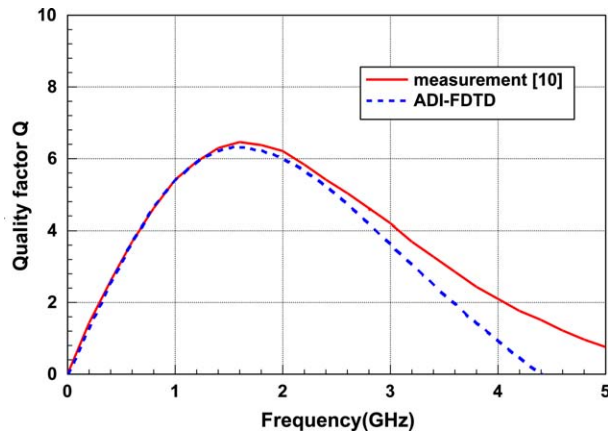


Figure 5 Measured and simulated Q -factor. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

is 6.6 at 1.6 GHz. Our simulation shows that the peak Q is 6.3 at 1.6 GHz, which is similar to the measurement result.

4. CONCLUSION

The ADI-FDTD can be used for efficient and stable electromagnetic modeling of the VLSI circuit as the time step is not restricted by the CFL stability condition. However, when the Berenger's PML is implemented in the ADI-FDTD method, this scheme will lead to late-time instability. In this article, we propose the modified PML conductivity profile to improve the stability of the ADI-FDTD with PML absorber. The multilevel crossover in VLSI circuit and RF inductor are studied. Compared to the conventional FDTD simulation, a significant reduction in calculation time can be achieved. Although the PML performance will be affected by the modified PML conductivity profile, it can be found that the simulation results are matched quite well with the reference results. The modified scheme can provide an efficient and accurate electromagnetic simulation method for VLSI circuits.

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COMPACT LOWPASS FILTER WITH A SHARP ROLL-OFF USING PATCH RESONATORS

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ABSTRACT: This article presents a new compact microstrip lowpass filter with sharp roll-off and ultrawide stopband using funnel and triangular patch resonators. The patch resonators are placed symmetrically about a high impedance central microstrip line. The filter has been designed and fabricated using a very low cost material. The experimental results show a good agreement with the simulated results and demonstrate that, the sharp roll-off and good stopband performance is obtained by the proposed filter. The 3 dB cutoff frequency of the proposed filter is at 5.55 GHz with a roll-off of 84 dB/GHz and its stopband extends up to 11.8 GHz. The filter has an ultra compact size of $9.4 \times 8 \text{ mm}^2$. © 2014 Wiley Periodicals, Inc. *Microwave Opt Technol Lett* 56:2534–2536, 2014; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.28644

Key words: funnel patch resonator; lowpass filter; microstrip line; transmission zero; triangular patch resonator

1. INTRODUCTION

High performance and compact lowpass filters are in great demand for present communication systems to suppress harmonics and spurious signals. Microstrip filters offer low insertion loss in the passband and infinite attenuation in the stopband together with compact size, low cost, and ease of fabrication. Filtering of undesired frequencies using microstrip can be accomplished with conventional design techniques, such as stepped impedance lines or tuned stubs. However, these filter structures require large layout area to obtain sharp frequency characteristics [1]. Compactness and sharp roll-off will be obtained by introducing defective ground structure, which also exhibits wide harmonic suppression and slow-wave characteristics [2–4]. But these filters cannot be fixed on a metal base due to the inherent defects in the ground plane. Various methods have been proposed to develop a high performance, compact microstrip lowpass filters by cascading multiple resonators. A microstrip lowpass filter using the stepped impedance hairpin resonator was reported in [5]. Even though the size reduction was achieved in this configuration, the response is not sharp. Good stopband performance was achieved by multiple resonators and meander transmission line [6, 7], the filter passband was too narrow and its transition characteristics were very poor. By introducing in-line beeline CMRC, a lowpass filter featured with a wide stopband was proposed in [8], but it is hard to achieve sharp roll-off and good passband characteristics. Multiple stub-loaded tapered microstrip resonator cells was also used to create lowpass filter with good in-band and out-of-band performance as in [9], but it requires relatively large layout area. More over the above mentioned filters are designed using high cost substrate.