Interface Engineering for High-Performance Top-Gated MoS₂ Field-Effect Transistors

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In recent years, due to the intriguing electrical and optical characteristics, two dimensional (2D) layered transition metal dichalcogenides such as molybdenum disulfide (MoS_2) have attracted tremendous research attention.[1–7] Similar to their well-known cousin, graphene, MoS_2 exhibits many excellent properties including the superior mechanical flexibility, impressive thermal stability, absence of dangling bonds and compatibility to silicon CMOS processes.[1,8–10] More importantly, in a distinct contrast to the bandgap issue of graphene,[11] MoS_2 is semiconducting with a satisfied thickness-dependent bandgap of 1.2 to 1.8 eV,[7,12] which can enable lots of fascinating device applications in field-effect transistors (FETs) with the extraordinary on/off current ratio ($>10^8$),[1,13,14] nonvolatile memory devices,[15–17] ultrasensitive photodetectors,[18–20] integrated circuits and logic operation,[21,22] etc. All these have elucidated the promising nature of MoS_2 being the ideal alternative channel material for thin-film transistors (TFTs) for the continued device scaling beyond Moore's Law.[4,8,23,24]

However, until now, majority of the efforts have been focused on the integration of MoS_2 devices in the back- or dual-gated geometry due to the difficulty of compact and conformal top-gated dielectric deposition directly onto the 2D channel for the realization of high-performance top-gated FETs.[25] In order to integration in TFT circuit for practical application, top-gated MoS_2 FETs with high-*k* dielectric is necessary. First, back- or dual-gated FET is not compatible with integrated circuit technology as it cannot individually tune each device like a top-gate. Second, to decrease the operation voltage and permit further device scaling, it is expected that the gate dielectric layers in future devices will be much thinner and have higher values of dielectric constant *k*. Moreover, top-gated configurations are essential to suppress coulomb scattering in MoS_2 channels for the low-power device operation with the enhanced gate coupling, carrier mobility and saturated current.[1,26,27] Although uniform films of high-*k* dielectric in the thickness of sub-10 nm have been well-established in atomic layer deposition (ALD) and fully reported in the literature,[28–30] conformal deposition of dielectrics on MoS_2 remains challenging since there is not sufficient dangling bond or nucleation site on the 2D channel for the initiation of uniform dielectric deposition. It is observed that the island type growth of dielectrics (e.g., HfO_2) results in these non-uniform films on MoS_2 in which the lack of observable covalent bonding at the dielectric/channel interface would induce a substantial leakage owing to the high activation energy for the dissociative reaction between HfO_2 and MoS_2.[25] There are few reports regarding aggressive scaling of dielectric thicknesses for MoS_2 FETs, probably due to the difficulty in achieving pinhole-free, thin dielectrics over a large area. In this regard, interface or dielectric engineering is an important step towards the practical implementation of MoS_2 devices with the optimized performance.

In general, there are limited studies performed to improve the coverage of high-quality ALD dielectrics on MoS_2 channels. For example, surface functionalization of MoS_2 channels with oxygen plasma or ultraviolet ozone is recently demonstrated to promote the reactivity of MoS_2 with ALD precursors, but the energetic oxygen species may inevitably damage the 2D channels inducing defects to deteriorate their corresponding electrical properties.[31–33] In this work, we explore the case of interface engineering further by utilizing an ultrathin metal oxide (MgO, Al_2O_3 and Y_2O_3) buffer layer inserted between the ALD-HfO_2 and MoS_2 channel in order to achieve conformal HfO_2/MoS_2 interfaces with the minimal interface defect density down to $(2.3 \pm 0.8) \times 10^{12}$ cm^{-2}eV^{-1}. Exploiting these enhanced gate stack dielectrics, we attain the highest saturation current (526 μA/μm) of any MoS_2 transistor reported to date, which is comparable to the same scaled state-of-the-art Si MOSFETs.

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At the same time, these devices also exhibit the impressive room-temperature mobility (63.7 cm^2/V·s), on/off current ratio (> 10^8) and near-ideal sub-threshold slope (SS = 65 mV/decade). Notably, the versatility of this interface engineering technique is further illustrated with the construction of high-performance MoS$_2$ integrated circuits such as inverters with a large voltage gain of 16, making them attractive for the incorporation into digital components. Demonstration of all these suggests that the performance of few-layer MoS$_2$ FETs can reach near intrinsic limits at room temperature along with the proper interface engineering and propose future directions to improve electrical characteristics in layered semiconductors.

Few-layer MoS$_2$ are exfoliated from commercially available crystals of molybdenite utilizing the scotch-tape technique[34,35] and transferred onto p$^+$-Si wafers covered with a 300 nm thick SiO$_2$. Here, 3–5 layers MoS$_2$ are employed to obtain high current and mobility, meanwhile, avoiding degradation in on/off ratio or sub-threshold slope (SS).[36] Prior to the HfO$_2$ growth by ALD, an ultrathin metal buffer layer with the nominal thickness of 1 nm is deposited on the MoS$_2$ surface by thermal evaporation. Then the devices are placed in a drying oven for several hours to be naturally oxidized, which is confirmed by the spectra analysis of X-ray photoelectron spectroscopy (Figure S1). After the buffer layer process, the samples are taken out and transferred into the ALD chamber for the deposition of HfO$_2$. The structural schematic is shown in **Figure 1**a. Figure 1b-e give Atomic Force Microscopy (AFM) images of the MoS$_2$ surface after 20 ALD cycles using precursors of tetrakis(dimethylamino)hafnium and water at 95 °C. It is noted that a relatively low deposition temperature of 95 °C is employed here to minimize the coalescence of buffer layer which would degrade the subsequent device performance. As predicted, the HfO$_2$ layer directly deposited on the bare MoS$_2$

exhibits the formation of pinhole-like defects and the resulted film is not continuous and compact (Figure 1b). This phenomenon has been understood in the way as there are no out-of-plane covalent functional groups for the initiation of the ALD reaction. The HfO$_2$/MgO/MoS$_2$ stack also presents large amount of pinholes, which can be attributed to numerous gaps existing among large MgO particles such that conformal HfO$_2$ deposition is hardly achieved (Figure 1c). In contrast, very few pinholes are observed for the HfO$_2$/Al$_2$O$_3$/MoS$_2$ and HfO$_2$/Y$_2$O$_3$/MoS$_2$ stacks, indicating the importance of proper buffer layer materials (Figure 1d-e). Specifically, since Y has the highest melting point among all the buffer materials here, Y is believed to behave less sensitive to the coalescence at the ALD process temperature; therefore, the HfO$_2$ layer deposited with the Y$_2$O$_3$ buffer layer gives the least amount of pinholes and results a conformal ultrathin film suitable for the gate dielectric. Importantly, as depicted in Figure 1f, there is no obvious change in Raman spectra among all structures, indicating that the HfO$_2$/Y$_2$O$_3$/MoS$_2$ stack fabricated in the present interface engineering approach does not introduce any noticeable lattice damage or bond-disorder into MoS$_2$ channels.

FETs based on few-layer MoS$_2$ are then fabricated with the architecture illustrated in **Figure 2**a lower inset. After MoS$_2$ flakes are mechanically exfoliated and transferred on the substrates, electrical contacts of Cr/Au (5/50 nm) are patterned on top of MoS$_2$ channels by thermal evaporation. After forming the contact electrodes, a 28 nm thick HfO$_2$ film is deposited onto the MoS$_2$, pre-deposited with the appropriate buffer layer, as the top-gated dielectrics by ALD. The top-gated electrode (50 nm thick Au) is subsequently completed. Scanning electron microscopic (SEM) image of a representative device is shown in Figure 2a upper inset. In order to investigate the fundamental device performance, the MoS$_2$ FETs are fabricated with
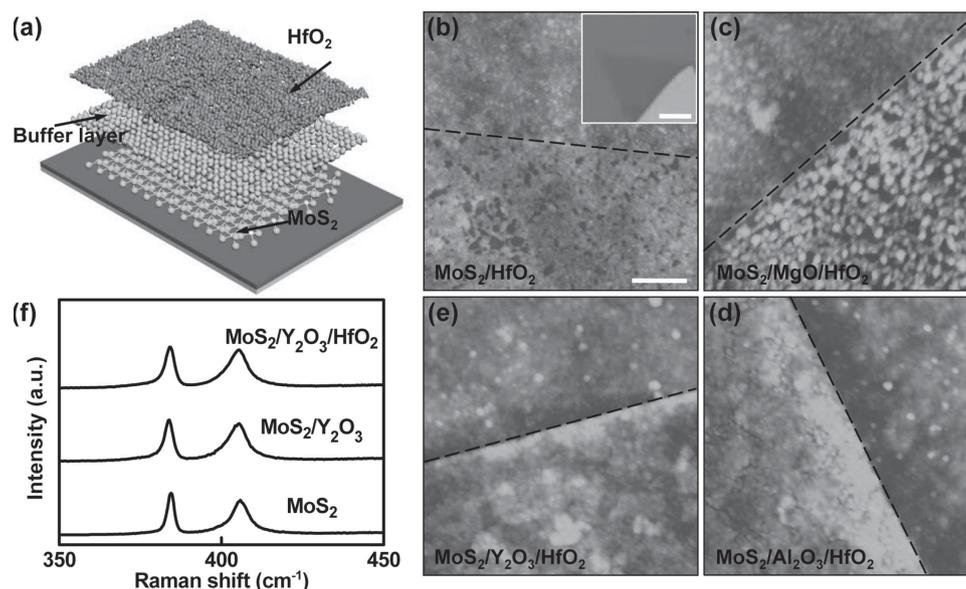

Figure 1. Schematic, surface morphology and structural properties of few-layer MoS$_2$ with the interface engineering. (a) Structural schematic of few-layer MoS$_2$ covered with the metal oxide buffer layer and HfO$_2$ film. (b-e) AFM images of MoS$_2$ surface after 20 ALD cycles of HfO$_2$ deposition with and without the metal oxide buffer layer. The dash line designates the boundary between MoS$_2$ and underlying SiO$_2$. Scale bar is 100 nm. Inset is the corresponding optical image of a few-layer MoS$_2$ flake used for the HfO$_2$ deposition. Scale bar is 5 µm. (f) Raman spectra of a few-layer MoS$_2$ flake before and after Y$_2$O$_3$ buffer layer deposition, followed by the HfO$_2$ growth.
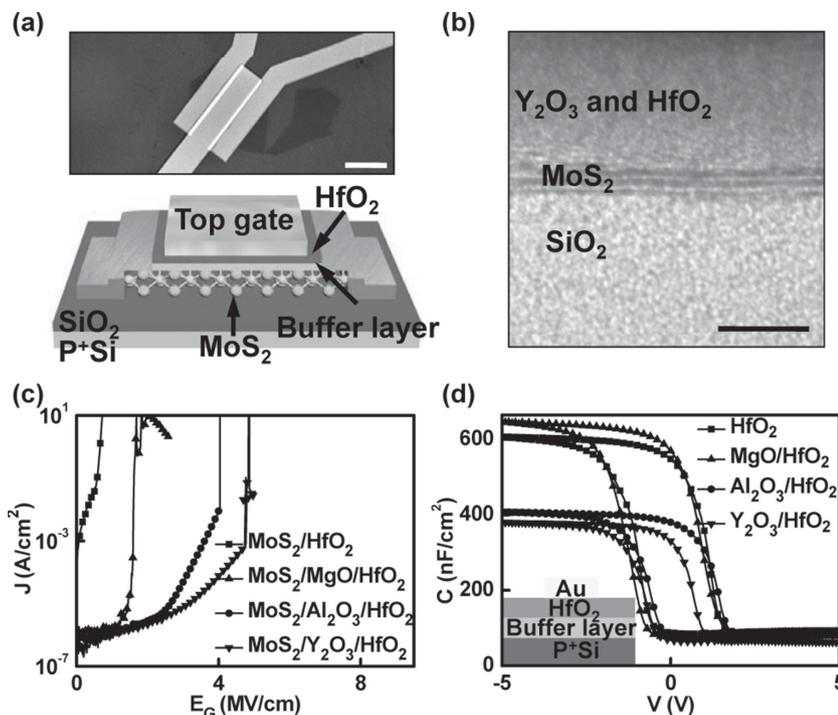
Figure 2. Fabrication of few-layer top-gated MoS_2 FETs and corresponding dielectric properties. (a) Illustrative schematic of the top-gated MoS_2 FETs (lower inset) and SEM image of a representative device (upper inset). Scale bar is 5 μm. The complete gate to source or drain overlapping is used to minimize the parasitic resistance. (b) Cross-sectional HRTEM image of the interface between MoS_2 and HfO_2 dielectric. Scale bar is 5 nm. (c) The leakage current density (J) curves for top-gated devices with different gate structures. (d) CV curves of HfO_2 based capacitors at 1MHz with different metal oxide buffer layers. Inset is the structural schematic of the capacitors.

the complete gate to source or drain overlapping in order to minimize the parasitic resistance.[37] The cross-sectional high-resolution transmission electron microscopic (HRTEM) image of $HfO_2/Y_2O_3/MoS_2$ stack is presented in Figure 2b, which exhibits a uniform and compact interface between MoS_2 and HfO_2 without any significant gap and defects. Also, there is not any obvious Y_2O_3/HfO_2 boundary observed, which is possibly due to the solid solution formation induced by the atomic inter-diffusion at the Y_2O_3/HfO_2 interface. Further measurement of the hard breakdown characteristic is performed to evaluate the electrical reliability of the device (Figure 2c). As compared with the MoS_2/HfO_2 stack, HfO_2 deposited with metal oxide buffer layers exhibit a substantial improvement in breakdown field (E_G). In specific, with the MgO, Al_2O_3 or Y_2O_3 buffer layer, the E_G value increases from 0.2 MV/cm (MoS_2/HfO_2 stack) to 4.8 MV/cm ($MoS_2/Y_2O_3/HfO_2$ stack). This observation can be attributed to the difference in the trap-assisted current through defects in the HfO_2 layer.[38] It simply means that with the help of Y_2O_3 buffer layer, $MoS_2/Y_2O_3/HfO_2$ stack is the most compact with minimal defect density.

In order to extract the dielectric constant for HfO_2 deposited at such low temperature (95 °C) and investigate the corresponding device performance, capacitors are fabricated by depositing 28 nm thick HfO_2 on p$^+$-Si substrates with and without metal oxide buffer layers, respectively, with the illustration as shown in Figure 2d inset. Based on the capacitance

versus voltage (CV) curves of HfO_2 without the buffer layer (Figure 2d), a high dielectric constant of 19 can be extracted, indicating the extremely optimized ALD condition. The reduction of capacitance deposited with Y_2O_3 and Al_2O_3 buffer layers can be associated with the series connection of capacitors. However, the MgO buffer layer based HfO_2 yields the largest capacitance, even larger than the one of pristine HfO_2. A possible reason is that the coalesced MgO particles increase the upper and lower surface area of HfO_2 which would affect the resulting capacitance. (Figure S2). Additionally, although the nominal Y thickness is 1 nm, the real Y thickness may be 2–4 nm and the corresponding Y_2O_3 thickness may be 3–7 nm (Figure S3).

Next, the fabricated top-gated MoS_2 FETs are electrically characterized at room temperature. In this study, a total of 90 devices are constructed to shed light on the electrical properties with different metal oxide buffer layers (MgO, Al_2O_3 or Y_2O_3) statistically. All devices are measured at a fixed condition including temperature, humidity and V_{gs} sweep rate in order to minimize the disturbance of uncertainty random circumstance factors. **Figure 3**a-c show typical transfer characteristics of top-gated MoS_2 FETs which represent the highest field-effect mobility (μ_{FE}) among each type of devices. The hysteresis characteristic is shown in Figure S4. All fabricated devices exhibit clearly n-type conduction and transistor behavior, being consistent with the previous reports. Importantly, the transfer characteristics demonstrate the ability to modulate the resistance of the MoS_2 channel by changing the top-gated voltage, yielding an on/off current ratio exceeding 10^8. In detail, μ_{FE} is estimated using the equation:

$$\mu_{FE} = \frac{g_m L_{ch}}{W C_i V_{ds}} \tag{1}$$

in the linear operation regime. Here $g_m = dI_{ds}/dV_{gs}$ is the transconductance and $L_{ch} = 3$ μm is the device channel length. C_i is the unit-area capacitance of the top gate which is given in Figure 2d. Using the approximate capacitance values and measured device parameters, a high mobility value (63.7 cm^2/V·s) based on the Y_2O_3 buffer layer is obtained. Although the back-gate measurement of our devices gives much higher mobility values of 500 to 1000 cm^2/V·s, these values may be greatly over-estimated due to the capacitive coupling between the top- and back-gates.[39,40] At the same time, Figure 3d-f depict the output characteristics recorded from the same devices, illustrating that I_{ds} increases linearly with V_{ds} at low V_{ds} and saturates at high V_{ds}. The linear regime can be attributed to the good ohmic contacts between the Cr/Au electrodes and the MoS_2. The pinch-off and I_{ds} saturation suggest that the carrier transport is completely controlled by the top-gated bias. The corresponding
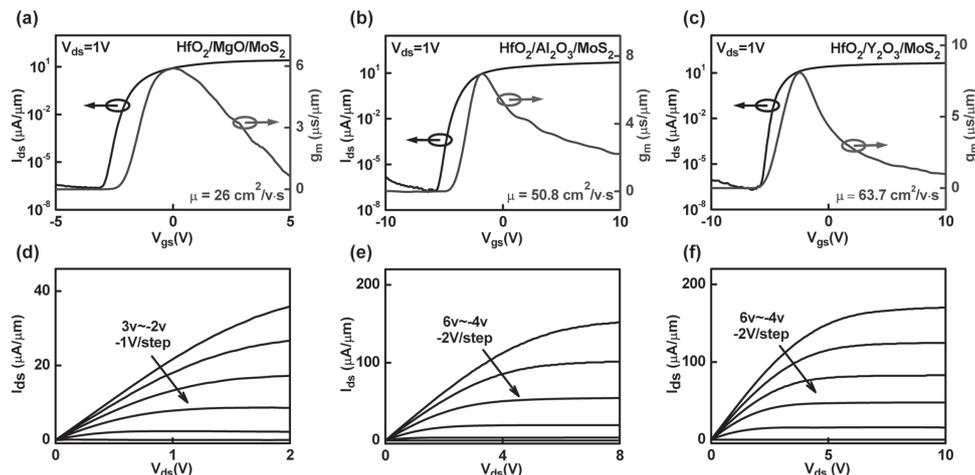
Figure 3. Electron transport in top-gated few-layer MoS$_2$ FETs. (a-c) Transfer characteristics of the typical top-gated MoS$_2$ FETs using different metal oxide buffer layers (MgO, Al$_2$O$_3$, and Y$_2$O$_3$). (d-f) Output characteristics of the same devices. Drain voltage is applied carefully to avoid breakdown of the devices. The MoS$_2$/Y$_2$O$_3$/HfO$_2$ stack shows the excellent current saturation, which is extremely important for both digital and analog circuits.

gate leakage curves are shown in Figure S5. Notably, the device with Y$_2$O$_3$ buffer layer shows more advantages in the current saturation due to the higher drain voltage which is limited by the breakdown voltage; this result together with good stability under negative bias stress (Figure S6), indicating that MoS$_2$/Y$_2$O$_3$/HfO$_2$ stack is more suitable for TFT applications.

Moreover, in view of the performance variance associating with the non-uniformity of MoS$_2$ thickness as well as the device fabrication, a statistical study of the key parameter of devices is necessary in order to gain a comprehensive understanding of the electrical properties. **Figure 4**a-c show the distributions of μ_{FE} with different buffer layers. All the values are extracted at 1 V drain bias and 3 µm channel length. A total of 30 devices are studied for each type of devices. The average and standard deviation of the calculated mobility are 15.9 ± 7.2, 37.4 ± 11.4 and 47.7 ± 11.9 cm^2/V·s for the devices using MgO, Al$_2$O$_3$ or Y$_2$O$_3$ buffer layers, respectively. The difference in mobility can be connected to the interface properties between MoS$_2$
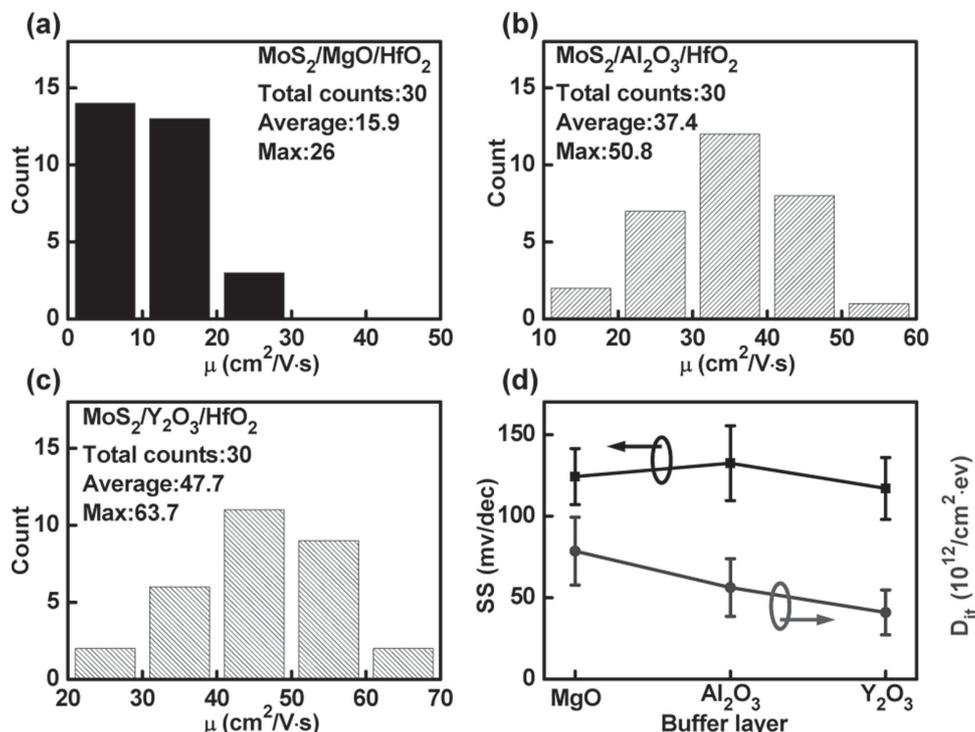

Figure 4. Statistical studies on electrical properties for top-gated few-layer MoS$_2$ FETs. (a-c) Field-effect mobility distributions of top-gated MoS$_2$ FETs deposited with different buffer layers. Average mobility values of 15.9 ± 7.2, 37.4 ± 11.4 and 47.7 ± 11.9 cm^2/V·s for MgO, Al$_2$O$_3$ and Y$_2$O$_3$ buffer layers are acquired, respectively. (d) The average values of SS and D_{it} extracted from 30 devices for each type.
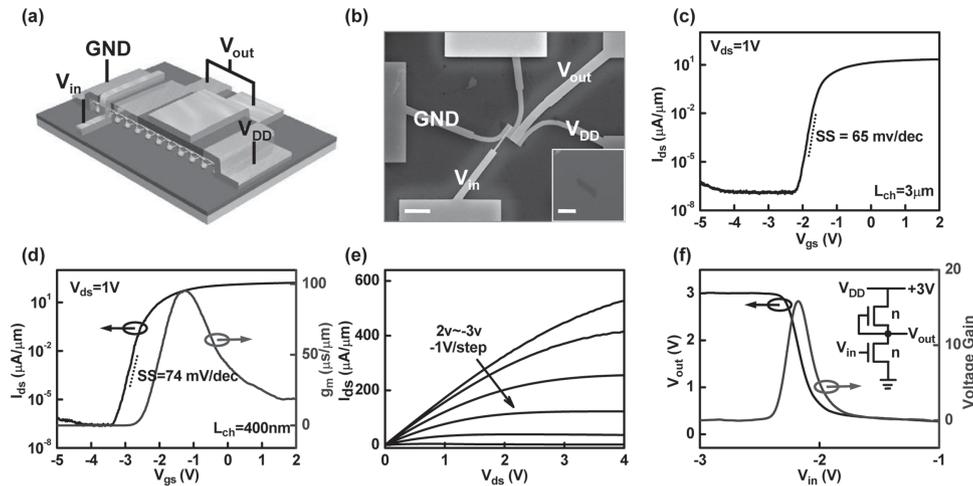
Figure 5. Integrated circuits based on top-gated few-layer MoS_2 FETs with the 9 nm thick HfO_2 dielectric. (a) Structural schematic of the integrated MoS_2 inverter together with electrical connections used to characterize the device. The inverter is composed of two transistors with different channel length, 400 nm and 3 μm. (b) SEM image of the device. Here, complete overlapping gate to source or drain and long contact length of 2 μm are employed to minimize the parasitic and contact resistance. Inset shows the optical image of a few-layer MoS_2 used to fabricate the device. (c-d) Transfer characteristics of 400 nm and 3 μm MoS_2 transistors. The *SS* value is improved to 65 mv/dec and 74 mv/dec respectively, indicating the excellent interface quality and scalability. (e) Output characteristics of the 400 nm MoS_2 transistor with a record current density of 526 μA/μm achieved. (f) Voltage gain of the inverter. At V_{DD} = 3 V, the peak voltage gain of the inverter is about 16. Inset gives the schematic drawing of the equivalent electronic circuit.

and HfO_2 dielectric layer. In this case, interface trap density (D_{it}) is employed to evaluate the interface quality using the equation:[1,41,42]

$$D_{it} = \frac{C_i}{q}\left(\frac{q \cdot SS}{KT \ln 10} - 1\right) \tag{2}$$

Here, q is the electron charge and T (300 K) is the measurement temperature. Calculating the density of interface traps, one obtains the lowest value of $(2.3 \pm 0.8) \times 10^{12}$ $cm^{-2}eV^{-1}$ for the $MoS_2/Y_2O_3/HfO_2$ stack (Figure 4d). This value is similar to the one reported for the optimized $Al/HfO_2/SiO_2/Si$ capacitors,[43,44] which indicates an excellent interface quality between MoS_2 and HfO_2 employing our interface engineering of the Y_2O_3 buffer layer. This is probably due to the good wetting between Y and MoS_2,[45] which lead to a uniform, compact and pinhole-free $MoS_2/Y_2O_3/HfO_2$ stack. In addition, as metal thin film is known to possess a lower melting point than the bulk material, which is expected to form island easily on MoS_2 surface, in this case, as compared to Mg and Al, Y has the advantage in much higher melting point such that leading to a fully conformal film in this study.

However, the thick dielectric leads to a poor gate control over the driving current, resulting in poor *SS* value (over 100 mV/dec), high operating voltage and high threshold voltage. Here, utilizing the above interface engineering of $MoS_2/Y_2O_3/HfO_2$ stack, HfO_2 dielectric thickness is further reduced down to 9 nm which has an enhanced gate capacitance of 780 nF/cm². As compared with the 28 nm thick HfO_2 layer, a higher breakdown field of 7 MV/cm is achieved here and this can be simply explained with the series capacitor model. Meanwhile, there is not any obvious change in the leakage current, indicating the high quality of HfO_2 dielectric layer (Figure S7). Our integrated circuit, a fully integrated inverter,

is composed of two n-type transistors realized on the same few-layer MoS_2, as depicted in **Figure 5**a-b. The channel length is 3 μm and 400 nm, respectively. In order to obtain higher output current and transconductance, complete overlapping gate to source or drain and long contact length of 2 μm (length of source/drain) are employed to minimize parasitic and contact resistance.[46,47] Utilizing this configuration, the smallest contact resistance is measured to be 0.33 ± 0.04 Ω·cm at V_{gs}–V_t = 3 V, where V_t represents the threshold voltage (Figure S8), Due to the higher gate control, all devices show a dramatic improvement in SS (65 mv/dec for L_{ch} = 3 μm and 74 mV/dec for L_{ch} = 400 nm) which is close to the theoretical limit (Figure 5c-d). Meanwhile, as L_{ch} is reduced to 400 nm, more improvements in electrical properties are acquired, including high saturation current of 526 μA/μm and large g_m of 94 μS/μm at V_{ds} = 1 V (Figure 5e). To the best of our knowledge, these are the highest values reported for any MoS_2 FETs so far.

Another important parameter, saturation velocity (V_{sat}) which is closely related to the maximum drain current achievable, is also discussed here. In general, the saturation velocity is determined by the charge carrier transit time (τ) across the channel length. It can be calculated by this equation:[48]

$$V_{sat} = \frac{L_{ch}}{\tau} = \frac{L_{ch}g_{sat}}{C_g} \tag{3}$$

Here, g_{sat} is the max transconductance as the device is operated in saturation regime. Based on this equation, the calculated V_{sat} value is about 2.1×10^6 cm/s, similar to the carrier saturation velocity reported in previous studies.[49] This value, together with high on/off ratio ($>10^8$), enable it with the great potency for high-speed thin film transistors with the low power consumption.

COMMUNICATION

We then further proceed by demonstrating that our few-layer MoS_2 integrated circuits can operate as the most basic logic gate, a logic inverter, which can output a voltage representing the opposite logic level to its input. The quality of a logic inverter is often evaluated through its ability in the voltage gain, which is defined as $gain = -dV_{out}/dV_{in}$ where V_{out} is output voltage and V_{in} is input voltage. During the test process, input voltage V_{in} is applied to the local gate of the switch transistor while the supply voltage $V_{DD} = 3\ V$ is applied to the drain electrode. In the circuit shown in Figure 5b, a large voltage gain close of 16 is achieved (Figure 5f), indicating the attractiveness of this device for the integration of logic gate arrays.

In summary, this letter provides the experimental evidence of the effects of optimized interface engineering in MoS_2 transistors. Utilizing the $MoS_2/Y_2O_3/HfO_2$ stack, the fabricated device exhibits high electron mobility of 63.7 $cm^2/V\cdot s$ and large on/off current ratio exceeding 10^8. By further scaling down the HfO_2 dielectric to 9 nm, a near-ideal sub-threshold slope (65 mV/dec) is achieved, indicating the excellent interface quality and scalability. As the channel length is reduced to 400 nm, the device shows the highest saturation current of 526 μA/μm, which is the best value reported for any MoS_2 devices to date. In addition, we also construct and demonstrate the performance of a basic logic device, an inverter, achieving a large voltage gain of 16. Although the saturation current and mobility measured with the $MoS_2/Y_2O_3/HfO_2$ stack already exceeds most competing semiconductor materials for large-area TFTs by orders of magnitude, the values can be further improved by more appropriate dielectric choices. The interface engineering allows the integration of top-gated MoS_2 transistors with impressive performance, and thus opens the roadmap for practical applications in MoS_2 TFT integrated circuits.

Experimental Section

ALD Growth of HfO_2: ALD of HfO_2 on the contacted MoS_2 flake is performed at 95 °C using KE-MICRO TALD-200A system. The TDMAH precursor source is heated to 90 °C while the H_2O source is kept at room temperature. The carrier and purge gas is high purity Ar with a flow rate of 33 sccm. The pulse time for TDMAH and H_2O are 0.04 and 0.022 s, respectively. The post TDMAH pulse purge is with Ar for 120 s and the post H_2O purge with Ar for 100 s. The results in a growth rate of 1.4 Å/cycle.

Device Fabrication and Measurements: Few-layer MoS_2 flakes are mechanically exfoliated from bulk MoS_2 crystals and transferred to the pre-cleaned highly doped p-type silicon substrates with a thermally grown 300 nm thick SiO_2 layer. Then the substrates are spin-coated with MMA and PMMA, and the EBL (JEOL 6510 with NPGS) is employed to define the source and drain pattern. The Cr/Au (5 nm/50 nm) electrodes are deposited by metal evaporation and lift-off processes. After HfO_2 deposition, top-gated electrodes (Au/50 nm) are completed by the second lithographic patterning and metallization process. Thickness of HfO_2 is ensured by Bruker Multimode 8 AFM and ellipsometer. Electrical characterizations are carried out with the Lake Shore TTPX Probe Station and Agilent 4155C Semiconductor Parameter Analyzer. Capacitance-voltage characteristics are measured with Agilent B1500A.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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