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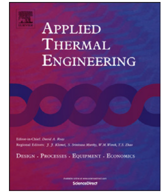

Evaluation of thermal performance of all-GaN power module in parallel operation

Po-Chien Chou, Stone Cheng*, Szu-Hao Chen

Dept. of Mechanical Eng., National Chiao-Tung University, Hsinchu 300, Taiwan

HIGHLIGHTS

- This work reveals the sorting process of GaN devices for parallel operation.
- The variations of $I_{D\ max}$, R_{ON}, V_P, and g_m with temperature are established.
- The temperature-dependence parameters are crucial to prevent hot spots generation.
- Safe working operation prevents thermal runaway and hottest cell destruction.

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ABSTRACT

This work presents an extensive thermal characterization of a single discrete GaN high-electron-mobility transistor (HEMT) device when operated in parallel at temperatures of 25 °C–175 °C. The maximum drain current ($I_{D\ max}$), on-resistance (R_{ON}), pinch-off voltage (V_P) and peak transconductance (g_m) at various chamber temperatures are measured and correlations among these parameters studied. Understanding the dependence of key transistor parameters on temperature is crucial to inhibiting the generation of hot spots and the equalization of currents in the parallel operation of HEMTs. A detailed analysis of the current imbalance between two parallel HEMT cells and its consequential effect on the junction temperature are also presented. The results from variations in the characteristics of the parallel-connected devices further verify that the thermal stability and switching behavior of these cells are balanced. Two parallel HEMT cells are operated at a safe working distance from thermal runaway to prevent destruction of the hottest cell.

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1. Introduction

Improvements in GaN-on-Si process technology in recent years have enabled large-area GaN HEMT power devices to be fabricated [1,2]. The availability of large-area devices does not ensure the economic viability of their mass production. As wide band-gap semiconductors, the die cost increases drastically with the size of the device because growth non-uniformity increases and processing yield declines [3,4]. This effect is the main reason for fabricating GaN power modules by bonding multiple lower-current cells in parallel to yield the desired high current rating. Previous studies have shown that the device power handling capabilities are dependent directly on maximum operating junction temperature [5,6]. We presented the methodology to raise the rating current of our GaN HEMT-based modules and our newly developed 200 V/45 A GaN module with the same package size as the 600 V 50 A IGBT power module. Proper thermal management is critical because localized self-heating effects under high power operation significantly impact device's performance and reliability. The use of infrared microscopy and electrical measurements (R_{ON} and $I_{D\ max}$) are employed to produce accurate channel to mounting temperature differentials. Most applications require that the junction temperature be maintained below 175 °C to ensure reliability [7,8]. The failure rate increases very rapidly about this temperature [9]. The junction temperature substantially affects influences switching characteristics and, therefore, dynamic current sharing. Several SiC-based power modules have been developed [10–13]. However, the performance of individual GaN HEMTs that are operated in parallel in a module has not been examined. Analysis of parallel operation of HEMTs in a module is difficult because access to individual devices is impossible unless they are un-encapsulated using infrared thermal imaging [14,15]. Accordingly, this study investigates the thermal parameters that influence static and dynamic current

* Corresponding author.
E-mail address: stonecheng@mail.nctu.edu.tw (S. Cheng).

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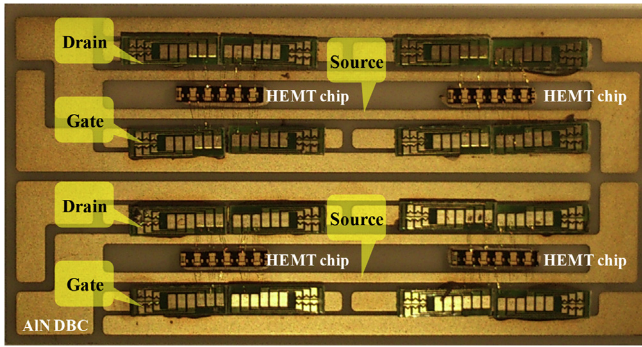

Fig. 1. Test module with four GaN HEMT chips mounted on a common source pad. A parallel drain leads extended to the upper, and a gate leads extended to the lower. The circuit layout is designed for die-level sorting.

sharing and, therefore, on junction temperature. The rest of this paper is organized as follows. The parameters that critically influence the feasibility of the parallel-connected HEMTs are experimentally examined [16,17]. The variations of maximum drain current ($I_{D\ max}$), on-resistance (R_{ON}), pinch-off voltage (V_P) and peak transconductance (g_m) with temperature in the range 25 °C–175 °C are obtained to elucidate the scaling of the device parameters [18,19]. The dependence of key transistor parameters on temperature is determined to support reliable parallel operation over a wide range of temperatures. Finally, analyses of the switching behavior of two parallel devices reveal a positive temperature coefficient of resistance tends to inhibit the generation of hot spots and to equalize the currents [20–22]. The results of the switching operation of devices further verify that these cells are thermally

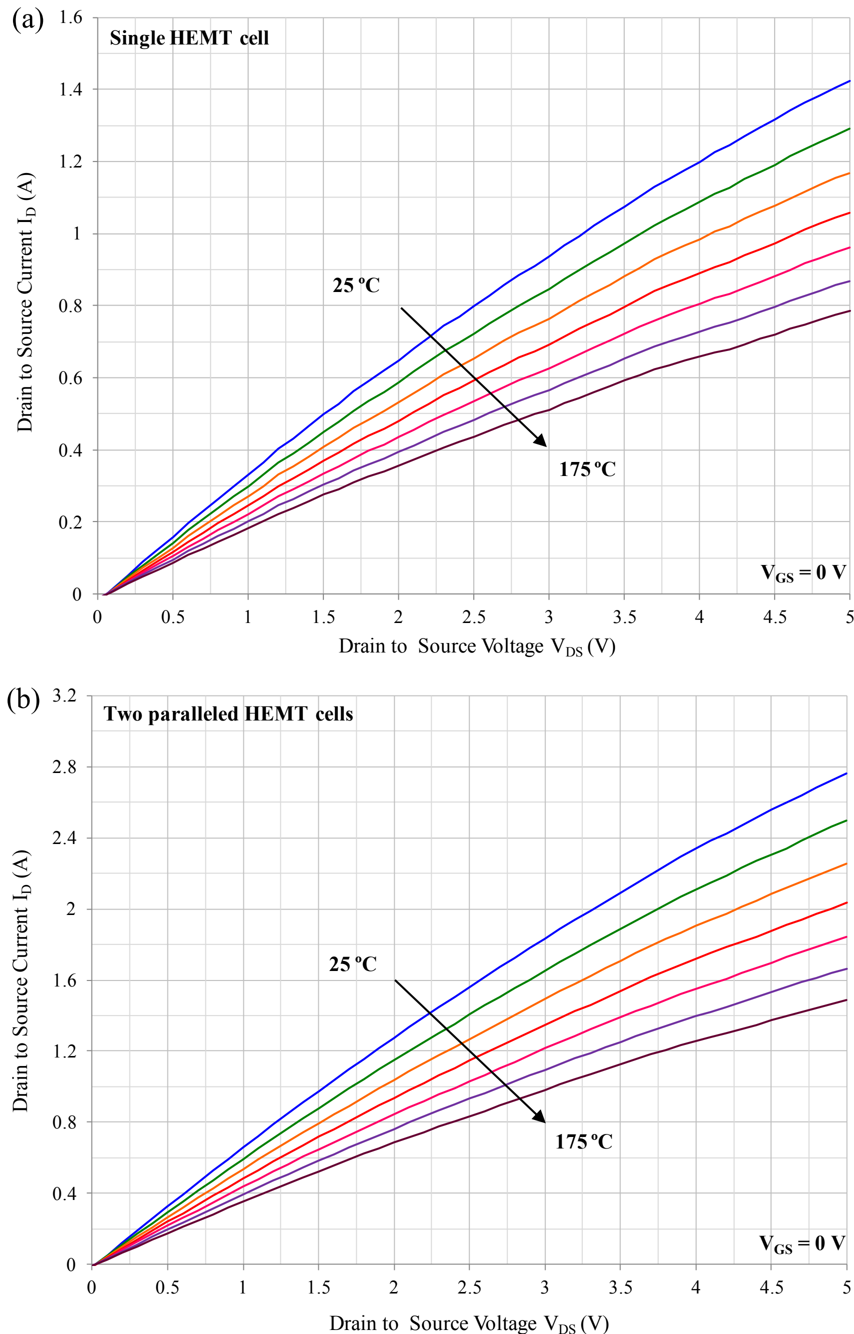

Fig. 2. Forward I_D–V_{DS} characteristics of (a) single and (b) parallel HEMT cells.

balanced with parallel compensation during switching transitions Fig. 1.

2. Packaging design of a ceramics-based GaN power module

Fig. 2 shows that each direct bond copper (DBC) substrate of a GaN power module contains an array of 24 GaN HEMT cells that are arranged in two rows of four chips. The chips are bonded to a common AlN substrate using sintered silver nano-particles and then wire-bonded to the electrical interconnect board. The DBC substrate provides good coefficients of thermal expansion (CTE) matching and a path for efficient heat transfer that removes heat from GaN HEMTs. According to the developed thermal stability criterion, favorable heat sharing (using a ceramic heat sink and the minimization of thermal resistance between HEMTs) causes the hottest cell to heat its surrounding cells, increasing their share of HEMT's drain current, greatly reducing the tendency for thermal runaway [23]. Additionally, unequal cooling of parallel HEMT cells can result in further current imbalance in the module since the GaN HEMT on-state and switching characteristics depend on temperature.

3. Static and transient behavior of GaN HEMTs at various temperatures

Following the characterization of individual dies, two cells were in the module were selected for parallel operation based upon matching output characteristics (I_D–V_{DS}) and transfer characteristics (I_D–V_{GS}). Current imbalance negatively affects the operation of parallel HEMTs. If the thermal resistance is constant and unaffected by temperature, then the junction temperatures of the parallel HEMTs may differ. To analyze current sharing, the effect of temperature must be analyzed in a steady state. The thermal performance of HEMTs was obtained for both single and parallel cells at various base-plate temperatures. The module was placed in a thermostatic chamber at ambient temperatures (T_A) of 25 °C–175 °C. For GaN HEMT, 175 °C yields the highest channel temperature. At each temperature, the DC I–V curves were measured, and maximum drain current ($I_{D\ max}$), on-resistance (R_{ON}), transconductance (g_m), and pinch-off voltage (V_P) were recorded. The experimental setup involved a Keithley 2601A, which operated the gate terminal and a Keithley 2651A, which operated the drain terminal, for electrical measurement. The current pulse widths were limited to minimize self-heating of the chips, which was less than 0.4 °C at the maximum current pulse. These electrical parameters were measured by simultaneously applying drain and gate biases at the sub-microsecond time-scale. Under this condition, dissipated power was negligible, and the channel temperature equaled the ambient temperature based on the assumption that the thermal conductivities of both GaN and Si were linear in the temperature range of 25 °C–175 °C. In each case, the least-squares curve that is fitted to the experimental data is plotted. The static and dynamic characteristics were extracted to reveal how these parameters scale-up in parallel GaN HEMTs.

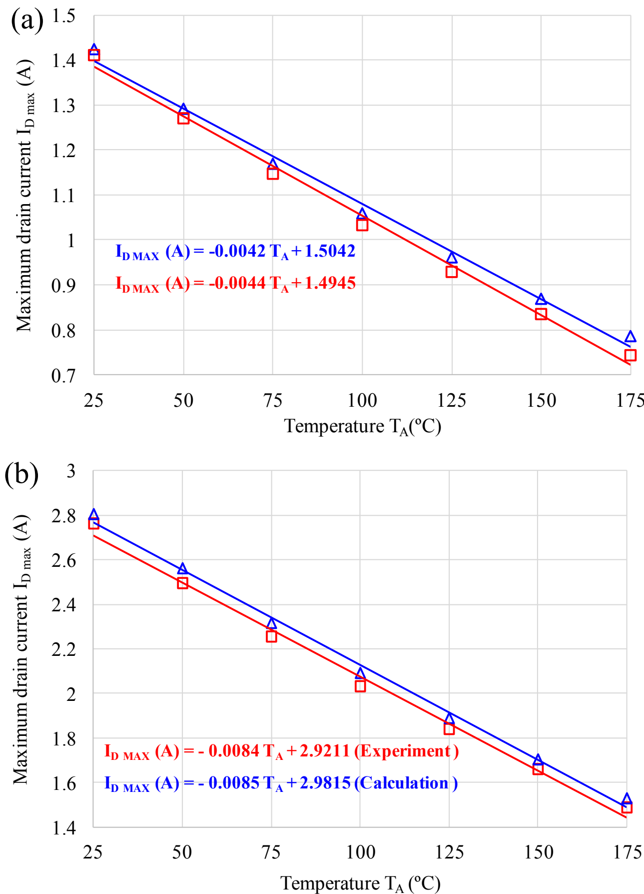

Fig. 3. Extracted $I_{D\ max}$ of (a) single and (b) parallel HEMTs over a range of temperatures, T_A, from 25 °C to 175 °C. The maximum drain current $I_{D\ max}$ (drain current at V_{DS} = 5 V and V_{GS} = 0 V) declined as the ambient temperature (T_A) increased.

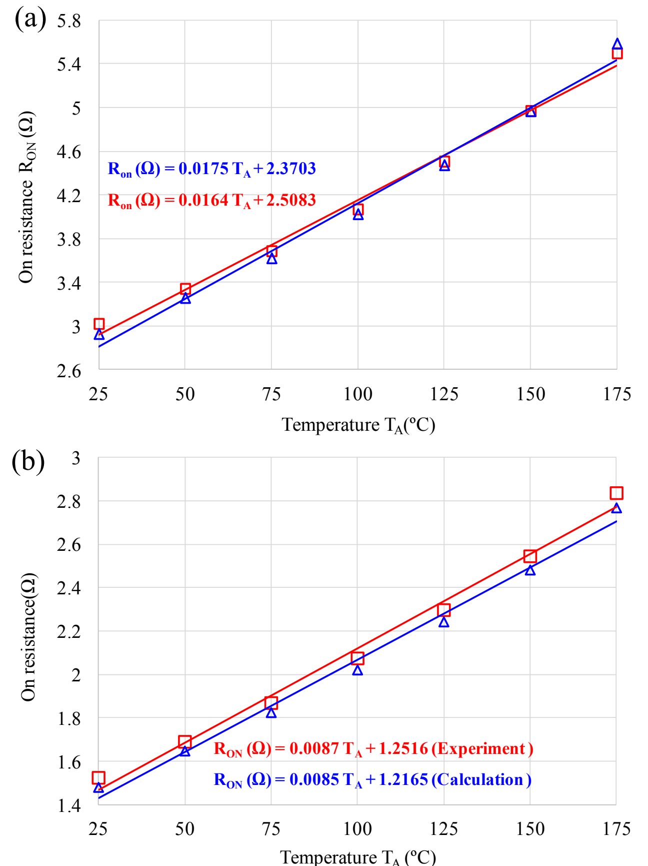

Fig. 4. Extracted R_{ON} of (a) single and (b) parallel HEMTs over a range of temperatures, T_A, from 25 °C to 175 °C. On-resistance R_{ON} increases with temperature T_A.

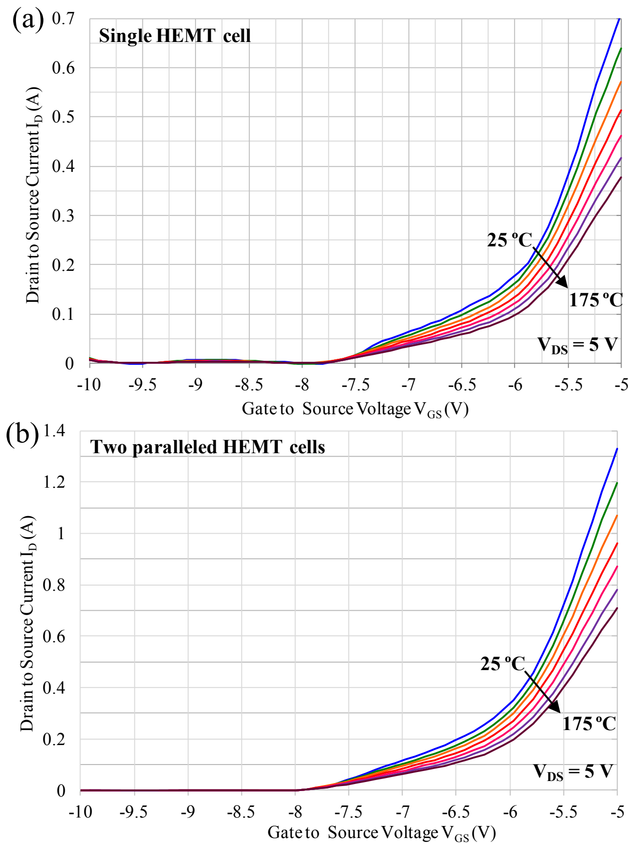

Fig. 5. Transfer characteristics (I_D–V_{GS}) of (a) single and (b) parallel HEMT cells.

3.1. Measurements of maximum drain current ($I_{D\ max}$) and on-resistance (R_{ON})

Fig. 2 plots the forward I_D–V_{DS} characteristics of both single and parallel GaN HEMT cells at temperatures from 25 °C to 175 °C. The I_D–V_{DS} plots were obtained by sweeping V_{DS} from 0 V to V_{DS} (max = 5 V) with V_{GS} set to 0 V. In Fig. 2, $I_{D\ max}$ is defined as I_D at V_{DS} = 5 V and V_{GS} = 0 V, and R_{ON} is defined as the reciprocal of the slope of I_D–V_{DS} in the linear region at V_{GS} = 0 V. Fig. 3 plots $I_{D\ max}$ for a single HEMT cell and for two parallel HEMT cells at temperatures from 25 °C to 175 °C. The mean square slope of $I_{D\ max}$ as a function of T_A is −0.42%/°C and −0.44%/°C for the two HEMT cells. Fig. 3(b) compares the variation of $I_{D\ max}$ with temperature for two parallel HEMT cells with the calculated value for single devices. The experimental and calculated $I_{D\ max}$ for two HEMTs slightly differ. Fig. 4 also plots the obtained on-resistances of both single and parallel cells at temperatures from 25 °C to 175 °C. As expected, the on-resistance, R_{ON}, *versus* T_A, has a slope of 1.64%/°C and 1.75%/°C for the two devices, respectively. The temperature coefficient was positive, indicating that, as temperature increased, $I_{D\ max}$ declined and R_{ON} increased. With a good thermal path between two parallel HEMTs, the positive temperature coefficient reduces the current in the hottest cell and forces more current to flow in the cooler cell, avoiding thermal runaway and destruction of the device. This process provides an essential thermal equilibrium that enables the two parallel cells to function reliably simplifying parallel operation. The on-resistance of two parallel HEMT cells was almost half of that of the single HEMT cell at the same ambient temperature. On-resistance R_{ON} increased with T_A at 0.87%/°C, and Fig. 4(b) presents excellent agreement between the experimental and calculated results.

3.2. Measurement of pinch-off voltage (V_P) and peak transconductance (g_m)

Fig. 5 plots the I_D–V_{GS} characteristics of single and parallel HEMTs. The I_D–V_{GS} plots were obtained by sweeping V_{GS} from −10 V to V_{GS} (max = 0 V) with V_{DS} set to 5 V. These HEMTs have a positive temperature coefficient throughout their operating range of temperatures and the currents in the cells in parallel are therefore expected to be equalized. The power MOSFET has a small region with a negative temperature coefficient where there no current-equalization occurs [24]. Operation within this region generates potential hot spots within the module and limits its current-carrying capacity. Fig. 6 shows that the pinch-off voltage shift increases with ambient temperature in both the single and parallel cells. V_P was calculated by extrapolating I_D in the I_D *versus* V_{GS} graph to I_D = 1% of the room temperature $I_{D\ max}$, at V_{DS} = 10 V, and taking the corresponding V_{GS} value as V_P. V_P was obtained at 1% of $I_{D\ max}$ rather than the typical 1 mA/mm leakage current because the leakage current depended strongly on temperature dependence because of the presence of defects. The changes in V_P with temperature for the two HEMT cells were 0.13%/°C and 0.16%/°C, respectively. The experimental results thus obtained during parallel operation depend on temperature in the same way. Fig. 6(b) reveals that the experimentally determined temperature increase of 0.14%/°C in the parallel HEMTs did not significantly differ from the calculated value. Fig. 7 plots the measured peak transconductance (g_m) as a function of temperature. The figure indicates that temperature was a significantly negatively related to g_m in both single and parallel cells. The change in g_m with temperature was −0.23%/

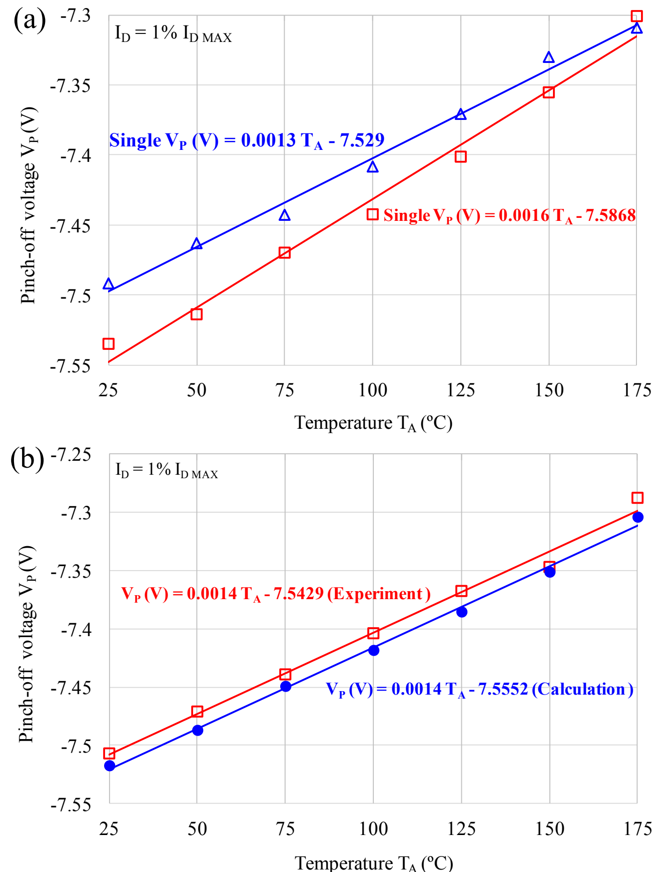

Fig. 6. V_P of (a) single and (b) parallel HEMTs over a range of temperatures, T_A, from 25 °C to 175 °C. Pinch-off voltage increased with temperature.

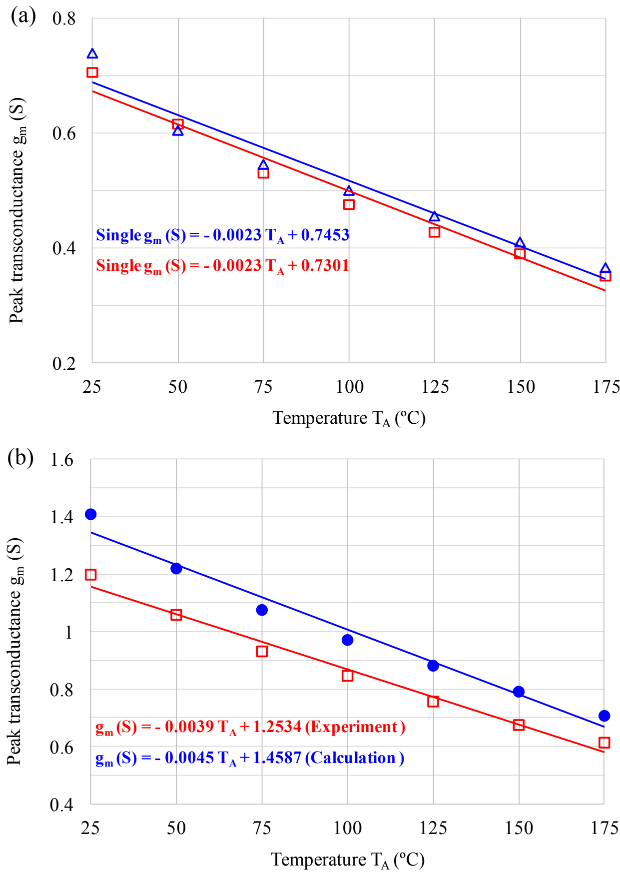

Fig. 7. Dependence of transconductance on temperature. Transconductance decreases with as temperature increases for both (a) single and (b) parallel cells.

°C for the single HEMT cell and −0.39%/°C for the two parallel HEMT cells. Notably, the calculated and experimental g_m values differed slightly owing to trapping at or near the surface. The parallel HEMT cells have a larger g_m than the single HEMT cell. This increase in g_m impacts the switching speed of the HEMT cell when they are in parallel.

4. Dynamic characterization and analysis of two parallel HEMT cells

Fig. 8 displays the switching performance when the circuit was tested using a gate pulse. The operating temperature was swept from room temperature to 175 °C in the same thermostatic

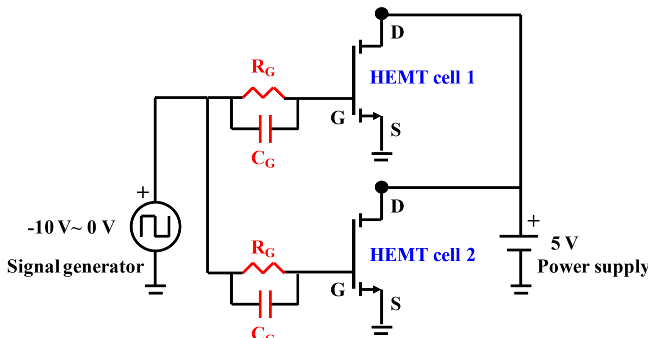

Fig. 8. Drive circuit.

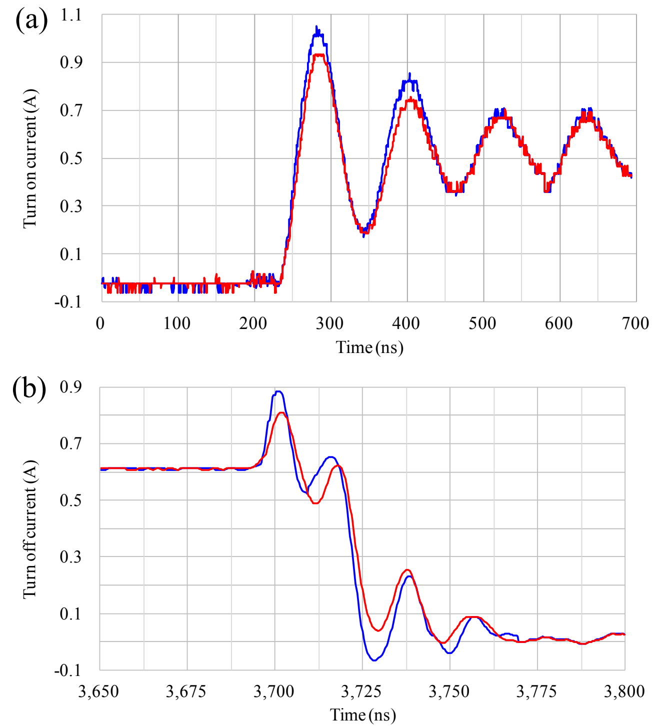

Fig. 9. (a) Turn-on and (b) turn-off waveforms of two parallel HEMT cells at room temperature, 25 °C.

chamber that was used to perform the static I–V characterization. Switching is carried out at the frequencies up to 100 kHz and a 20% duty cycle. Since low current densities and high voltages can result in thermal runaway in parallel operation, $V_{GS} = 0$ V is used for turn-

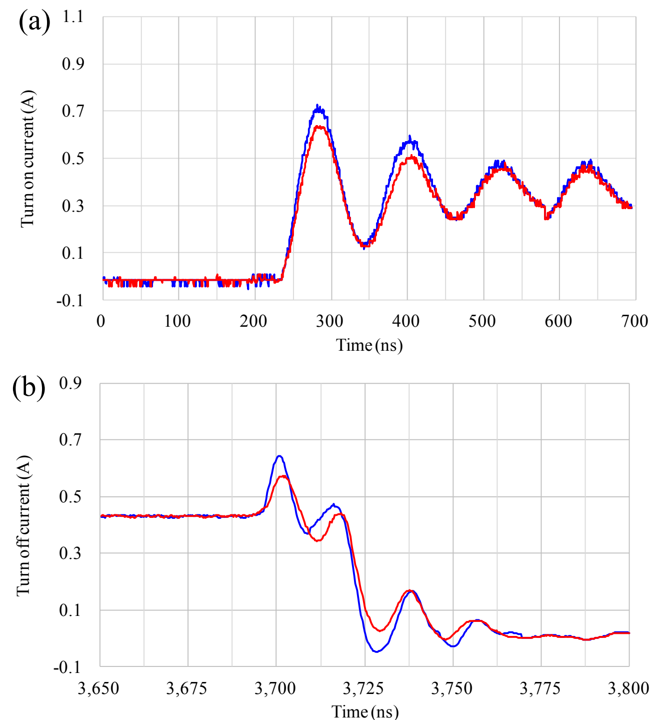

Fig. 10. (a) Turn-on and (b) turn-off waveforms of two parallel HEMT cells at an operating temperature of 175 °C.

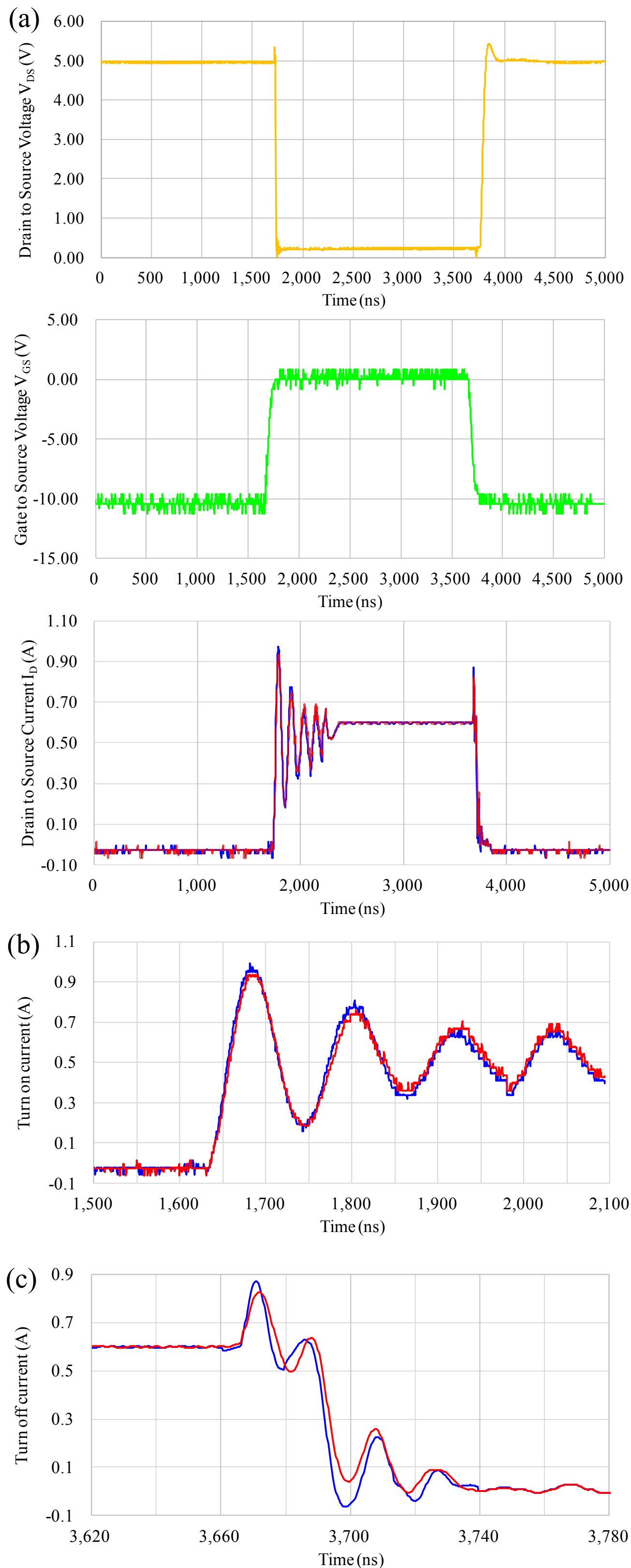

Fig. 11. Operating waveforms of two parallel HEMTs with a common gate drive. (a) Complete switching period. (b) Zoom-in during turn-on. (c) Zoom-in during turn-off.

on, and $V_{GS} = -10$ V is used for turn-off with V_{DS} held at 5 V. Each cell has its own gate resistance of 22 Ω and gate capacitance of 10 nF to stabilize the parallel operation during switching. The power test circuit must be symmetrical. The loop inductance in each test circuit must be as small as possible to minimize voltage overshoot when the device is turned off. The current rating of the assembly must not exceed 70%–80% of the total maximum current of the cells to compensate for the inevitable parameter mismatch between the cells. Even with thermal de-rating, a thermocouple is required to ensure that the individual operating temperatures are always close to each other [25].

Like SiC MOSFETs, GaN HEMT devices have a positive temperature coefficient in the on-resistance characteristics, which enables parallel operation. Figs. 9 and 10 plot the dynamic switching behaviors during the parallel operation of two HEMT cells. Based on the assumption that the base temperatures of the heat sink in the two packages are equal, and their thermal resistances are similar, the results of the switching operation may be regarded as effectively indicating temperature variation. Notably, the current is shared equally between the HEMT cells under initial transient conditions during turn-on and turn-off. Apparently, mismatching is minimal, and no oscillation is observed in current. The figure shows a very close waveform matching at turn-on. Equal current distribution of paralleled cells is essential to maintaining close matching of the junction temperatures of the individual cells and to prevent possible thermal runaway. Figs. 9(b) and 10(b) apparently reveal that current mismatching is minimal and remains essentially constant until each cell approaches the steady state. The test circuit must be symmetric with identical connection impedances of each cell.

Fig. 11 presents the repetitive switching of two parallel HEMT cells at room temperature, 25 °C. The figure clearly demonstrates that favorable current sharing was achieved in the HEMT pair when the junction temperatures were stabilized. The current waveforms are super-imposed, and their similarity limits the current mismatch between the HEMTs to only 0.2%, mainly because of the difference between the temperature-dependent parameters affects the dynamic behavior of the two parallel HEMT cells. The parasitic elements that are connected into circuit also contribute to this effect. In spite of the mismatches between the parameters of the HEMTs, a favorable current distribution in the two parallel HEMT cells is obtained using series gate resistors. The current imbalance, which causes variations in the junction temperatures of the HEMTs, is acceptable, possibly because of the similar driving conditions, the careful design of the common package, and the special attention that was paid to improving heat sharing among the HEMT cells. The satisfactory experimental results verify the feasibility of the parallel operation of discrete GaN HEMTs in which current can be shared between two parallel HEMT cells.

5. Conclusions

To justify the use of GaN technology in high-power, high-temperature applications, device performance must be evaluated across a wide range of temperatures to support the development of multi-chip power modules. This study examined thermal effects on the I_D–V_{DS} and I_D–V_{GS} characteristics of both single and parallel GaN HEMTs at temperatures from 25 °C to 175 °C. The highly uniform static current sharing between the cells prevents overloading of the device by an excessive current. The effects of temperature on maximum drain current ($I_{D\ max}$), on-resistance (R_{ON}), pinch-off voltage (V_P) and peak transconductance (g_m) are measured. The variations of $I_{D\ max}$, R_{ON}, V_P, and g_m with temperature are established for both single and parallel operations. The analyses of transient behavior revealed that two parallel HEMTs effectively

share current during inductive switching and maintain this sharing up to a high temperature of 175 °C. In spite of the mismatch between temperature-dependent parameters, the current sharing of the two parallel HEMT cells is satisfactory. The current imbalance, which is responsible for variations in the junction temperatures of the HEMTs, is acceptable when the parameters are appropriately sorted. Experimental results further verify the operation of parallel-connected HEMTs at a safe working distance from thermal runaway or destruction of the hotter cell.

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