40 nm Bit-Interleaving 12T Subthreshold SRAM With Data-Aware Write-Assist

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***Abstract*—This paper presents a new bit-interleaving 12T subthreshold SRAM cell with Data-Aware Power-Cutoff (DAPC) Write-assist to improve the Write-ability to mitigate increased device variations at low supply voltage under deep sub-100 nm processes. The disturb-free feature facilitates the bit-interleaving architecture that can reduce multiple-bit errors in a single word and enhance soft error immunity by employing error checking and correction (ECC) techniques. The proposed 12T SRAM cell is demonstrated by a 4 kb SRAM macro implemented in 40 nm general purpose (40GP) CMOS technology. The test chip operates from typical V_{DD} to 350 mV ($\sim$100 mV lower than the threshold voltage) with V_{DDMIN} limited by Read operation. Data can be written successfully for V_{DD} down to 300 mV. The measured maximum operation frequency is 11.5 MHz with total power consumption of 22 μW at 350 mV, 25 °C.**

***Index Terms*—Data-aware, low supply voltage, SRAM, subthreshold voltage, write-assist.**

I. Introduction

THE USAGE OF SRAM continuously increases in system-on-chip (SOC) designs. Recently, the demand for ultra-low power battery-operated devices is growing relentlessly, especially in implanted medical instruments and wireless body sensing networks where low supply voltage and low power SRAMs are required to extend system operation time under limited energy resources. Supply voltage scaling is the most effective way to reduce both switching power and leakage power for CMOS VLSI. However, designing robust SRAMs for near threshold or subthreshold operation is extremely challenging due to increased device variations and reduced design margins at low supply voltages with extremely scaled processes.

The conventional 6T SRAM cell has a very simple structure. However, its operation margin suffers from Read disturb, Half Select disturb, and the conflicting Read/Write requirements [1]. Moreover, due to increasing threshold voltage fluctuations caused by global and local process variations in advanced CMOS processes, the Read and Write stability of 6T SRAM degrade rapidly with V_{DD} scaling. Various Read/Write-assist schemes have been proposed for robust low-voltage operation [2]–[16]. These techniques include utilizing dual supply voltages to adjust the cell supply voltage [17], raising the cell virtual-VSS [18], reduced [17] or boosted word-line (WL) [19] and negative bit-line [2], [20]. However, the minimum operation voltage (V_{DDMIN}) of the conventional 6T cell is limited to around 700 mV [6]. Read disturb is one of the constraint for V_{DDMIN} of the conventional 6T cell. A 7T cell [11] was proposed to mitigate Read disturb at the expense of Write-ability due to single-ended Write operation. 8T [20] and 10T [21] cells with single-ended Read were also proposed. In these schemes, cell storage nodes were decoupled from the bit-line during Read operation to eliminate Read disturb and improve Read Static Noise Margin (RSNM). A 9T cell [22] was proposed utilizing feedback-cutoff NMOS transistors to enhance the Write margin and a dynamic Read decoupled scheme to eliminate Read disturb to achieve subthreshold operation. However, feedback-cutoff NMOS transistors caused floating storage nodes, which could be easily affected by leakage current and coupling noise. [6] proposed a 9T bit-cell with supply feedback to internally weaken the pull-up current during Write cycles. It utilized a storage node to control the gating PMOS transistor. However, the Write "1" ability and Hold "1" stability became worse and could be easily disturbed. Many studies have also proposed peripheral assist circuits to improve the Read/Write stability under subthreshold operation. However, the peripheral circuits are susceptible to global and local variations. For example, negative bit-line (NBL) is an effective scheme to improve Write-ability. When variations become severe, especially under low voltage operation, the negative voltage range may become limited, resulting in insufficient negative voltage level and Write failure. Conversely, excessively negative voltage level may cause the storage data of the Write half-select cells in the selected column to be flipped.

Furthermore, when SRAMs operate under near-threshold or subthreshold region, alpha-particles or energetic cosmic rays can potentially induce soft errors more easily because the critical charge, Q_{CRIT}, is reduced [23]. Soft error rate (SER) can be reduced effectively by combining bit-interleaving architecture with error correction code (ECC) techniques [24]–[26]. In [19], a cross-point Write structure using series-connected double-layer NMOS pass transistors is employed to eliminate Write half-select disturb and facilitate bit-interleaving architectures at the expense of Write-ability. As such, both the row-based word-line and column-based Write word-line need to be boosted to enhance Write-ability for subthreshold operation due to the series NMOS pass transistors. The boosted Read/Write assist circuits require large boosting capacitors and

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complex timing control logics, thus incurring large overhead on area and timing control design. Moreover, the boosting ratio depends strongly on the supply voltage. At lower supply voltages, it needs a larger boosting capacitor to have a sufficient boosting ratio.

In this work, we propose a novel 12T bit-cell with a differential cross-point data-aware power-cutoff (DAPC) Write-assist for low-voltage operation. During the Write operation, depending on data-in, the proposed bit-cell internally cuts off supply voltage for either the left or right half-cell to weaken the pull-up network of the bit-cell, thus assisting the discharging of the storage node. This proposed scheme improves Write-ability without employing additional peripheral Write-assist circuits and related boosting and timing control circuits. Furthermore, this bit-cell employs a cross-point Write structure with a data-aware column-based Write Word-Line (WL) to eliminate Write Half-Select (WHS) disturb. Thus, the bit-cell supports a bit-interleaving architecture to improve soft error immunity. The rest of the paper is organized as follows. Section II discusses the severe process variation under low supply voltages. The detail and operation of the proposed 12T SRAM cell are described in Section III. Section IV explains the architecture and design considerations of a 4 kb SRAM test macro implemented in 40GP bulk CMOS technology. Section V presents the measurement results to validate the 12T SRAM performance. Section VI concludes this paper.

II. Driving Strength Ratios at Low Supply Voltages

SRAM design faces the challenges of degraded on/off current ratio and the large process, voltage and temperature (PVT) variations in the near-threshold and subthreshold region [2]. At low supply voltage, SRAM suffers instability in Write and Read operations due to large variability of the "ON" current (Ion) caused by threshold voltage fluctuations resulting from global and local process variations. Fig. 1(a) shows the simulated driving current of MOSFET at 65 nm and 40 nm bulk CMOS process technologies for general purpose application with 10 000 samples Monte Carlo simulations at 350 mV supply voltage. The distribution of 40 nm (line with circular dots) is much wider than that of 65 nm (line with square dots). The standard deviation of the driving current of 40 nm process technology is 1.77× of 65 nm. Fig. 1(b) illustrates the ratio of NMOS "ON" current (Ion_n) to PMOS "ON" current (Ion_p) with the minimum iso-size transistors. There are 173 cases (circled by the dash line) with ratio less than 1 under low voltage operation (350 mV) for 10 000 samples Monte Carlo simulations. On the other hand, all ratios are larger than 1 under typical voltage operation (900 mV). The results show that the variations are much more severe at low supply voltages. The ratio of less than 1 means that the driving current of PMOS is stronger than NMOS. This situation affects the Write-ability of SRAM bit-cells, especially for the conventional bit-cells with Read/Write β-ratio sizing conflict, rendering the sizing of bit-cells more difficult. The first row of Table I shows the threshold voltage (Vt) of NMOS and PMOS, and the values of Vt are normalized to 65 nm. The second row represents one sigma variation of Vt ($1\sigma\Delta\text{Vt}$) and the values are also normalized to 65 nm. The data show that the local variation in 40 nm bulk CMOS process increases significantly and is 67% and 89% larger than that in 65 nm process for NMOS and PMOS, respectively. This paper proposes a robust 12T bit-cell to mitigate variations in advanced bulk CMOS technology. The proposed

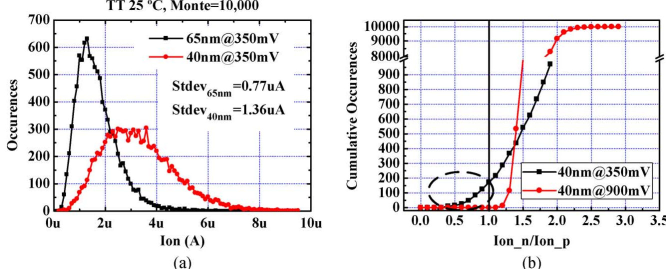

Fig. 1. (a) Simulated driving current of 65 nm and 40 nm, (b) simulated ratio of driving current of iso-size N/PMOS between subthreshold and super-threshold supply voltages with 10 000 samples Monte Carlo simulations.

TABLE I
Local Random Variation of Minimum Size Device

	NMOS		PMOS	
	65 nm	40 nm	65 nm	40 nm
Vt (normalized)	1x	1.21x	1x	1.45x
1 σ ΔVt (normalized)	1x	1.67x	1x	1.89x

bit-cell selectively cuts off the power supply for the half-cell where "0" is to be written into the storage node to eliminate the contention from the cell pull-up network, thus significantly enhancing the Write-ability.

III. The Proposed 12T SRAM Cell

Fig. 2(a) and (b) show the schematic and cell layout of the proposed 12T SRAM cell. The 12T SRAM cell consists of a core, PUL, SWL, PDL, PUR, SWR, and PDR, and differential Read/Write ports, PGL1, PGL2, PGL3, PGR1, PGR2, and PGR3. The Read Word-Line (RWL) and Virtual VSS (VVSS) are row-based, and Write Word-Line A (WWLA), Write Word-Line B (WWLB), Bit-Line (BL), and Bit-Line Bar (BLB) are column-based. The cell layout shows the layers from diffusion up to metal-3. The logic layout rules in 40GP CMOS process restrain the poly-to-poly space to several discrete spacing due to the concern of poly critical dimension uniformity (CDU) control. To comply with the design rule, we have to add 4 segments of dummy-poly in the bit-cell as shown in Fig. 2(b). Additionally, we share the dummy poly, diffusion and contacts as much as possible to minimize the bit-cell and SRAM array area. As shown in Fig. 2(b), we use the minimum width for all cell transistors. The reason is that the proposed bit-cell employs Read buffers to decouple storage nodes (Q and QB) from BL and BLB to eliminate Read disturb and DAPC Write-assist to enhance Write-ability, thus there is no sizing conflict between Read and Write operations. However, we enlarge the length of PDL and PDR by 2× to reduce the leakage current of SRAM arrays to reduce static power consumption by 48% compared with that using the minimum lengths for PDL and PDR. The simulated post-layout timing diagram of the 12T cell is shown in Fig. 2(c). In Hold mode, RWL, WWLA and WWLB are disabled and VVSS is held at V_{DD}. Data is held by cross-coupled inverters and decoupled from BL/BLB. Table II lists the truth table of the proposed 12T bit-cell for different operation conditions.

A. Read Operation With Read Buffer

In Read mode, the selected RWL is enabled and the corresponding VVSS is forced to ground, while WWLA and WWLB remain disabled. Read buffers read the stored data to BL and

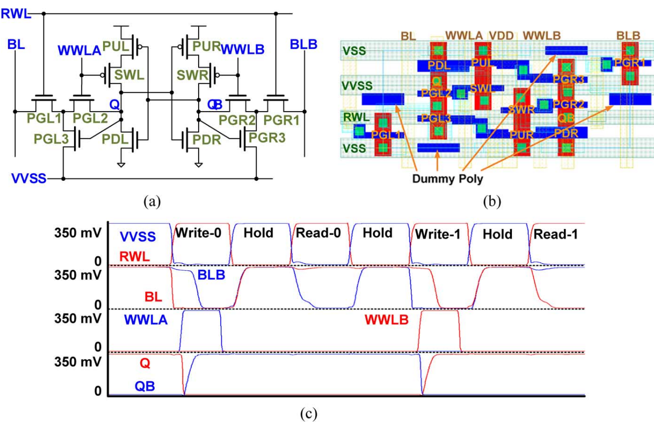

Fig. 2. (a) Schematic, (b) cell layout, and (c) simulated post-layout timing diagram of the proposed 12T SRAM.

TABLE II
OPERATION CONDITION OF THE PROPOSED 12T SRAM CELL

	Hold	Read	Write '0'	Write '1'
RWL	GND	V_{DD}	V_{DD}	V_{DD}
VVSS	V_{DD}	GND	GND	GND
WWLA	GND	GND	V_{DD}	GND
WWLB	GND	GND	GND	V_{DD}
BL	V_{DD}	V_{DD}(floating)	GND	V_{DD}
BLB	V_{DD}	V_{DD}(floating)	V_{DD}	GND

BLB. Due to the differential bit-line (BL and BLB) configuration, we employ a current-mode latch sense amplifier (SA) [27] to sense the difference of the voltages of BL and BLB for robust Read operation. To reduce the offset voltage of SA, dummy MOSs are placed adjacent to SA circuits. Since the disabled WWLA/WWLB turn on SWL/SWR and turn off PGL2/PGR2 to isolate Q and QB from BL and BLB, respectively, the Read Static Noise Margin (RSNM) of the 12T SRAM cell is almost equal to its Hold SNM and is much larger than that of 6T SRAM cell. The 12T SRAM cell has Read SNM of 120 mV at 350 mV V_{DD}. Even though the 6T SRAM cell has been sized up by increasing the width of the pull-down NMOS transistors to mitigate Read disturb, the RSNM of the upsized 6T SRAM cell is only 27.5 mV as shown in Fig. 3. The RSNM improvement is $4\times$ even if 6T SRAM cell is sized up to the same area of the 12T SRAM cell. In addition, two NMOSs with minimum size are stacked in the BL/BLB to VVSS paths, thus the Read current of the 12T SRAM cell is $1.39\times$ less than that of the 6T SRAM cell. However, because the VVSSs of unselected cells sharing the same BL and BLB are held at V_{DD}, the BL leakage of the 12T SRAM cell is $4.77\times$ less than that of 6T SRAM cell as shown in Fig. 4. Therefore, a BL can afford more memory cells by using the 12T SRAM cell than the 6T SRAM cell during Read operation. Although, the 12T SRAM cell does not have Read stability problem, some peripheral Read-assist circuits can also be used to enhance Read speed without stability degradation, e.g., cascaded bit-line scheme [13].

B. Write Operation With Cross-Point Data-Aware Power-Cutoff Write-Assist (DAPC)

Fig. 5 illustrates the Write operation of the 12T SRAM cell with data-aware column-based WWLs. In Write "0" operation as shown in Fig. 5(a), RWL and WWLA are enabled; VVSS and BL are forced to ground; BLB is forced to V_{DD} while WWLB remains disabled. Then, node Q is discharged by BL through PGL1/PGL2 and by VVSS through PGL3 to Write "0" into the selected cell. At the same time, SWL is cut off and there is no charging path from V_{DD} to node Q. For Write "1" operation (Fig. 5(b)), RWL and WWLB are enabled; VVSS and BLB are forced to ground; BL is forced to V_{DD} while WWLA remains disabled. Then, node QB is discharged by BLB through PGR1/PGR2 and by VVSS through PGR3 to Write "1" into the selected cell. At the same time, SWR is cut off and there is no charging path from V_{DD} to node QB.

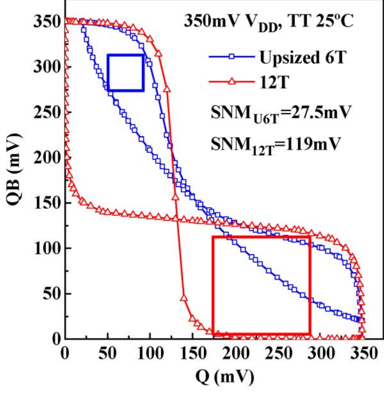

Fig. 3. Simulated Read SNM of Upsized 6T and the proposed 12T.

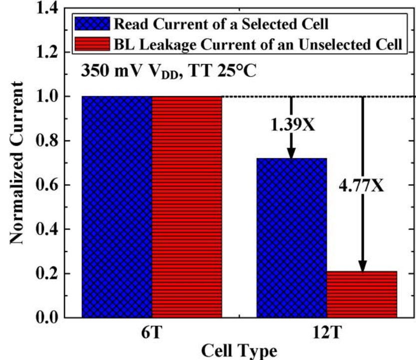

Fig. 4. Simulated BL leakage and Read current comparison.

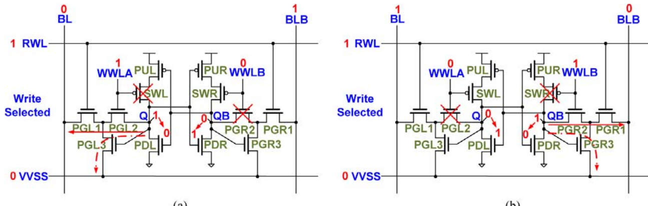

Fig. 5. Write operation of the proposed 12T SRAM cell, (a) Write selected cell with write "0," (b) Write selected cell with Write "1."

Since both the row-based RWL and column-based WWLA/WWLB need to be enabled to Write the selected cell and each column is selected individually via the values of WWLA and WWLB (i.e., Data-in), the cell provides a cross-point Write structure and there is no disturb for half-select cells during Write operation. Fig. 6 shows the Write Static Noise Margin (WSNM) versus V_{DD} at the Slow N Fast P (SNFP) corner (the worst corner for Write) of the proposed 12T cell, the 10T cell in [19] and the conventional 8T cell in [20] with iso-area sized for Write operation. The proposed 12T cell has the best WSNM due to the DAPC Write-assist scheme. The WSNM is 156 mV

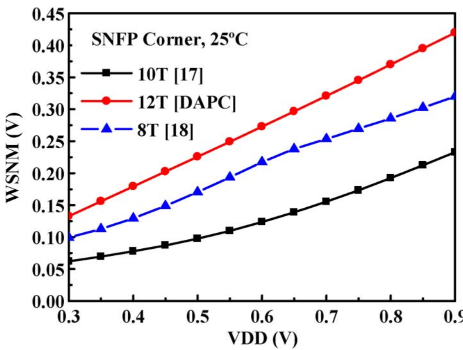

Fig. 6. Write SNM comparison of 8T, 10T and 12T cells with iso-area at SNFP and 25 °C.

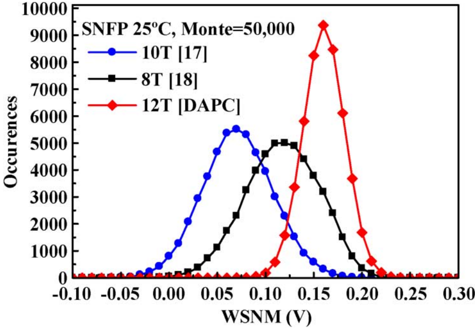

Fig. 7. Write SNM comparison at 0.35 V V_{DD} with 50 000 samples Monte Carlo simulations.

at 350 mV V_{DD}. Fig. 7 shows the Monte Carlo simulation results of WSNM at SNFP, 350 mV and 25 °C. The mean value of WSNM of the proposed 12T cell is 1.38× and 2.2× of the conventional 8T [20] and 10T cell in [19], respectively. Moreover, since the proposed 12T cell does not have P/N contention during Write operation, Write-assist techniques can also be used to enhance Write speed without stability degradation, e.g. boosted word-line [19] and/or negative bit-line [10].

Fig. 8 shows the Monte Carlo simulation results of Write failure rate of the three SRAM cells at SNFP, 25 °C with local random variation. A Write failure occurs when the Write margin becomes negative. The conventional 8T SRAM cell [20] with the conventional 6T Write mechanism has Write failure when V_{DD} is lower than 500 mV. Since the 10T SRAM cell [19] performs Write operation through two stacked NMOS, the Write margin of the 10T SRAM cell is worse than that of conventional 8T SRAM cell and Write failure of the 10T SRAM cell happens when V_{DD} is lower than 600 mV. In contrast, the 12T SRAM cell has no Write failure when V_{DD} is higher than 300 mV.

C. Column Write-Half-Select (WHS)

During Write operation, the column-based WWLA or WWLB cuts off the stacked SWL or SWR of the column WHS cells as illustrated in Fig. 9. During Write "0" to the selected cell, if node Q of the column WHS cells store "0," the "0" could be safely latched by NMOS (PDL/PDR) as shown in Fig. 9(a). However, if node Q of the column WHS cells store "1," the node would be at a floating-V_{DD} situation since the stacked PMOS/SWL is cut off as shown in Fig. 9(b). Fortunately, VVSS is attached to logic-1 level for the unselected rows during Write operation, and node L could be charged to high voltage level

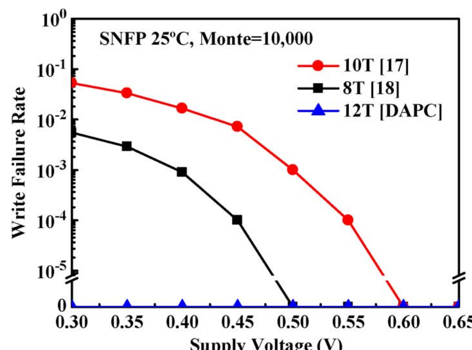

Fig. 8. Write Failure Rate comparison at SNFP and 25 °C with 10 000 samples Monte Carlo simulations.

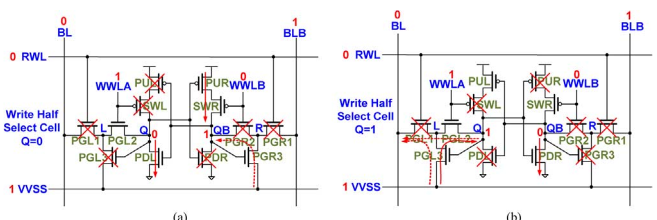

Fig. 9. Column Write half-select cell of the proposed 12T SRAM cell, (a) column WHS cell with Q = 0, (b) column WHS cell with Q = 1.

by PGL3 which is turned on by node Q. After WWLA turns on PGL2, node Q would be charge-shared by node L, and node Q would maintain its voltage at a high level. Node Q and L are weakly clamped at a high level by PGL2 and PGL3. As the floating-1 data at node Q suffers the leakage through the off transistors PGL1 and PDL, the floating-1 data at node Q would decrease slowly. Data-Retention-Time (DRT) is defined as how long the data at node Q stays above the logic-1 threshold. The situation of QB node is the same as Q node because of the symmetric cell structure.

To mitigate the degradation of floating-1 level of Q or QB in column WHS cells, the Write WL pulse width of WWLA/WWLB must be longer than the Time-to-Write of the selected cell but shorter than the DRT of the column WHS cells. Extensive Monte-Carlo simulations indicate that the DRT is significantly longer than the Time-to-Write at 350 mV V_{DD}. Fig. 10 shows the Monte Carlo simulation results of the Write selected cell and Write half-select cells. As shown in Fig. 10, the Write time margin is still 2× longer than Write time even with local random variation. It shows that the bit-cell can function properly by designing a proper word-line pulse width between the Write time and DRT.

Table III compares the characteristics of the SRAM bit-cells. The proposed 12T SRAM bit-cell (DAPC12T) with data-aware Write-assist eliminates both Read disturb and Write half-select disturb. Furthermore, the DAPC12T cell exhibits better Writeability than single-ended disturb-free (SEDF9T) cell [2] and bit-interleaving 10T (BI10T) cell [19] due to the power-cutoff Write technique. The bit-cell area of the DAPC12T cell with all minimum size transistors is 1.64× of the conventional 8T cell. The ratio would become smaller than 1.64× if the conventional 8T cell is sized up for Write consideration. Although the conventional 8T cell can be sized up for Write, its V_{DDMIN} is still limited by the Write operation due to P/N contention. The

TABLE III
CHARACTERISTICS OF SRAM BIT-CELLS

Bit-cell	6T	8T	CP8T[15]	BI10T[19]	CLA10T[16]
Schematic					
Read/WHS Disturb Free	✗/✗	✓/✗	✗/✓	✓/✓	✗/✗
Write Method	P/N Fighting*	P/N Fighting*	P/N Fighting*	P/N Fighting*	P/N Fighting* + CLA***
Bit-cell Area	0.77X	1X	1.1X	1.61X	1.2X

Bit-cell	SF9T[6]	SEDF9T[2]	LAT12T	This Work
Schematic				
Read/WHS Disturb Free	✓/✗	✓/✓	✓/✗	✓/✓
Write Method	Supply Feedback	P/N Fighting* + DAWA WWLs**	Feedback Cutoff	Power Cutoff + DAWA WWLs**
Bit-cell Area	1.2X	1.52X	2.31X	1.64X

* P/N Fighting: Fighting between pull-up PMOS and pass-gate NMOS ** DAWA WWLs: Data-Aware Write-Assist Write Word-Lines
*** CLA: Column Line Assist

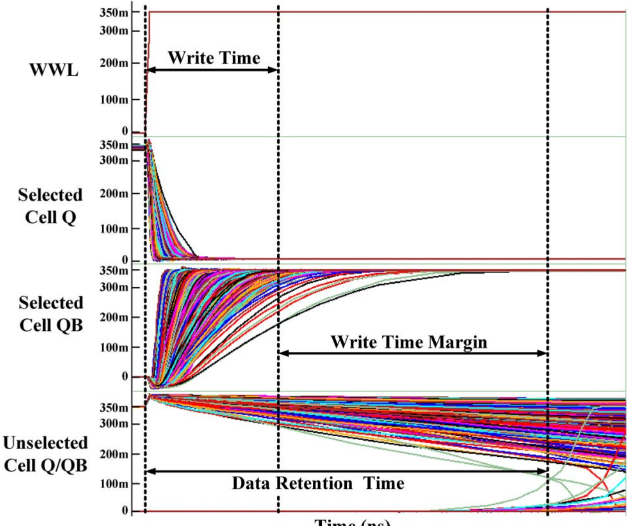

Fig. 10. Simulated column Write half-select cells with 5000 samples Monte Carlo simulation.

sub-array bit-density of the conventional 8T and the DAPC12T is 186 $\mathrm{MB/mm^2}$ and 113 $\mathrm{MB/mm^2}$, respectively.

IV. TEST CHIP IMPLEMENTATION

To verify the proposed SRAM cell, a 4 kb SRAM test macro is implemented in 40GP CMOS technology. The floorplan of the 4 kb SRAM macro is shown in Fig. 11. The 4 kb SRAM macro consists of 4 blocks with 16 rows by 64 columns per block. The I/O is 16 bits wide. Due to the disturb-free nature of the 12T cell, the test chip employs distance-4 bit-interleaving architecture, which can reduce soft error by using single-bit error correction code compared with non-bit-interleaving architecture [24]. The decoders and other peripheral circuits use static CMOS logic for robust subthreshold operation. The entire array functions at one supply voltage. Signals are transferred into or out of the 4 kb SRAM macro through level shifters. Because of the large voltage difference between the typical supply voltage (900 mV) and intended V_{DD} for the 4 kb subthreshold SRAM macro, two intermediate voltages are applied in level-down (LVD) and level-up (LV) shifters to ensure the signal integrity.

In the test chip, we utilize 4 kinds of inverter chains to generate different pulse widths, and the control signals are controlled by external pins. Thus we can adjust the Write word-line pulse width during Write operation to prevent the stored data in WHS cells from flipping with excessively long Write word-line pulse width.

The procedure of the Read operation is as follows. First, the word-line enable (WLE) signal is activated to enable the signal, PA, which is determined by row pre-decoder circuits (XPRED). Second, the selected Read word-line (RWL) is asserted by the enabled PA signal to turn on the pass gates (PGL1/PGR1). Third, the selected bit-cell by RWL starts to access the stored data to local BL. Fourth, local evaluation circuits (LDIDO), SAs, begin to transfer the data from local BL to global BL (GBL). Finally, the data are delivered from GBL to the data outputs (DO) by global evaluation circuits (GDIDO). The components of the post-layout simulated Read access time at 350 mV, 25 $^{\circ}\mathrm{C}$, and TT corner are shown in Fig. 12. The portion from WLE to RWL consumes 54% of the Read access time. The cell access time from RWL to BL consumes 8%. The rest 38% is consumed for BL to transfer the data to DOs. The post-layout simulated Read access time is 30.27 ns at 350 mV, TT, 25 $^{\circ}\mathrm{C}$. The Write time is significantly shorter than the Read access time, as the length of Write time is up to when cell

BSEL: Bank select
XDEC4: 4-bit row decoder

Fig. 11. The floor plan of 4 kb SRAM test chip.

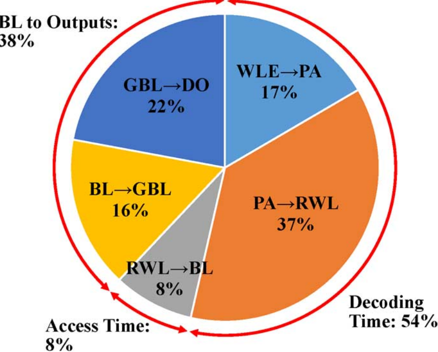

Fig. 12. Components of post-layout simulated Read access time at 350 mV, TT, and 25 °C.

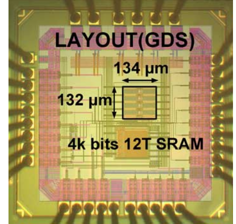

Fig. 13. Microphotograph of SRAM test chip.

storage nodes flip. The post-layout simulated Write access time is 23.01 ns at 350 mV, TT, 25 °C.

The 4 kb test chip core area is 134 μm × 132 μm. The microphotograph of the test chip is shown in Fig. 13. Because there is a passivation layer covering the test chip, the microphotograph shown is composed of the layout view overlaid on the actual test chip.

V. Measurement Results

Fig. 14 shows the measured waveforms captured by the logic analyzer at 350 mV. In the top of Fig. 14, we Write all "1" first when Write Enable Bar (WEB) signal is "0," then Read all data written in the 4 kb SRAM array when WEB is "1." In the bottom of Fig. 14, the measured pattern is the worst case for Write half-select cells and Read selected cells. When Writing "0" to the selected cells, all other cells on the same column store "1" (worst case pattern for Write half-select cells), the column-based WWLA will be forced to V_{DD} to cut off the feedback of the memory cells on the selected columns. It is advantageous for Write selected cells, but an undesired condition for WHS cells.

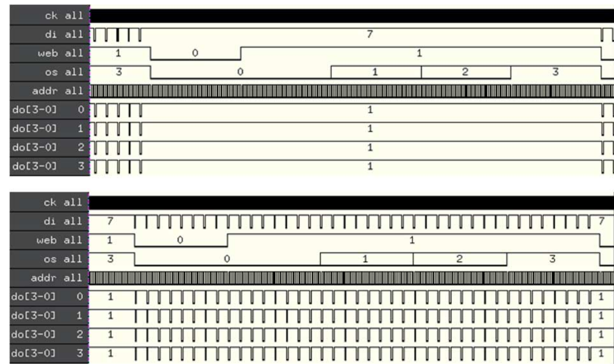

Fig. 14. Measurement results using logic analyzer.

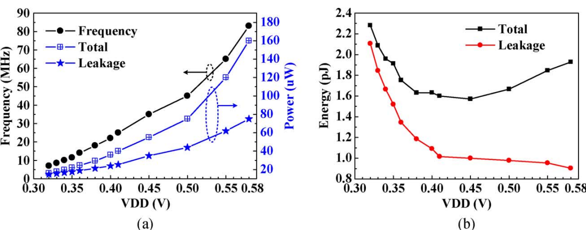

Fig. 15. (a) Measured maximum frequency and power consumption, and (b) measured energy per operation, at maximum frequency versus V_{DD} at 25 °C.

For Read "0," all other unselected cells on the same column store "1" (worst case pattern for Read). The test chip works correctly under the worst case pattern as shown in the bottom of Fig. 14. Furthermore, as four 4-to-1 multiplexers are used to reduce the number of output pins due to pad limitation, we use two output select pins to select the data output signals for measurement.

Fig. 15(a) shows the measured maximum operation frequency of the test chip. The test chip works correctly under the worst case input test patterns at 350 mV V_{DD} with 11.5 MHz operation frequency. There are only 3 bits failure in 4 kb from 320 mV to 340 mV V_{DD} with a 10 mV step. The V_{DDMIN} of the test chip is 350 mV and is limited by Read operation. The limitation is due to the sense amplifiers since the sense amplifiers cannot differentiate the voltage difference from the differential bit-lines correctly when the supply voltage is lower than 350 mV. The Write V_{DDMIN} is lower at 300 mV and is the same as the Hold V_{DDMIN} because the proposed cell has significantly improved Write-ability. Furthermore, the measurement set-up introduces a 50 mV peak-to-peak supply noise even with decoupling capacitors, thus limiting the measurement of V_{DDMIN}. The measured total and leakage power dissipation at the maximum operation frequency are also shown in Fig. 15(a). At low voltage, leakage power dominates the total power dissipation because there is a longer static time duration in the operation period at a slow operation frequency than at a fast operation frequency. Thus, leakage power is about 79% (64%) of total power dissipation at 350 mV (450 mV).

Fig. 15(b) shows the measured average energy per operation for accessing data at the maximum operation frequency. A tradeoff between power and operation frequency can be found in the near-threshold region with a slightly higher power figure, but with a significant increase in performance. The 12T SRAM in 40GP technology achieves better energy saving at near-threshold region ranging from 380 mV to 450 mV. The minimum energy per operation is 1.6 pJ at 450 mV. The

TABLE IV
FEATURE LIST OF WORKS

	[14][20]	[19]	[6]	This Work
Cell/Process	8T/65 nm	10T/90 nm	9T/40 nm LP	12T/40 nm GP
V_{DDMIN}	350 mV	160 mV	400 mV (Measured) 250 mV (Simulated)	350 mV 300 mV (Write)
Memory Capacity	256 kb	32 kb	8 kb	4 kb
Frequency @ V_{DDMIN}	25 kHz	500 Hz	1 MHz @ 400 mV	11.5 MHz 3 MHz (Write)
Total; Leakage Power @ V_{DDMIN}	3.4 μW; 2.2 μW	0.123 μW; N. A.	N. A.; 60 nW*	22.0 μW; 17.5 μW
Total; Active Energy /operation @ V_{DDMIN}	136 pJ; 48 pJ	246 pJ; N. A.	N. A.; 0.36 pJ*	1.91 pJ; 0.39 pJ
Peripheral Write Assist Scheme	50 mV WL boosting; Collapsed VDD	80 mV (50% V_{DD}) WL boosting	-	-
Bit-interleaving	No	Yes	No	Yes

*: Only the array and internal peripherals (precharge circuits, write drivers, sense inverters)

V_{DDMIN} of the 4 kb test chip is 350 mV which is much lower than that of the conventional 6T SRAM. The test chip operates correctly at 11.5 MHz and consumes 22.0 μW at 350 mV V_{DD}. Table IV compares key features of several subthreshold SRAM designs. It is to be noted that we proposed a 12T bit-cell to reduce leakage power and total power as much as possible by subthreshold operation in an aggressively scaled 40 nm CMOS node which is characterized for high performance applications. The leakage power level is not as low as previous implementations in 65 nm or 180 nm nodes with additional techniques to reduce leakage power. We proposed a low-power and subthreshold operation memory in a high-performance node instead.

VI. CONCLUSION

A bit-interleaving 12T subthreshold SRAM cell with data-aware power-cutoff Write-assist has been demonstrated in this paper. The 12T cell eliminates Read disturb and Write half-select disturb, and improves the Write-ability by using data-aware power-cutoff scheme for robust subthreshold operation. Low-voltage operation is accomplished without the need for any additional peripheral Write- and Read-assist circuits. A 4 kb test chip has been implemented in 40GP CMOS technology. The measured results demonstrate error free functionality under the worst-case bit-line data patterns down to 350 mV ($\sim$100 mV lower than the threshold voltage), limited by Read operation. Data can be written successfully down to 300 mV. In subthreshold region, the 4 kb test chip operates at 11.5 MHz with 22 μW power consumption. The minimum energy per operation is 1.6 pJ at 450 mV.

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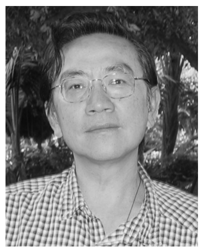

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