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Effects of threading dislocations on drain current dispersion and slow transients in unpassivated AlGaN/GaN/Si heterostructure field-effect transistors

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Current transient analysis combined with response to pulsed bias drives have been used to explore the possibilities of threading dislocations affecting the current dispersion characteristics of AlGaN/GaN heterostructure field-effect transistors (HFETs). A growth strategy is developed to modulate the dislocation density among the heterostructures grown on silicon by plasma-assisted molecular-beam epitaxy. Slow pulsed I-V measurements show severe compressions and appear to be significantly dependent on the threading dislocation density. By analyzing the corresponding slow detrapping process, a deep-level trap with emission time constant in the order of seconds was identified as the cause. Among the specimens, both in the epilayers and at the surface, the number of dislocations was found to have a notable influence on the spatial distribution of deep-level trap density. The observations confirm that the commonly observed degraded frequency performance among AlGaN/GaN HFETs in the form of DC-radio frequency dispersions can at least partly be correlated with threading dislocation density. © *2014 AIP Publishing LLC*.
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Current dispersion remains a major reliability constraint in realizing the true potentials of AlGaN (or InAlN)/GaN based heterostructure field-effect transistors (HFETs).[1,2] The phenomenon is characterized by significant decrease in microwave power output from those predicted by DC load line curves, and exemplifies increase in knee voltage in addition to the collapse of the channel current (I_{DS}) at pulse biases. Till date, the emergence of a charged "virtual gate"[1] is the most accepted model for this manifestation with SiN surface passivation being the preferred solution of the same, regardless of the inconsistent success.[3] However, the precise origin of the involved trap states, along with the exact physical mechanisms behind trapping and passivation are still vastly unknown.

On the other hand, threading dislocations (TDs), often present in large numbers in the heteroepitaxially grown III-Nitride epilayers on sapphire/Si substrates, are a topic of great interest. Numerous arguments on the adverse effects of TD density (TDD) on device properties such as luminescence efficiency in light emitters[4] (LEDs and LASERs) or leakage current density in Schottky diodes[5] are well documented in literature. In contrast, whether the same deep-level nature and line charging characteristics of TDs that diminish luminescence and create vertical/lateral leakage paths, are also responsible for current dispersion accompanied by slow transients, is a plausibility that has not been well explored.[6,7] Besides, majority of the comparative studies on properties of dislocations involved growth on different substrates and/or epitaxial reactors. On account of such properties being greatly influenced by the stoichiometry and the nature of the strain fields around the dislocation core,[8] the interpretations might not have been exhaustive.

Several self-consistent density-functional and first-principles empirical potential based calculations as well as experimental observations of electron energy loss spectra (EELS) around the core have long-established the deep level identity of both screw and edge dislocations.[9,10] Compared to most other impurities, vacancies, and antisite defects, the carrier emission time constant (τ_{en}) from such trap states are estimated to be much higher (in the order of seconds) owing to their theoretical position in the bandgap (E_g).[7] Furthermore, if an electron trap can be considered at every $c/2$ translation of a dislocation,[8,11] the volume concentration of these traps among different epistructures should vary proportionately to their TD densities. Also, such observations should hold true for spatial probing of trapping/detrapping phenomenon, since threading dislocations should be able to induce traps throughout the epilayers, and also at the intersections with the surface.

In this regard, the present investigation aims to perceive the correlations between the threading dislocation density (TDD) and the deep-level traps that give rise to current collapse accompanied by severe gate/drain lags. Accordingly, comprehensive analysis of pulsed output characteristics (I-V data) and detrapping transients are performed on molecular-beam epitaxy (MBE) grown dislocation-modulated AlGaN/GaN/Si HFETs (spanning TD density orders apart). Experimental observations supported by

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proposed mechanisms were found to sufficiently explain the physical processes involved in dispersion for all the specimens.

All the heterostructures were grown on Si (111) substrates in a SVTA plasma-assisted MBE (PAMBE) system, equipped with conventional elemental Ga and Al effusion cells, and nitrogen rf-plasma source (SVTA-RF45). The identical devices were comprised of a thin AlN nucleation layer, a GaN/AlN interlayer stack, a thick GaN buffer layer, an undoped $Al_{0.3}Ga_{0.7}N$ barrier, and a GaN cap layer with nominal thicknesses as shown in Fig. 1(a). Reports suggest that the traditional methods of controlling dislocations in other III-Vs such as insertion of a super lattice structure (SLS) or varying the thickness of the buffer itself may not be that effective for GaN heteroepitaxy.[12] Hence, to modulate dislocations among the epistructures, an alternative approach was adapted, which require precise substrate temperature (T_{Sub}) variation during specific layer growth while keeping all other parameters alike. For that purpose, the growth temperature (calibrated by emissivity corrected pyrometry with two colour reflectometry, SVTA-IS4K) of AlN nucleation layer was kept at either 800 °C (for wafer A and B) or 950 °C (wafer C), whereas the final GaN buffer layer was grown at 715, 740, and 750 °C for wafer A, B, and C, respectively.[13]

It is well documented that in material systems having large lattice mismatches (such as ∼19% between AlN and Si in present case), epitaxy supposedly commences with nucleation of hexagonal pyramids, faceted on low energy $\{1\bar{1}00\}$ and (0001) planes. These pyramids eventually coalesce giving rise to TDs at each coalescence boundary.[14] Thus, an increase in T_{sub} during AlN nucleation layer growth decreases the aspect ratio of the nucleating islands, but increases their density,[15] which in turn effectively increases the overall TD density. Additionally, both the wafer curvature and the stress relaxation rate of the thick GaN buffer on the GaN/AlN stress mitigating stack is known to gradually rise with growth temperature, and reportedly results in a higher dislocation density.[16] On these accounts, the dislocation density was found to consistently increase among the wafers A, B, and C as confirmed by dark-field diffraction contrast imaging in a JEOL JEM-2100 transmission electron microscope (TEM) operated at 200 kV. For the micrographs, cross sectional samples were prepared by standard techniques of ultrasonic disc cutting, mechanical polishing, dimpling, and Ar^+ ion milling at 3 kV up to electron transparencies. In all the samples, interacting TDs and stacking faults were indistinguishable at the interface, but the $\langle 0001 \rangle$ propagating TD density was fairly constant in the rest of the buffer, and barrier layers (Figs. 1(b)–1(g)). Trace analysis from several regions yielded a dislocation count of $\sim 1 \times 10^9/cm^2$ for A, $\sim 7 \times 10^9/cm^2$ for B, and $\sim 5 \times 10^{10}/cm^2$ for C, thus validating the anticipated growth approach. Also, the dislocation types were determined from systematic $\bar{g}.\bar{b}$ visibility criteria, where g and b are, respectively, the diffraction vector and the burgers vector. Notably, most of the dislocations were projected out of contrast in $\bar{g} = 0002$ two beam conditions, but were visible with $\bar{g} = 11\bar{2}0$, thus designating an edge character (pure a-type or mixed a + c-type) with $\bar{b} = \frac{1}{3}\langle 11\bar{2}0 \rangle$ for majority of the dislocations.

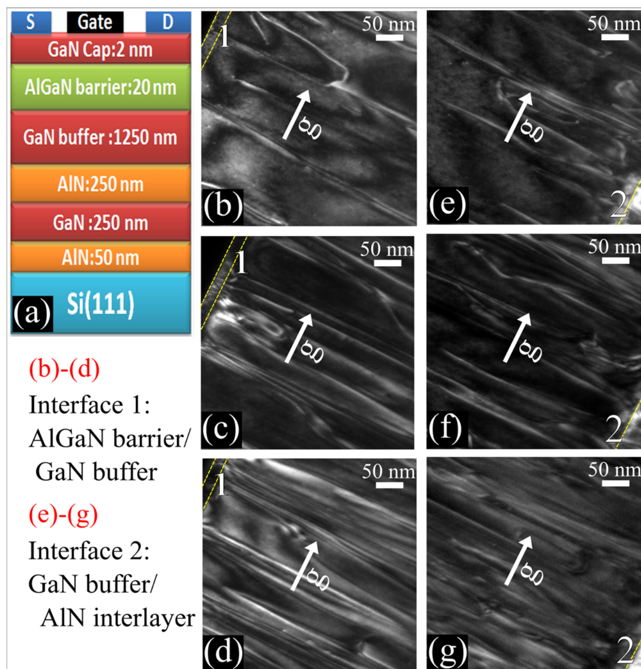

FIG. 1. (a) Represents the epitaxial schematic of the heterostructures with nominal epilayer thicknesses. Also, dark-field cross sectional TEM images of (b), (c), and (d) taken under two-beam conditions with g = $[11\bar{2}0]$ show the variation of TD distribution at the AlGaN barrier/GaN buffer interface for specimen A, B, and C, respectively, whereas images (e), (f), and (g) show the corresponding variation at the GaN buffer/AlN interlayer interface for the same specimens.

HFETs with double fingered $2 \times 50\,\mu m$ gates ($L_{SG} = 3\,\mu m$, $L_{GD} = 15\,\mu m$) were fabricated by simultaneous optical contact lithography on all the three wafers by source-drain ohmic metallization, mesa isolation by Cl_2/Ar plasma etching, and e-beam deposition of gate metal stack. No passivation schemes were employed so as to thoroughly examine the characteristics of the surface states.

Pulsed I-V measurements, which provide an approximate assessment on the effects of trapping on large signal performance, were carried out on fabricated devices in common source configuration by a Keithley 4200SCS parameter analyzer modular framework with digitizing oscilloscope. Coplanar HFETs were probed with synchronized gate and drain pulses from various quiescent points (Q_{DC}: $V_{GS} = 0$ V, $V_{DS} = 0$ V; Q_{SGF}: $V_{GS} = -6$ V, $V_{DS} = 0$ V; Q_{DGN}: $V_{GS} = 1$ V, $V_{DS} = 10$ V; and Q_{DGF}: $V_{GS} = -6$ V, $V_{DS} = 10$ V) to scrutinize the trapping site and nature. Larger voltages were avoided to prevent any long term defect degradation, and to represent intrinsic device conditions. In our experiments, to analyze both the capture time and the severity of the deep-levels involved, pulses with large ON time (5 ms) and OFF times (5/45/95 ms) were implemented. The measured pulsed currents from DC bias condition (Q_{DC}) were in accordance to the respective sheet resistivity (for $V_{GS} = 1$ V, $V_{DS} = 10$ V; I_{DSS}(A): 523 mA/mm, I_{DSS}(B): 658 mA/mm, and I_{DSS}(C): 466 mA/mm), and showed no indication of compression or trapping. Conversely, for the other bias states, different extents of current collapse (such as in Figs. 2(a) and 2(b)) was observed in all the specimens, which can be quantitatively described by normalized compression factor (n.c.f.)

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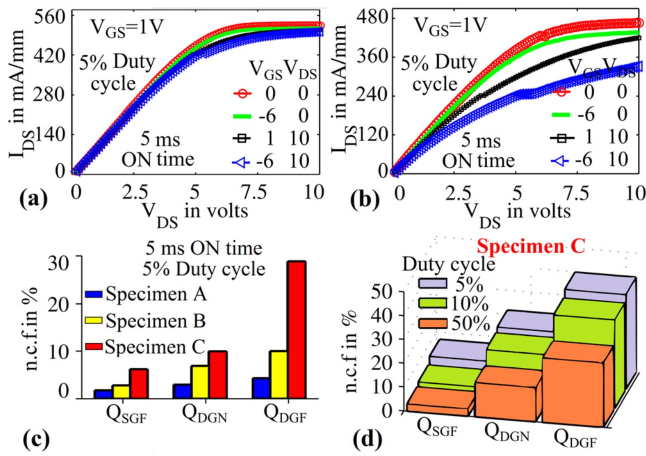

FIG. 2. (a) and (b) illustrates the markedly different pulsed I-V curves for specimen A and C, respectively. Also, the various levels of compression, (c) among the specimens for identical bias conditions, and (d) in individual specimens (such as C, the one with the highest dislocation density) for different duty cycles and biasing, correlate TDDs with pulsed responses.

$$\text{n.c.f. (in \%)} = \frac{I_{DS}(Q_{DC}) - I_{DS}(Q_{ref.})}{I_{DS}(Q_{DC})} \times 100, \quad (1)$$

where $I_{DS}(Q_i)$ is the drain current in either the saturation ($V_{GS} = 1$ V, $V_{DS} = 10$ V; Fig. 2(c)) or linear ($V_{GS} = 1$ V, $V_{DS} = 6$ V; Fig. 2(d)) regime, pulsed from the respective bias condition. Visibly, for any biasing state and pulsing scheme, current compression for representative devices increased in the order of wafer A < B < C, in all regions of operation. This behavior is quite evident from the comparisons of Fig. 2(c) where in particular n.c.f. of I_{DSsat} from Q_{DGF} bias conditions escalated among specimen A, B, and C from 4.3% to 10.0%, and 28.8%, respectively. Also, with decreasing duty cycle (increasing pulse filling time) the compression was more intense in all specimens (e.g., as seen in Fig. 2(d), a tenfold decrease in duty cycle increased n.c.f. in specimen C from 14.2% to 21.6% for Q_{DGN} and 27.0% to 39.8% for Q_{DGF} biasing, and probing I_{DS} in the linear region). The generalization of the findings was confirmed by using different sequences of bias and allowing restoration to normal state. All these results established the presence of a deep-level trap having a large capture time constant (τ_{cn}) and two main features: (i) the trap density increases progressively from wafer A to C, and (ii) the trap can induce significant current collapse for favourable trapping conditions both in the buffer (Q_{DGN}) and in the barrier/surface (Q_{DGF}).

Conventional deep level trap spectroscopy (DLTS) is not suitable for the detection of deep-level traps in wide bandgap AlGaN/GaN HFETs partly for the very high temperature requirements, and also for the difficulties involved in data acquisition and interpretation.[17,18] Hence, to extract signature emission time constants (τ_{en}), detrapping transient methodology[19,20] was customized to quantify relative trap magnitudes from single temperature measurements. Consequently, either a high OFF-state ($V_{GS} = -6$ V, $V_{DS} = 8$ V) or a high ON-state ($V_{GS} = 1$ V, $V_{DS} = 10$ V) 1 s long filling pulse was applied and the temporal response of the I_{DSlin} (at $V_{GS} = 1$ V, $V_{DS} = 3$ V) for all the three specimens were monitored by sampling the drain current at finite time intervals. Next, the detrapping transient data were fitted to a sum of exponentials having logarithmically equispaced time constants ranging from 1 ms to 100 s as in

$$I_{DS}(\text{transient}) = a_0 + a_1 \exp(-t/\tau_{1en}) + a_2 \exp(-t/\tau_{2en}) + \cdots + a_n \exp(-t/\tau_{nen}), \quad (2)$$

where a_i quantifies the trap having detrapping emission time constant τ_{ien}. For fitting purpose, a finite differencing method based non-linear algorithm was developed in which the total number of coefficients (n) was optimized for least computation time as well as for accuracy of relative amplitudes and time constants of the traps. The as-computed relative densities along with their emission time constants are reconstructed in the plots of Fig. 3, revealing the presence of a prominent deep level trap ($\tau_{en} > 1$ s). Here, as depicted in Fig. 3(a), a slight variation among the peak positions (from 3.054 s for C to 7.743 s for B) can be observed in the detrapping transient analysis after a high OFF-state pulse. In contrast, the recovery transients from high ON-state pulse features almost identical time constants (~2 s) along with a dramatic increase in the relative trap amplitude for specimen C (Fig. 3(b)). Remarkably, for either of the implemented pulses, the trap density among the three specimens increased in a manner consistent with earlier pulsed I-V analysis.

In view of the absence of deep level dopants, the characteristics of the trapping/detrapping dynamics can be well explained considering dislocation induced states. The OFF-state trapping (Fig. 4(a)) originates from the gate leakage current, and comprises of Frenkel-Poole emission into the AlGaN barrier and/or 1-D hopping conduction[21] over the surface states (presumably created by the extended intrusion of the dislocations at the surface, and acting as virtual gate). On the other hand, during an ON-state pulse as in Fig. 4(b), trapping is most likely to occur in the conducting buffer region. Notably, the moderate bias conditions implemented in this study are not energetically sufficient for the channel

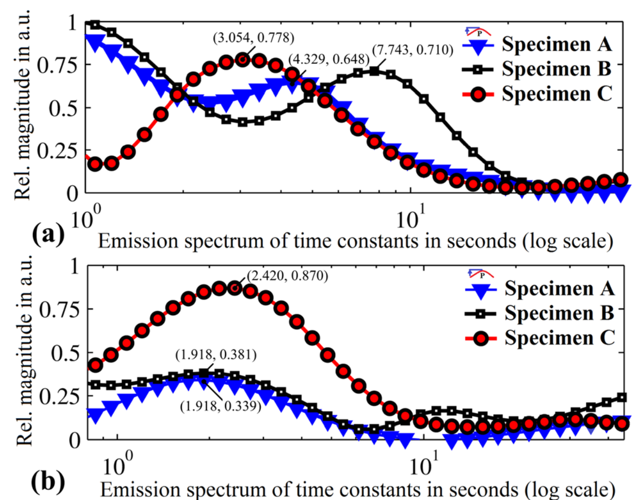

FIG. 3. Emission time constant spectra for all the HFETs as analysed from detrapping transients after (a) high OFF-state or (b) high ON-state pulse. The values in the parenthesis designate the time constant, and the relative trap density for each of the specimens during the corresponding detrapping process. The presence of a prominent deep-level trap is prominent in both the spectrums.

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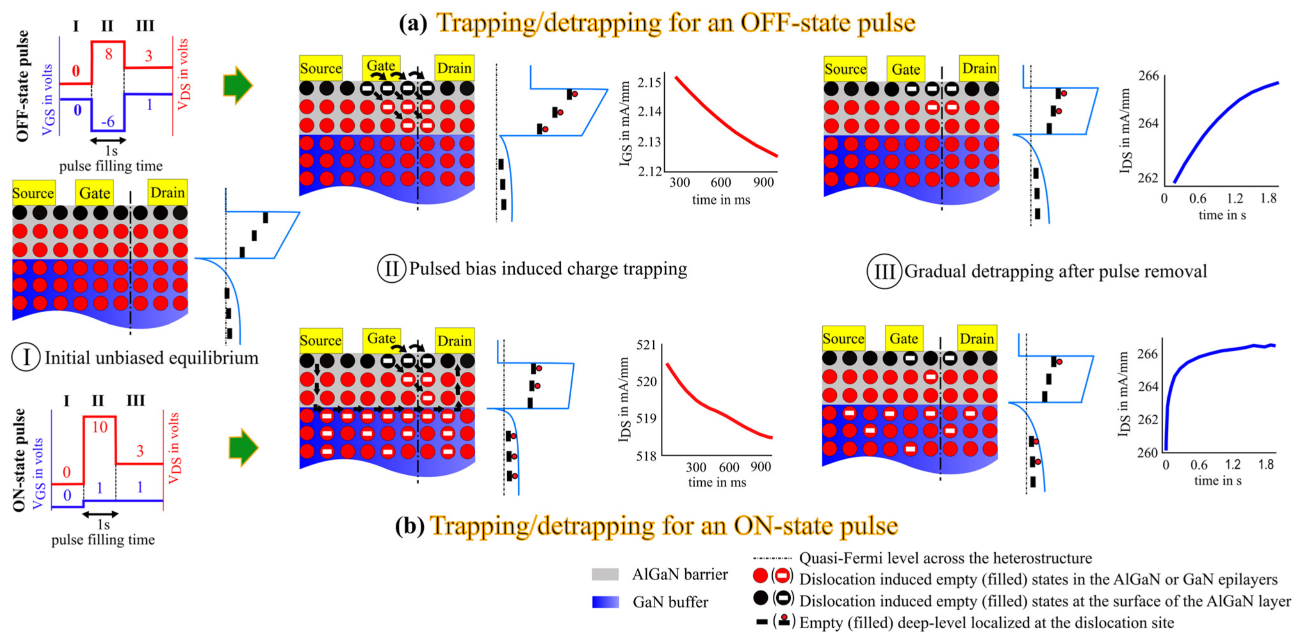

FIG. 4. Postulated physical mechanisms involved in dislocation induced trap related processes corresponding to (a) high OFF-state pulse and (b) high ON-state pulse. The heterostructure band diagrams at the cutline are shown along with the time evolution of relevant currents for specimen A in each state.

electron to overcome the conduction band discontinuity at the heterojunction or create a hot electron injection near the buffer/substrate interface. Thus, buffer trapping phenomenon involves only those dislocation states that are in proximity of the channel in the GaN layer. Additionally, depending upon the gate leakage during the ON-state pulse, trapping may take place also in the barrier by mechanisms analogous to the OFF-state pulse. Now, as for either of the pulses, trapping process at any instant is proportional to the number of remaining unoccupied states, and hence, the trapping currents (I_{DS} or $|I_G|$) decreases exponentially with time. Subsequently, during detrapping under the dark measurement conditions, release of the electrons from the captured states to the conduction band minima can only be aided by thermal emission with corresponding large τ_{en}. On that note, the observed variations in Fig. 3(a) could have arose from the change in activation energy of the dislocation related deep-levels owing to the unintentional composition fluctuations in the barrier[22] (as the molecular fluxes were the same but the T_{Sub} for $Al_xGa_{1-x}N$ growth varied in accordance with the underlying GaN layer). Such dependence modulates τ_{en} of the traps participating in OFF-state detrapping, and hence, the exact time constant cannot be undoubtedly confirmed. Though, for obvious reasons this has little influence on the observed ON-state spectrum of Fig. 3(b), nevertheless significant additional trapping in the barrier during the ON-state pulse resulted in a sharply enhanced trap density for the specimen C, having an order higher ON-state gate leakage than the other two representative devices.

A comparison of the outcomes from this study with the ones reported in literature further strengthens the proposed dislocation-defect origin of relevant deep-level traps. A notable increase in density of such traps with large τ_{en} was found to occur after a 10-h long OFF-state stress in similar transient analyses of GaN HFETs on SiC,[20] but were mostly non-existent in unstressed devices.[19,20] Consistent with the inverse piezoelectric effect created evolution of structural defects under stress degradation,[23] an analogous nature can indeed be assigned to dislocations. Then, the absence of these traps in unstressed HFETs can be reasoned by the far less number of dislocations in GaN grown on SiC owing to the reduced lattice mismatch. On another instance,[24] the recoverable trapping phenomenon indicated the presence of deep-level traps prior to the stress tests with the activation energy and trapping mechanisms bearing close resemblance to dislocation assisted tunnelling transport.[25] Though the trapping effects were ambiguously attributed to "C" dopants, involvements of the deep-levels induced by dislocations are also very likely given the pronounced presence of the later in nitride epilayers on Si as stated before.

In conclusion, the measurements and analysis of pulsed response, and transient curves unveiled a correlation between TDDs and deep-level traps for unpassivated AlGaN/GaN/Si HFETs. Significant compression of the pulsed I-V characteristics indicated trapping phenomenon both in the bulk and at the surface. The emission time constant extracted from drain current transients also exhibited the presence of a deep-level trap. Shallow defects cannot be held responsible for such characteristics. Also, as both the severity of the pulsed current collapse and density of the deep-levels were found to vary in accordance with TDDs, hence the origin of such deep-levels can certainly be attributed to electrically active dislocations. Further assessment of the exact trapping process and involved dislocation type is presently under investigation.

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