Built-in Effective Body-Bias Effect in Ultra-Thin-Body Hetero-Channel III–V-on-Insulator n-MOSFETs

Chang-Hung Yu, *Student Member, IEEE*, and Pin Su, *Member, IEEE*

***Abstract*— This letter reports a built-in effective body-bias effect in ultra-thin-body (UTB) hetero-channel III–V-on-insulator n-MOSFETs. This effect results from the discrepancies in electron affinity and the effective density-of-states of conduction band between the III–V and conventional Si channels. Our study indicates that, in addition to permittivity, it is the built-in effective body-bias effect that determines the drain-induced-barrier-lowering characteristics of the hetero-channel devices. This intrinsic effect has to be considered when one-to-one comparisons among various UTB hetero-channel MOSFETs regarding the electrostatic integrity are made.**

***Index Terms*— Ultra-thin-body (UTB), III-V, hetero-channel, drain-induced-barrier-lowering (DIBL), electrostatic integrity (EI).**

I. Introduction

HIGH-MOBILITY III-V materials such as $In_xGa_{(1-x)}As$ have been proposed as hetero-channels (high-mobility channel with Si-substrate) for post-Si CMOS devices because of their superior carrier transport properties [1]–[6]. However, one intrinsic drawback of these III-V compounds is their higher permittivity and worse device electrostatic integrity (EI) [6]. Ultra-thin-body (UTB) structure with thin buried oxide (BOX) has been regarded as promising device architectures to mitigate the EI problem [7], [8]. In addition to better gate control and smaller random dopant fluctuation (due to undoped or lightly-doped channel [9], [10]), the UTB with thin BOX structure also enables more efficient threshold-voltage (V_T) modulation and power/performance optimization through body bias (V_{BS}) [7], [8]. Besides the permittivity, whether there is any other intrinsic mechanism determining the EI of UTB hetero-channel III-V-on-insulator (III-V-OI) devices is an important question. In this letter, with the aid of TCAD simulation, we report a built-in effective body-bias effect in UTB III-V-OI n-MOSFETs. Its impacts on the drain-induced-barrier-lowering (DIBL) characteristics of various hetero-channel devices have also been investigated.

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The authors are with the Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail of corresponding author: pinsu@faculty.nctu.edu.tw).

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II. Results and Discussion

In this letter, the UTB devices are designed with 50nm nominal gate length (i.e., L = 50 nm unless otherwise specified), 50nm gate width (W), 1nm equivalent oxide thickness (EOT), 15nm channel thickness (T_{ch}), and 15nm BOX thickness (T_{BOX}). The channel, source/drain, and Si-substrate (p-type) doping concentrations are 10^{15} cm^{-3}, 5×10^{19} cm^{-3}, and 10^{18} cm^{-3} [7], respectively. Abrupt junction between source/drain region and channel region is assumed. The transport model we employ is the classical drift-diffusion model with constant mobility model [11], [12], and the impact of interface trap is not considered. In this letter, the threshold voltage (V_T) is determined at a given current: $[100\ \text{nA}\times(\text{W/L})]\times(\mu_{\text{channel}}/\mu_{\text{Si}})$ where μ_{channel} represents the carrier mobility of the high-mobility channel [12].

Using TCAD simulation [11], Fig. 1(a) compares the DIBL characteristics for UTB SOI, GeOI, and $In_{0.53}Ga_{0.47}As$-OI n-MOSFETs. It can be seen that the GeOI device exhibits larger DIBL than the SOI counterpart because of its higher permittivity. However, the $In_{0.53}Ga_{0.47}As$-OI device exhibits worse DIBL than the GeOI counterpart ever though it has smaller dielectric constant ($\varepsilon_r = 13.9$) than Ge ($\varepsilon_r = 15.8$). Fig. 1(b) further compares the DIBL characteristics for the $In_{0.53}Ga_{0.47}As$-OI, $In_{0.53}Ga_{0.47}As$-OI with $\varepsilon_r = 11.7$ (the same dielectric constant as Si), and SOI devices under various body biases. It can be seen that, although the DIBL of $In_{0.53}Ga_{0.47}As$-OI can be improved by reducing the dielectric constant from 13.9 to 11.7, it is still significantly larger than that of SOI for a given V_{BS}. Note that in Fig. 1(b) the DIBL increases with more positive V_{BS} because more positive V_{BS} pulls the electron profile toward the back interface and thus reduces the gate control [13].

The anomalous DIBL characteristics shown in Fig. 1 can be explained by Fig. 2, which compares the profiles of the conduction band edge (E_C) along the channel-thickness direction between long-channel UTB $In_{0.53}Ga_{0.47}As$-OI and SOI devices at $V_{BS} = 0$V and $V_{GS} = V_T$. As indicated in Fig. 2, the slope of E_C (and thus the vertical electric field) in the channel region for the $In_{0.53}Ga_{0.47}As$-OI device is smaller than the SOI counterpart. This result infers that there exists an effective built-in forward body-bias in the $In_{0.53}Ga_{0.47}As$-OI

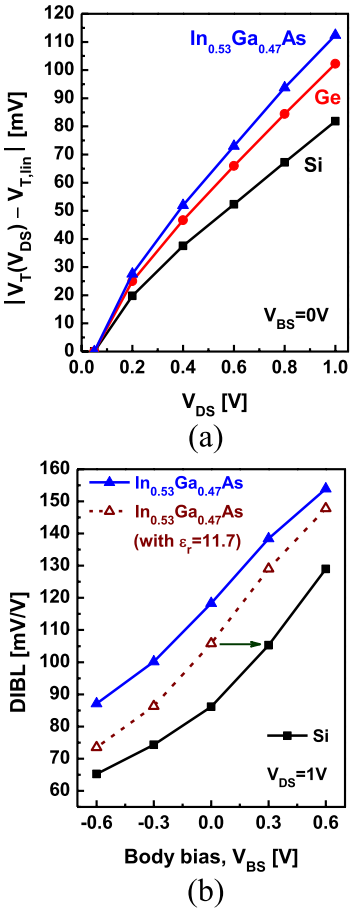

Fig. 1. (a) Comparison of the DIBL characteristics for UTB SOI, GeOI, $In_{0.53}Ga_{0.47}As$-OI n-MOSFETs. (b) Merely considering the impact of permittivity cannot explain the discrepancy in the DIBL versus V_{BS} characteristic between $In_{0.53}Ga_{0.47}As$-OI and SOI devices.

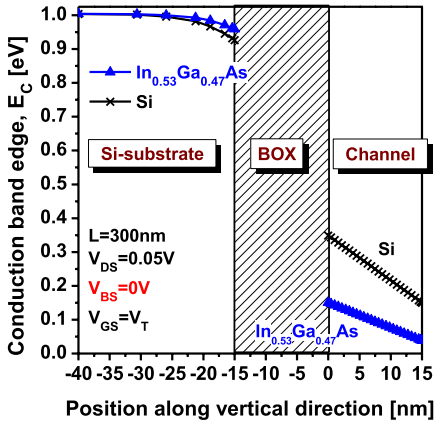

Fig. 2. Comparison of the E_C distributions along the channel-thickness direction showing the difference in vertical field (slope of E_C) between the $In_{0.53}Ga_{0.47}As$-OI and SOI n-MOSFETs. The two devices possess identical threshold voltage. This profile is extracted at the location where the minimum potential occurs for carrier flow along the channel-length direction (~L/2).

device (relative to the SOI device). This built-in effective body-bias ($V_{BS,eff}$) is intrinsic to hetero-channel MOSFETs with Si-substrate and can be expressed as (under classical approximation)

$$V_{BS,eff} = \frac{1}{q}\left(\chi_{ch}^{III-V} - \chi_{ch}^{Si}\right) + \frac{kT}{q}\ln\left(\frac{N_{C,ch}^{III-V}}{N_{C,ch}^{Si}}\right) \quad (1)$$

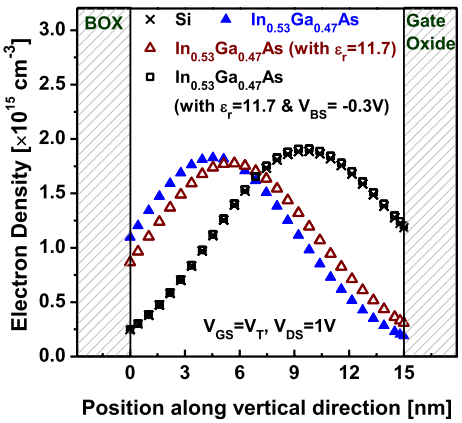

Fig. 3. After considering the impacts of permittivity and built-in effective body-bias effect, the channel electron profile for the $In_{0.53}Ga_{0.47}As$-OI device coincides with that of the SOI device. The electron density is evaluated at the location where the minimum potential occurs for carrier flow along the channel-length direction.

where kT/q is the thermal voltage, χ_{ch} the electron affinity for channel, $N_{C,ch}$ the effective density-of-states of conduction band for channel, and the superscripts *III-V* and *Si* represent the III-V-OI and SOI devices, respectively. Since $\chi_{ch} = 4.5$ eV and $N_{C,ch} = 2.08\times10^{17}$ cm^{-3} for $In_{0.53}Ga_{0.47}As$ [12] and $\chi_{ch} = 4.07$ eV and $N_{C,ch} = 2.85\times10^{19}$ cm^{-3} for Si, there exists a 0.3V built-in forward body bias in the $In_{0.53}Ga_{0.47}As$-OI device at room temperature based on Eqn. (1).

Fig. 3 compares the electron density distribution along the channel-thickness direction for the $In_{0.53}Ga_{0.47}As$-OI and SOI devices. It can be seen that the electron centroid of the $In_{0.53}Ga_{0.47}As$ channel is closer to the back interface (solid upper triangle), and the impact of dielectric constant is modest (open upper triangle). However, if the built-in $V_{BS,eff} = 0.3$V is further compensated by external body biasing, the electron profile of the $In_{0.53}Ga_{0.47}As$-OI channel (open square) shows a fairly good agreement with that of SOI. This validates the accuracy of Eqn. (1) and demonstrates that, in addition to permittivity, it is the built-in $V_{BS,eff}$ that determines the electron profile and thus the electrostatic integrity of the $In_{0.53}Ga_{0.47}As$-OI device.

Fig. 4 investigates and compares the impacts of the built-in $V_{BS,eff}$ on the DIBL of various high-mobility hetero-channel devices (InP, $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$, InAs, InSb, and Ge). The built-in $V_{BS,eff}$ of these hetero-channel devices are calculated by Eqn. (1) and listed in Fig. 4. It can be seen that while the $V_{BS,eff} = 0.3$V for $In_{0.53}Ga_{0.47}As$-OI nFET, the GeOI nFET possesses a reverse $V_{BS,eff} = -0.1$V. This explains why in Fig. 1(a) the $In_{0.53}Ga_{0.47}As$-OI device exhibits worse DIBL than the GeOI counterpart in spite of its smaller permittivity. Another anomalous DIBL characteristic is that the InSb-OI device exhibits smaller DIBL than the InAs counterpart even though its permittivity is larger. This can also be explained by the difference of their built-in effective body bias ($V_{BS,eff} = 0.349$V for InSb while $V_{BS,eff} = 0.705$V for InAs). Fig. 4 indicates that the impact of $V_{BS,eff}$ on DIBL characteristics can be larger or comparable to the impact of permittivity for III-V-OI n-MOSFETs.

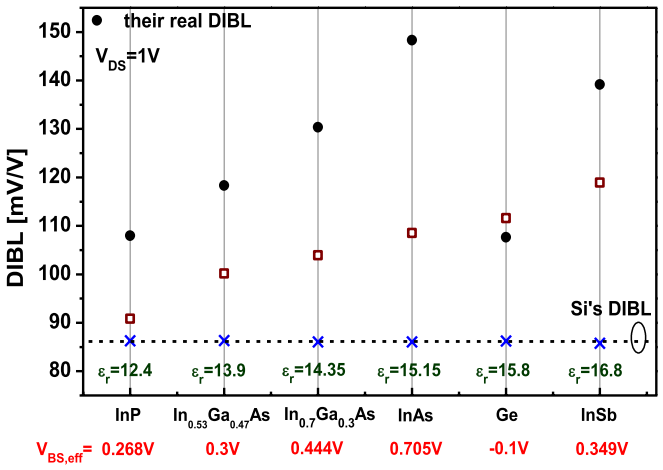

Fig. 4. Dissection of DIBL for various hetero-channel n-MOSFETs. The open square is obtained by applying external body biasing (with $-V_{BS,eff}$) to compensate the impact of the built-in $V_{BS,eff}$. The gap between solid circle and open square indicates the impact of $V_{BS,eff}$, while the gap between open square and blue cross indicates the impact of permittivity.

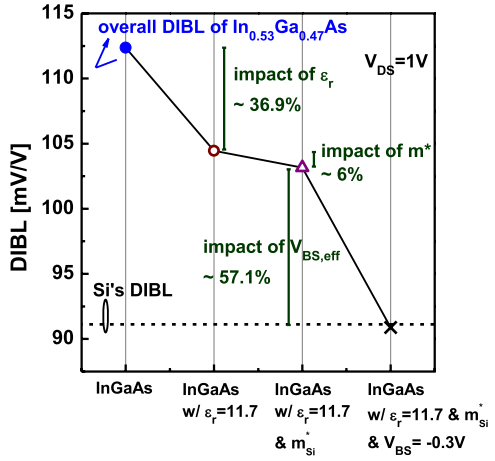

Fig. 5. Dissection of DIBL for the $In_{0.53}Ga_{0.47}As$-OI device under the quantum-mechanical condition. The gap between solid circle and open circle indicates the impact of permittivity (ε_r), the gap between open circle and the triangle indicates the impact of quantization effective mass (m^*), while the gap between the triangle and the cross indicates the impact of $V_{BS,eff}$.

The built-in effective body-bias effect, albeit reported in this letter under classical condition, is still present under the quantum-mechanical condition. In Fig. 5, we dissect the DIBL for the $In_{0.53}Ga_{0.47}As$ device by solving the Poisson-Schrödinger equations [11] (the quantization effective mass $m^* = 0.043m_0$ with m_0 the free electron mass and the nonparabolicity factor $\alpha = 1.24eV^{-1}$ [14]). It can be seen that the higher DIBL of the InGaAs device (as compared with the Si device) results from its ε_r, m^* and the built-in $V_{BS,eff}$, and the relative impacts of ε_r, m^* and $V_{BS,eff}$ are 36.9%, 6% and 57.1%, respectively. Note that without knowing the existence of the built-in effective body-bias effect, one can never explain the excess DIBL of the InGaAs device (the gap between the triangle and the cross).

It should be noted that for a given built-in $V_{BS,eff}$, a part of it may fall over the BOX and substrate depletion region. Therefore, its impact on DIBL may decrease for devices with thick BOX or light substrate doping. Besides, using Al_2O_3 (high-K) as the BOX material will increase the impact of the built-in $V_{BS,eff}$ on DIBL as compared with SiO_2.

III. Conclusion

We have reported a built-in effective body-bias effect in UTB hetero-channel III-V-OI n-MOSFETs. This effect results from the discrepancies in electron affinity and the effective density-of-states of conduction band between the III-V and conventional Si channels. In addition to permittivity, it is the built-in effective body-bias effect that determines the DIBL characteristics of the hetero-channel devices. This effect has to be considered when one-to-one comparisons among various UTB hetero-channel MOSFETs regarding the electrostatic integrity are made.

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