Suppression of the Boron Penetration Induced Si/SiO$_2$ Interface Degradation by Using a Stacked-Amorphous-Silicon Film as the Gate Structure for pMOSFET

Shye Lin Wu, Chung Len Lee, Tan Fu Lei, J. F. Chen, and L. J. Chen

Abstract— **This letter reports that the boron penetration through the thin gate oxide into the Si substrate does not only cause a large threshold voltage shift but also induces a large degradation in the Si/SiO$_2$ interface. An atomically flat Si/SiO$_2$ interface can be easily obtained by using a stacked-amorphous-silicon (SAS) film as the gate structure for p$^+$ poly-Si gate MOS devices even the annealing temperature is as high as 1000° C.**

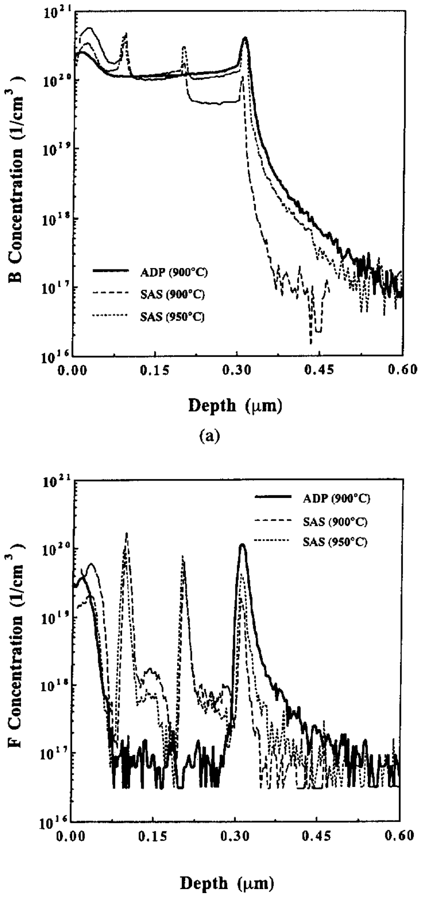
I. INTRODUCTION

RECENTLY, p$^+$ poly-Si has been widely used as the gate material of pMOSFET to avoid the short-channel effects [1]–[3]. The BF$_2$ ion implantation is typically used to form the p$^+$ poly-Si gate as well as the shallow p$^+$-n junction [3], Unfortunately, the F-incorporated p$^+$ poly-Si gate enhances the boron penetration through the thin gate oxide into the Si substrate and subsequently results in a large threshold voltage shift, a large charge trapping rate and a poor reliability of device [2]–[4]. Moreover, the more fluorine atoms pile up at the poly/Si/SiO$_2$ and Si/SiO$_2$ interfaces, the more serious the boron penetration effect occurs [5].

In this letter, from the observations of the high resolution transmission electron microscopy (HRTEM), it is found that the boron penetration through an ultra-thin gate oxide ($\leq$ 7 nm) into the Si substrate will also cause a drastic degradation in the Si/SiO$_2$ interface even the annealing temperature is as low as 900° C. This letter also proposes a stacked-amorphous-silicon (SAS) structure as the gate material of the p$^+$ poly-Si gate MOS device to suppress the boron penetration effect. An atomically flat Si/SiO$_2$ interface can still be obtained even the annealing temperature of the SAS gate is as high as 1000° C.

II. EXPERIMENTAL PROCEDURES

In this study, p$^+$ poly-Si gate MOS capacitors were fabricated on n-type (100) Si wafers with a resistivity of 5–20 Ω-cm. After a standard RCA cleaning process, all wafers were dipped in a diluted HF solution (1:50) to remove the native oxide. The wafers were loaded into the furnace at 600° C to reduce the thermal stress and to minimize the native oxide growth [6]. The temperature was gradually raised to 900° C in an N$_2$ ambient. After an N$_2$ pre-annealing stage for 60 min,



(a)

(b)

Fig. 1. The SIMS profiles of (a) boron and (b) fluorine of the 900° C-annealing p$^+$ SAS and ADP gate capacitors and the 900° C-annealing p$^+$ SAS gate capacitor.

Manuscript received October 22, 1993; revised January 15, 1993. This work was supported by the National Science Council of R.O.C. through research contract NSC82-0404-E009-190.

S. L. Wu, C. L. Lee, and T. F. Lei, are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

J. F. Chen and L. J. Chen are with the Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan, R.O.C.

IEEE Log Number 9400646.

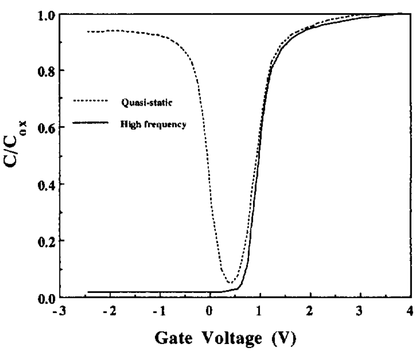


Fig. 2. The quasi-static and high-frequency CV characteristics of the 900° C annealing p$^+$ SAS gate capacitor.

an ultra-thin oxide of about 7 nm was grown in a dry O$_2$ ambient followed by annealing at the same temperature for 15 min in an N$_2$ ambient. An LPCVD amorphous silicon (α-Si) film with a total thickness of about 3000 Å was subsequently deposited at 550° C in three steps [7]. The deposition pressure and deposition rate were controlled at about 140–160 mtorr and 20 Å/min, respectively. The thickness of each α-Si layer was about 1000 Å. To make a comparison, the as-deposited poly-Si (ADP) film of about 3000 Å was deposited at 625° C in one step. The deposition pressure and the deposition rate were about 180–220 mtorr and 100 Å/min, respectively. Then, BF$_2$ ion implantation was performed at 50 keV with a dose of 6×10^{15} cm^{-2} and annealed at 800° C for 30 min in a dry O$_2$ ambient followed by driving-in at 850, 900, 950° C, and 1000° C for 15 min in an N$_2$ ambient. After aluminum metallization, all samples were sintered at 400° C for 20 min in an N$_2$ ambient to form a good ohmic contact.

The thickness of the ultra-thin oxide was determined by the high-frequency CV (HFCV) measurements by using the Keithley 590/595 CV analyzer and double checked by the HRTEM micrographs. The boron and fluorine profiles were analyzed by using a VG Ionex SIMS tool with an O$_2^+$ beam.

III. RESULTS AND DISCUSSIONS

Figs. 1(a) and (b) show the boron and fluorine profiles of the 900° C-annealing p$^+$ SAS and ADP gate capacitors and the 950° C-annealing p$^+$ SAS gate capacitor, respectively. For the p$^+$ SAS gate capacitors, due to the dopant segregation at the stacked-Si layer boundaries, the amount of boron and fluorine diffusion to the poly-Si/SiO$_2$ interface are less than that of the p$^+$ ADP gate capacitors. This is turn causes the boron and fluorine penetration through the thin gate oxide into the Si substrate for the p$^+$ SAS gate capacitors to be less than that of the p$^+$ ADP gate capacitor. It is noted that the amount of boron and fluorine penetration into the Si substrate of the 950° C-annealing p$^+$ SAS gate capacitor is even less than that of the 900° C-annealing p$^+$ ADP gate capacitor. Fig. 2 shows the quasi-static and the high frequency CV characteristics for the 900° C p$^+$ SAS gate capacitor. From these curves, it is seen that no gate depletion exists for this gate [8].

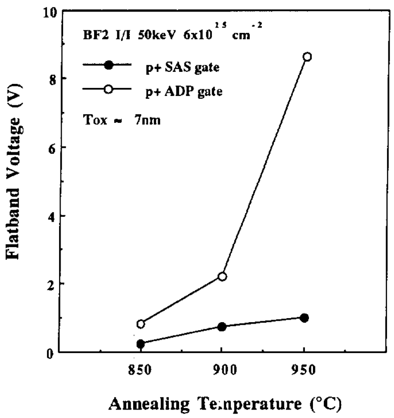
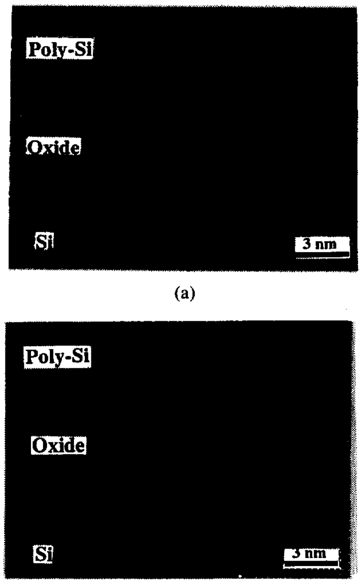


Fig. 3. The plot of the flat-band voltage (Vfb) vs. the annealing temperature of the p$^+$ SAS and ADP gate capacitors.



(a)

(b)

Fig. 4. The high-resolution TEM micrographs of (a) the 1000° C-annealing SAS gate structure and (b) the 900° C-annealing ADP gate structure.

Fig. 3 shows the plot of the flat-band voltage (V_{fb}) vs. the annealing temperature of the p$^+$ SAS and ADP gate capacitors. Due to the suppression of the boron and fluorine penetration into the ultra-thin gate oxide, the V_{fb} value of the 900° C- and 950° C-annealing p$^+$ SAS gate capacitors are 0.74 V and 0.99 V, respectively, while that of the 900° C- and 950° C-annealing p$^+$ ADP gate capacitors become 2.2 V and 8.6 V, respectively.

Figs. 4(a) and (b) are the HRTEM micrographs of the Si/SiO$_2$ interface of the 1000° C-annealing p$^+$ SAS gate structure and the 900° C-annealing p$^+$ ADP gate structure, respectively. It is seen that the Si/SiO$_2$ interface of the p$^+$ SAS gate structure is atomically flat. This result is consistent to that of the 900° C-annealing p$^+$ SAS gate and the n$^+$ poly-Si gate for the ultra-thin oxide prepared by using a low temperature wafer loading and N$_2$ pre-annealing process [6]. In contrast, the 900° C-annealing p$^+$ ADP gate structure has relatively rough Si/SiO$_2$ interface. Since both gate structures have the same ultra-thin oxide, the rougher Si/SiO$_2$ interface for the p$^+$ ADP gate structure is believed due to a large amount of the boron and fluorine penetration through the ultra-thin oxide into the Si substrate, as shown in Fig. 1.

IV. CONCLUSION

through an ultra-thin oxide ($\approx$ 7 nm) into the Si substrate cannot only cause a large flat-band voltage shift but also induce a drastic degradation in the Si/SiO$_2$ interface. An atomically flat Si/SiO$_2$ interface can be obtained by using the stacked-amorphous-silicon (SAS) gate structure even the annealing temperature is as high as 1000° C.

REFERENCES

[1] G. J. Hu and R. H. Bruce, "Design tradeoffs between surface and buried-channel FET's," *IEEE Trans. Electron Device*, vol. 32, pp. 584–588, 1985.

[2] C. Y. Wong, J. Y.-C. Sun, Y. Taur, C. S. Oh, R. Angelucci, and B. Davari, "Doping of n$^+$ and p$^+$ polysilicon in a dual-gate CMOS process," in *IEDM Tech. Dig.*, pp. 238–241, 1988.

[3] F. K. Baker, J. R. Pfiester, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, C. D. Gunderson, and L. C. Parrillo, "The influence of fluorine on threshold voltage instabilities in p$^+$ polysilicon gated p-channel MOSFETS," in *IEDM Tech. Dig.*, pp. 443–446, 1989.

[4] J. J. Sung and C. Y. Lu, "A comprehensive study on p$^+$ polysilicon-gate MOSFET's instability with fluorine incorporation," *IEEE Trans. Electron Devices*, vol. 37, pp. 2312–2321, 1990.

[5] H.-H. Tseng, M. Orlowski, P. J. Tobin, and R. L. Hance, "Fluorine diffusion on a polysilicon garain boundary network in relation to boron penetration from p$^+$ gates," *IEEE Electron Device Lett.*, vol. 13, pp. 14–16, 1992.

[6] S. L. Wu, C. L. Lee, and T. F. Lei, "Characterization of ultrathin oxide prepared by low-temperature wafer loading and nitrogen preannealing before oxidation," *J. Appl. Phys.*, vol. 72, pp. 1378–1385, 1992.

[7] S. L. Wu, C. L. Lee, and T. F. Lei, "High-performance polysilicon contacted shallow junctions formed by stacked-amorphous-silicon films," *IEEE Electron Device Lett.*, vol. 13, pp. 23–25, 1992.

[8] C. Y. Lu, J. M. Sung, H. C. Kirsch, S. J. Hillenius, T. E. Smith, and A. Manchanda, "Anomalous CV characteristics of implanted poly MOS structure in n$^+$/p$^+$ dual-gate CMOS technology," *IEEE Electron Device Lett.*, vol. 10, pp. 192–194, 1989.