InZnSnO-Based Electronic Devices for Flat Panel Display Applications

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This work demonstrates the versatility of amorphous InZnSnO (a-IZTO) oxide semiconductor, covering from the thin film transistor (TFT) to the resistive random access memory (RRAM) technologies for system-on-panel applications. The high-performance a-IZTO TFTs with effective carry mobility of 39.6 cm^2/V s, threshold voltage of -0.28 V and subthreshold swing of 0.25 decade/V are obtained in this study. Thermal post-annealing also was used to provide stable electrical characteristics with a few threshold voltage shift after positive gate bias stress. On the other hand, the RRAM device with a-IZTO film acting as active layer exhibits superior bipolar resistive switching characteristics. The wide ($>$10) resistance window and the stability endurance of hundreds cycle are achieved. Both of the proposed a-IZTO TFT and RRAM have promising potential to be integrated with a-IZTO-based periphery electronic circuits for flat-panel display applications.
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The system-on-panel (SoP) concept has been proposed to enable various functional devices, such as driver, sensor, memory and controller devices, to be integrated on a single panel for achieving high-performance, low-cost and more compact display products.[1,2] For the technology integration, several key electric devices, such as thin film transistor (TFT) and nonvolatile memory, are preferred to be fabricated with the same material and similar processes for manufacture with ease. In the SoP architecture, TFT devices are not only used to control the transmittance of the pixel, but also have to construct all the system circuits around the panel as basic switch or driver devices. In order to reduce the power consumption and scale down the bezel widths, the performance requirements of the TFT become critical especially on the mobility. Amorphous silicon, the most widely used material in TFTs as the channel layer, is suffering from the low mobility and leakage current. In 2004, the most popular material, amorphous indium gallium zinc oxide (a-IGZO), was proposed by H. Hosono et al. and attracted a lot of attention as a backplane material according to its transparency, high mobility and better bias stability.[3,4] However, the average mobility of a-IGZO TFTs is around 20 cm^2/V s and it's not enough to drive the circuits surrounded the display panel.[5,6] Besides, the high wet etching rate of a-IGZO, during the formation process of Mo or Al source (S)/drain (D) electrodes in PAN solution, causes the difficulty for fabricating a-IGZO TFTs with back-channel-etch (BCE) structure which is cheaper and simpler process than the etching stop one.[7–9]

The technology of memory device embedded in a display pixel can reduce power consumption and provide various functions for system driving circuits. The most popular nonvolatile memory, flash memory, has been widely used in many electronic products such as universal serial bus (USB), program-able logic circuit and radio-frequency identification (RFID).[10] However, the technology barrier for the integration of flash device on glass substrate is high since the flash device suffered from high programing voltage, long program/erase time and high process temperature.[11–13] The resistive random-access memory (RRAM), has been proposed as the promising alternative for the next generation non-volatile memory (NVM) application owing to its simple device structure, small size (4F^2), low programming voltage ($\sim$1 V), high operating speed ($\sim$ns) and a potential for 3-dimensional stacking.[14,15] By choosing the suitable material for resistive switching layer, the high-efficiency RRAM devices can be even fabricated at room temperature for display panels.

In this study, we propose the high-performance TFT and RRAM by using amorphous indium-zinc-tin oxide (a-IZTO) as the active layer. The a-IZTO thin film is promising for achieving high mobility TFT and serving as the switching medium for the RRAM device. Because of the gallium atom acting as the carrier suppressor in IGZO system, is replaced by the tin atom, the carrier concentration could be higher leading to a higher mobility of a-IZTO TFTs. The optimized composition of IZTO was published by M.-G. Kim et al.[16] The electron transport through extensive *s*-orbital overlap between In^{3+} ion and Sn^{4+} ion can provide better conducting behavior in a-IZTO thin film. With Tin oxide in the a-IZTO thin film, the etch resistance of a-IZTO layer against chemical etchants, for the S/D electrode formation also can be enhanced and lead to a better etch selectivity to S/D electrodes.[9] The a-IZTO TFT resultantly has the potential to be integrated with a-IZTO RRAM as one of periphery circuits for SoP applications.

Experimental

The inverted staggered passivation-free a-IZTO TFT devices were fabricated on a thermal oxide capped n$^+$ heavily-doped silicon (Si) wafer. First, the RCA-cleaned n$^+$-type Si substrate was thermally grown a 100-nm-thick silicon-oxide (SiO$_2$) as gate dielectric layer in a thermal furnace. Then, a 10-nm-thick IZTO film was subsequently deposited on the SiO$_2$ layer by RF sputtering with a IZTO target (In:Zn:Sn:O = 4:1:4:15 at%) at the pressure of 3 mtorr. The argon and oxygen flow rate during the sputtering process was 10 and 0.1 sccm, respectively. Then, a 100-nm-thick InSnO (ITO) layer was formed by the RF sputtering acting as the source and drain electrodes. The devices were finally annealed at 400°C for half hour in a thermal furnace with nitrogen gas environment. All the deposited films were patterned by shadow mask. The RRAM devices with the titanium nitride (TiN)/titanium (Ti)/ IZTO /platinum (Pt) were fabricated at room temperature. The 50 nm-thick IZTO resistive switching layer was deposited on the Pt bottom electrode (BE) by the sputtering only with the argon flow rate of 10 sccm. A 20 nm-thick Ti and 30 nm-thick TiN top electrode was subsequently sputter-deposited and patterned through shadow mask with a diameter of 0.2 mm. For the material analysis, another group of samples was fabricated with a 30-nm-thick IZTO thin deposited on the glass substrate, for measuring the film structure by the X-ray diffraction (XRD) and the transmittance of IZTO film by the UV visible spectroscopy. All the electrical characteristics of
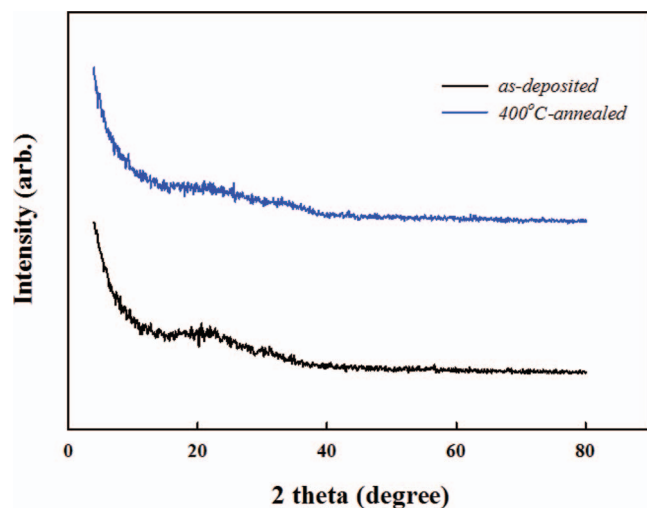
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Figure 1. X-ray diffraction spectra of a-IZTO film with and without 400°C thermal annealing.

a-IZTO TFT devices were measured by using the Keithley SCS 4200 semiconductor parameter analyzer.

Results and Discussion

Figure 1 shows XRD spectrum of IZTO thin films with and without 400°C post-annealing. From both of the spectra, there is no any sharp peak for the as-deposited and 400°C-annealed IZTO thin films. It indicates that the as-deposited film was amorphous type and will not be crystallized even after the thermal annealing at 400°C. The rough peak at 22° is the signal of glass substrate, which is not relative to the IZTO thin film. This amorphous characteristic of IZTO film can improve electrical uniformity of TFT devices.

The optical transmittance of 30 nm-thick IZTO thin film after 400°C thermal annealing is shown in Fig. 2. The a-IZTO film has high optical transmittance over 80% at the visible light regions and decreased to 40% with decreasing the wavelength down to 300 nm. The inset plots the relationship of $(\alpha h\nu)^2$ versus $h\nu$, and the optical bandgap of a-IZTO was extracted by using the Tauc model as the following:[17]

$$(\alpha h\nu)^n = D(h\nu - E_g)$$

where α is the absorption coefficient, $h\nu$ is the photon energy, E_g is the optical bandgap and D is a constant. The constant n is usually equal to 2 for amorphous semiconductors. The absorption coefficient
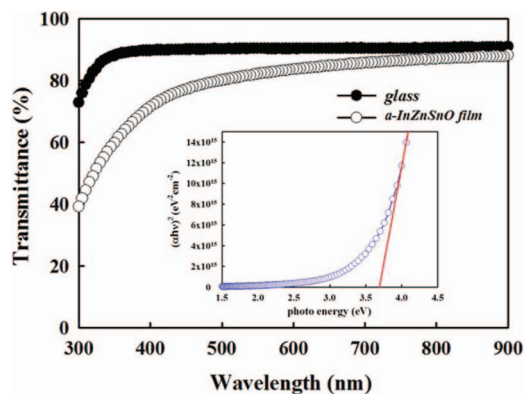

Figure 2. Optical transmission of 30 nm-thick a-IZTO film on glass after 400°C thermal annealing process. The inset plots the relationship of $(\alpha h\nu)^2$ versus $h\nu$ for the a-IZTO thin film.
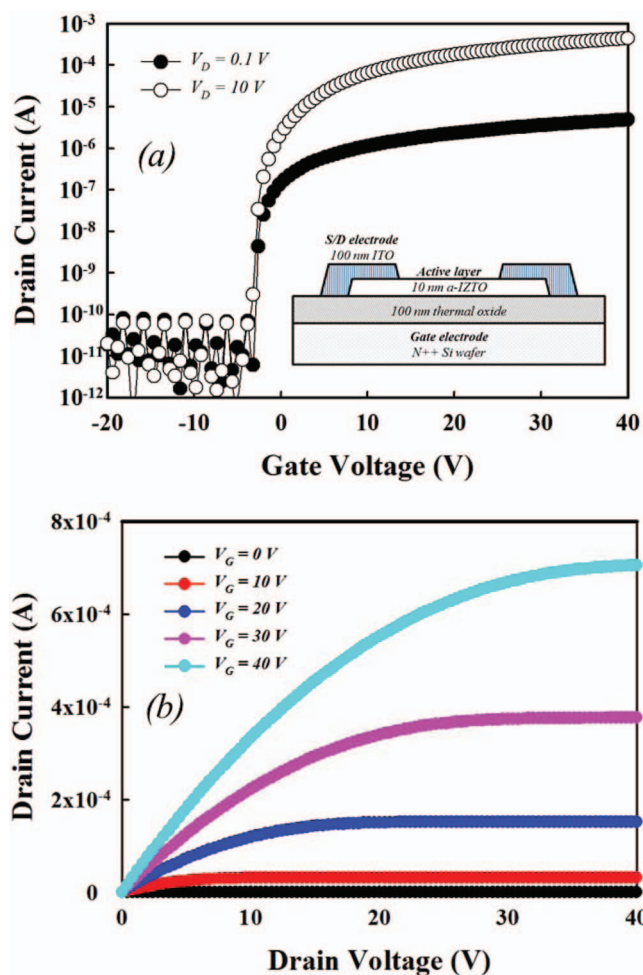

Figure 3. (a) I_D-V_G transfer characteristics of 400°C-annealed a-IZTO TFTs. The inset shows the schematic structure of inverted staggered a-IZTO TFTs. (b) I_D-V_D output characteristics of 400°C-annealed a-IZTO TFTs.

α can be obtained from the transmittance data by using the equation of $\alpha = (1/d) \times \ln(1/T)$, where d and T is the thickness and the transmittance of a-IZTO thin film, respectively. The optical bandgap of IZTO was 3.68 eV given by the intercept with $h\nu$ axis of the best fitting line. As for the photo light sensitivity of a-IZTO TFTs, we are still doing the research work on this topic and the completed results will be submitted soon to the journal.

Figure 3a shows the I_D-V_G transfer characteristics of 400°C-annealed a-IZTO TFTs. The field effect mobility (μ_{FE}) was extracted from the linear region with $V_D = 0.1$ V by the following equation:

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_D}$$

where the g_m and C_i is the transconductance and the gate capacitor per unit area, respectively.[18] The threshold voltage (V_{th}) is extracted from the constant current method which defined as the gate voltage corresponded to the normalize current at 10^{-8} A. The subthreshold swing (s.s.) is determined from the subthreshold region using the following equation:

$$s.s. = \left(\frac{d \log I_D}{d V_{GS}} \right)^{-1}$$

The μ_{FE}, V_{th} and s.s. of 400°C-annealed a-IZTO TFTs was 39.6 cm^2/V s, −0.28 V and 0.25 decade/V, respectively. The post-annealing process could enhance the structure relaxation and eliminate the defect states in a-IZTO thin film, which gained a higher mobility of a-IZTO
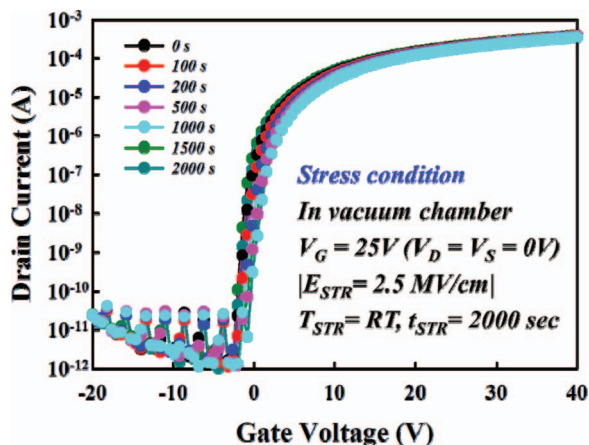
Figure 4. I_D-V_G transfer characteristics of 400°C-annealed a-IZTO TFTs after positive gate bias stress (PGBS) at room temperature with applying 25 V gate bias (2.5 MV/cm electrical filed) for 2000 sec.

TFTs than other published reports.[19,20] Also, the thermal energy could also improve the interface quality between gate insulator and a-IZTO layer, leading to a better value of s.s. than the one without post-annealing (not shown). Figure 3b shows I_D-V_D output characteristics of 400°C-annealed a-IZTO TFTs. From the region of small V_D, the drain current could increase linearly without any current crowding phenomenon. This indicated the contact resistance between a-IZTO channel layer and ITO S/D electrode was small. Also, the drain current saturated with 3×10^{-5} A has promising potential to provide a large driving current of devices for the applications of pixel switch and peripheral driver circuits.

Electrical reliability of a-IZTO TFT was studied with a gate bias testing, as shown Fig. 4. The a-IZTO TFT devices were applied a positive gate bias stress (PGBS) with the V_G = 25 V which equaled to 2.5 MV/cm electrical filed on the gate insulator for 2000 sec. The source and drain were grounded during the PGBS process. All the reliability test were measured in a dark vacuum chamber with the pressure of 5×10^{-5} torr to eliminate the ambient effects from the atmosphere such as oxygen and moisture. The V_{th} shift of device was about 1.96 V after the PGBS with slight degradation of s.s. and mobility. It was reported that the electrons trapped in the interface of a-IZTO /SiO$_2$ and the bulk of the a-IZTO channel layer dominated the degradation instead of the defect state creation.[21] With stressing the devices in an isolated vacuum chamber, the possibility of oxygen absorption at the back surface of the a-IZTO channel can be effectively excluded in this work. This measured device characteristics will be similar to the ones with a back channel passivation layer.

As for the application of a-IZTO film for RRAM device technology, Fig. 5 shows a typical bipolar current-voltage characteristic of IZTO RRAM device under dc sweeping mode at room temperature. In the beginning, the a-IZTO layer of RRAM device is gradually activated to form a conductive path, called the forming process. A sudden increase in current occurs at forming voltage, and the cell was transformed from high-resistance state (HRS) to low-resistance state (LRS). After sweeping the bias over the reset voltage around −1.5 V, an abrupt decrease in current was observed where the memory cell switches from LRS to HRS, called as reset process. Inversely, the cell turns back to LRS while applying a positive bias over the set voltage (~1 V), and a compliance current (I_{cc}) of 1 mA is assigned to prevent the permanent breakdown. Figure 6 shows the resistance-voltage curve, which clearly indicates the resistance window larger than ten at a reading voltage V_{read} = 0.2 V.

The cycling endurance of TiN/Ti/a-IZTO /Pt RRAM device is shown in Fig. 7. One cycle includes a single set process and a reset process. The set process is shown in Fig. 5 by the mark arrow 1 and 2, while the reset process by arrow 3 and 4. The resistance value of HRS and LRS were obtained at the reading voltage V_{read} = 0.2
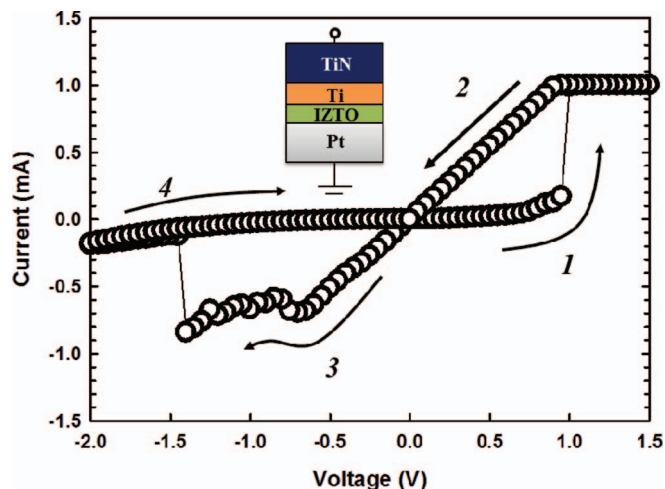

Figure 5. The typical bipolar resistance switching characteristics, including a set process indicated by arrow 1, and the reset process by arrow 3 and 4. The inset is showing a schematic plot of the a-AZTO resistive memory devices with titanium nitride (TiN)/titanium (Ti)/a-IZTO/platinum (Pt) structure.
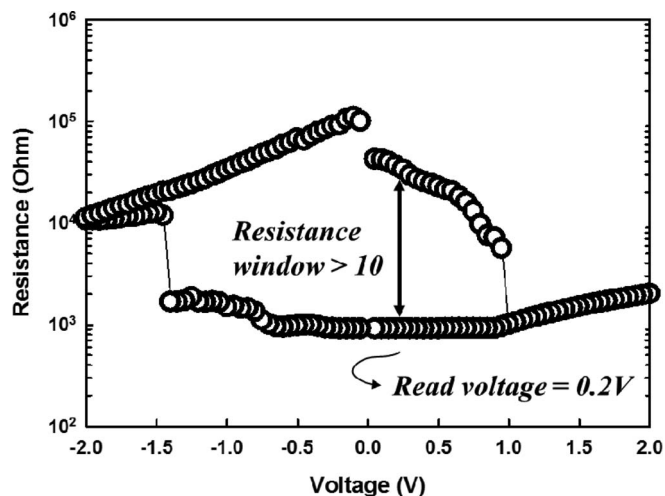

Figure 6. The resistance-voltage curve for the TiN/Ti/a-IZTO/Pt RRAM devices, which revealed the wide resistance window at the reading voltage.
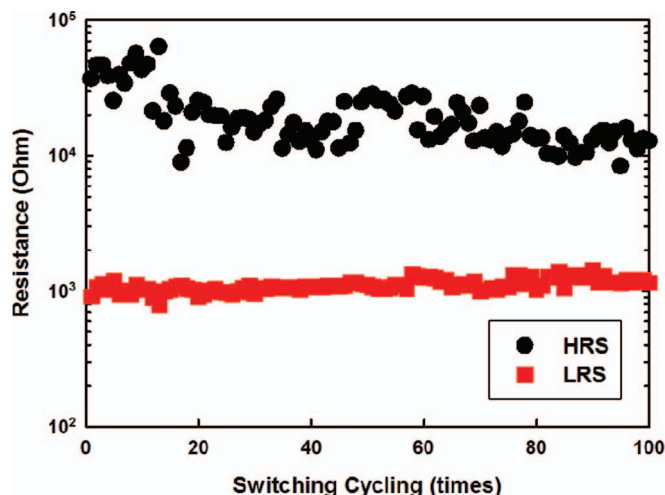

Figure 7. The stable endurance cycles of the TiN/Ti/a-IZTO/Pt RRAM device.
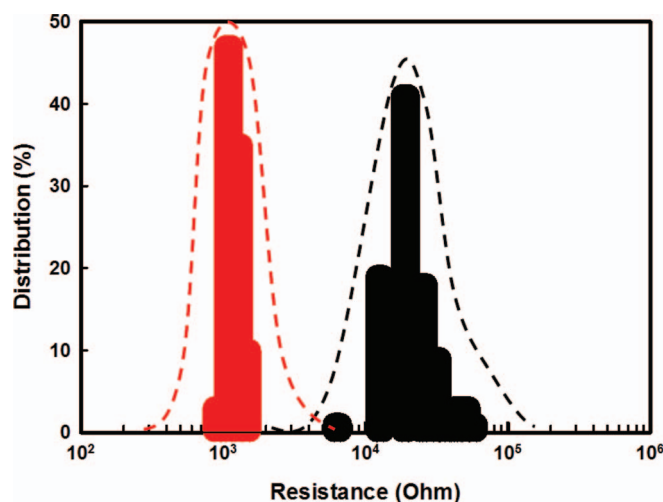
Figure 8. The statistical analysis of 100 times resistance distribution of the TiN/Ti/a-IZTO/Pt RRAM device.

V, respectively. The superior resistive switching characteristics, large (>10) resistance window, hundreds of cycle are revealed. Furthermore, the resistance distribution of the resistance switching events was analyzed, as shown in Fig. 8. It can be observed that a wide resistance window are exhibited, which is helpful for the operation of sense amplifier in a memory array technology.

The use of a-IZTO film as a nonvolatile memory channel will be easily integrated with the emerging a-IZTO TFT array technology in AMLCDs or AMOLEDs. The cross-sectional view of a-IZTO TFT connected to one RRAM cell structure is shown schematically in Fig. 9a, and the conceptual co-operation scheme for memory array application is shown in Fig. 9b. To set the cell to LRS, the selected WL, BL, and SL are biased at 10 V, 2 V, and 0 V. Since the unselected WL, BL and SL are biased at 0 V, 0 V and floated, respectively, the other cells will not be accessed and can sustain the previous states. The summary of operation conditions is also presented in Fig. 9c for set, reset, and read the 1T1R cell.

The advantages of IZTO-based RRAM include low programming voltage (<±2 V), low program/erase time (~100 ns),[22] low process temperature (nearly room temperature), small cell size ($4F^2$) and highly potential for ease integration due to its simple (metal/insulator/metal) structure. In addition, the a-IZTO-based
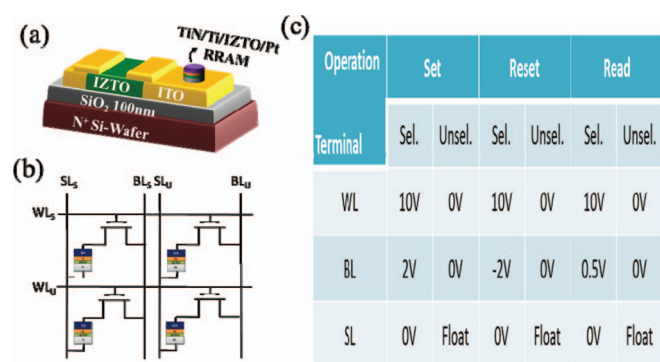
RRAM exhibits not only superior performance compared with the conventional RRAM,[14,15] but also has promising potential and beneficial for the low-cost technology to be integrated for system-on-glass applications.

Conclusions

In summary, InZnSnO-based electronic devices are studied for flat-panel display applications. The high-performance a-IZTO TFT exhibits superior electrical characteristics such as field effect mobility of 39.6 cm^2/V s, threshold voltage of −0.28 V and subthreshold swing of 0.25 decade/V. Also, the post-annealing process effectively reduces the defect states in a-IZTO channel layer and the interfacial ones between gate insulator and a-IZTO layers, leading to better electrical reliability with 1.96 V threshold voltage shift after PGBS. Furthermore, the TiN/Ti/a-IZTO/Pt RRAM devices show the attractive resistance switching behavior, including large memory window and high stability for electrical endurance. Finally, this work proposes a conceptual 1T1R memory array architecture associated with the operation scheme for the promising integration of a-IZTO-based TFT and RRAM devices.

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Figure 9. (a) The schematic cell diagram of one a-IZTO TFT connected with one a-IZTO RRAM. (b) The conceptual co-operation scheme for memory array application. (c) The summary of operation conditions for set, reset, and read processes for the 1T1R cell.

Operation	Set		Reset		Read	
Terminal	Sel.	Unsel.	Sel.	Unsel.	Sel.	Unsel.
WL	10V	0V	10V	0V	10V	0V
BL	2V	0V	-2V	0V	0.5V	0V
SL	0V	Float	0V	Float	0V	Float