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ORIGINAL ARTICLE

R.-H. Chen · C.-C. Chang · C.-M. Cheng

Fabricating a micromould insert using a novel process

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Abstract A new method of fabricating micromould inserts that is compatible with semiconductor manufacturing is proposed. Diffusion of phosphorous at a high temperature is first used to increase the electric conductivity of the surface of the silicon wafer to generate a silicon-based seed layer for electroforming. If the process temperature and the duration of doping with phosphorous are controlled, then the electric conductivity of this novel silicon-based seed layer can be expected to equal that of a metal seed layer. Then, a structure layer of amorphous silicon is successfully formed onto the silicon-based seed layer, by plasma enhanced chemical vapor deposition (PECVD). The structure layer has none of the defects that would be present if a metal seed layer were used to replace the silicon-based seed layer. Finally, a silicon-based master microstructure was created by using ICP-RIE to etch the structure layer. The silicon-based master has been demonstrated to be useable in successfully fabricating, by electroforming, a metal micromould insert with a large area and high aspect ratio.

Keywords Doping · Electroforming · ICP-RIE · Micromould insert · Microstructures · PECVD · Seed layer

1 Introduction

The fabrication of microstructures with high aspect ratios has received increasing interest in the field of microelectromechanical systems. The LIGA process, combining deep X-ray lithography, electroforming, and micromoulding, is particularly important. However, synchronization radiation is hard to obtain and the cost of an X-ray mask is high and the fabricating process is very complicated. The UV-LIGA process, combining UV-lithography, electroforming, and micromoulding, is highly compatible with the integrated circuit process. It is low-cost and the mask of it can be made easily. It is used to fabricate microstructures with high aspect ratios and to replace the traditional and expensive LIGA process. The electroforming process is a sub-process of LIGA or UV-LIGA process for fabricating metal microstructures. The electroformed mould inserts, whether high quality or not, are important in the subsequent micromoulding batch production [1, 2]. In the UV-LIGA process, the lithographed pattern plate is a three-layer structure. The bottom layer of the three-layer structure is a insulating base plate, such as a silicon wafer, glass, ceramic, or polymer. The middle layer of the three-layer structure is the conductive metal used as a seed layer in electroforming. The top layer of the three-layer structure is the photoresist pattern that has been lithographed. The seed layer for electroforming must have low sheet resistance and strong adhesion to the electroplate metal. The silicon wafer with seed layer formed by sputtering copper or evaporating titanium has a lower sheet resistance and initial current of electroforming than that deposited with other metals, so the processes of sputtering copper or evaporating titanium are extensively used [3]. However, the integrated circuit process is easily polluted by free electrons formed by sputtering copper or evaporating titanium, so neither sputtering copper nor evaporating titanium is compatible with the integrated circuit process. Accordingly, the concept of a microsystem that combines mechanical elements and integrated circuits is hard to be substantiated. In this work, the high-temperature diffusion process, which can be used to modify the sheet resistance of the silicon wafer and generate a silicon-based seed layer with the properties of both the base plate and the seed layer, is presented and compared with the traditional process of sputtering copper or evaporating titanium. The differences between the electroforming properties of the nickel microstructures formed by two processes are also analyzed. The new process presented here is developed to achieve economy and mass production.

R.-H. Chen (✉) · C.-C. Chang · C.-M. Cheng
Department of Mechanical Engineering,
National Chiao Tung University,
1001 Ta Hsueh Road, Hsinchu, Taiwan
E-mail: chenrh@mail.nctu.edu.tw

2 Fabricating the silicon-based master

Figure 1 shows the process of fabricating microstructures with high aspect ratios, as performed in this study. The fabricating

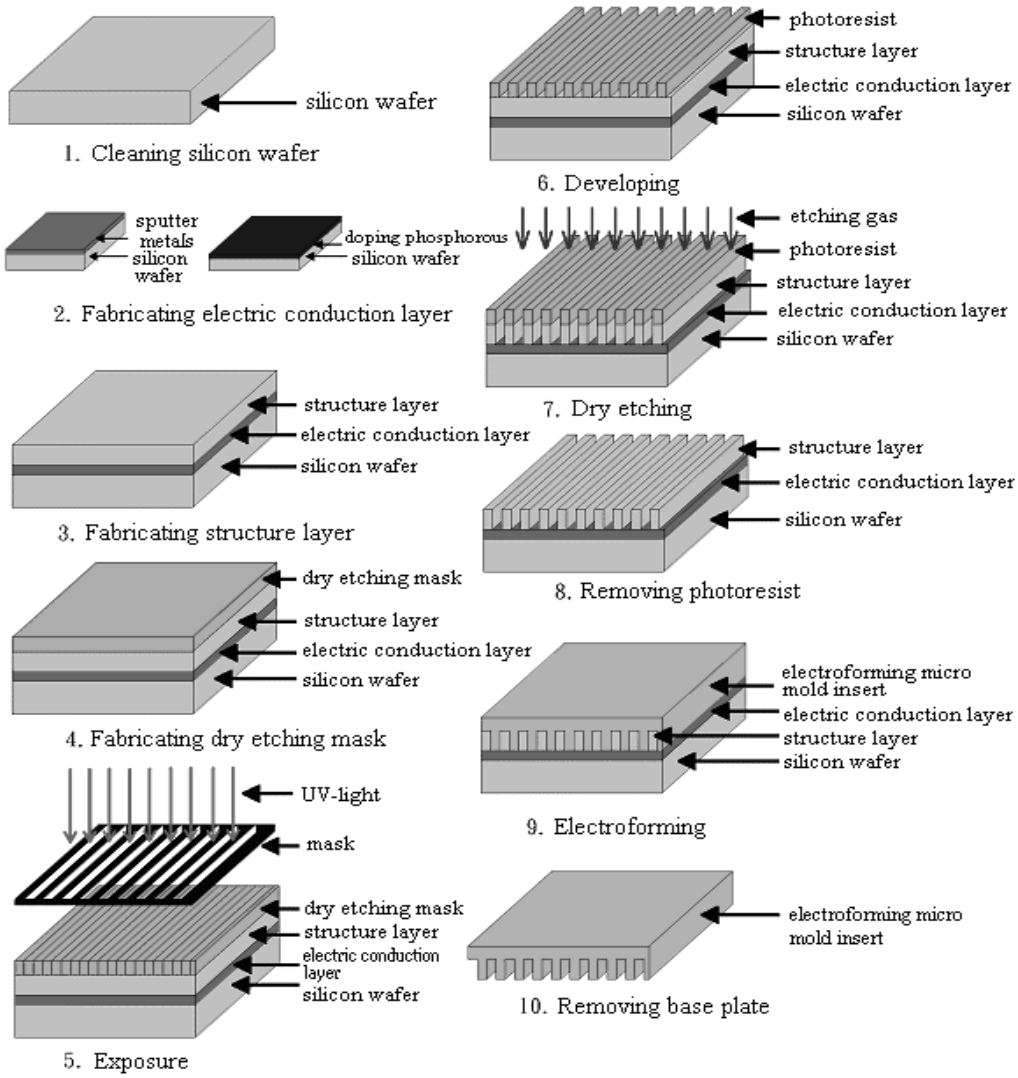


Fig. 1. The fabricating process of high aspect ratio microstructures

processes and properties of the seed and structure layers are as follows.

2.1 Fabricating the seed layer

The electrically conducting seed layer is made for performing electroforming. In this work, two kinds of seed layers were made: a metal seed layer used in traditional electroforming and a silicon-based seed layer proposed herein. In traditional electroforming, sputtering, evaporation, and silvered mirror reactions are used to fabricate the seed layer. This paper proposes the method of high-temperature diffusion to modify the sheet resistance of a silicon wafer for use as a seed layer; this method involves the high-temperature diffusion of phosphorous atoms into the silicon wafer. Phosphorous is a pentad, and so a phosphorous atom has one more electron than an atom of pure silicon. The conductivity σ of semiconductor materials, or the sum of the conductivities of the electrons in the conduction band and the holes in the valence band, is

$$\sigma = \sigma_{\text{electron}} + \sigma_{\text{hole}} = n_{\text{e}} \times q \times \mu_{\text{e}} + n_{\text{h}} \times q \times \mu_{\text{h}}, \quad (1)$$

where σ_{electron} and σ_{hole} are the conductivities provided by the electrons in the conduction band and the holes in the valence band, respectively, n_{e} and n_{h} are the numbers of electrons in the conduction band and holes in the valence band, respectively, μ_{e} and μ_{h} are constants of the material, and q represents electronic charge [4]. As shown in Eq. 1, when the number of electrons in the conduction band increases, the conductivity increases and can exceed that of the original pure silicon wafer. An increase in the diffusion temperature drives the electrons up into the conduction band, reducing the sheet resistance of the silicon wafer. Figure 2 presents the relationship between the sheet resistance of the silicon wafer and the process temperature of phosphorous diffusion. The figure implies that as the process temperature increases, the sheet resistance of the silicon wafer falls. When the process temperature increases to 1000 °C, the sheet resis-

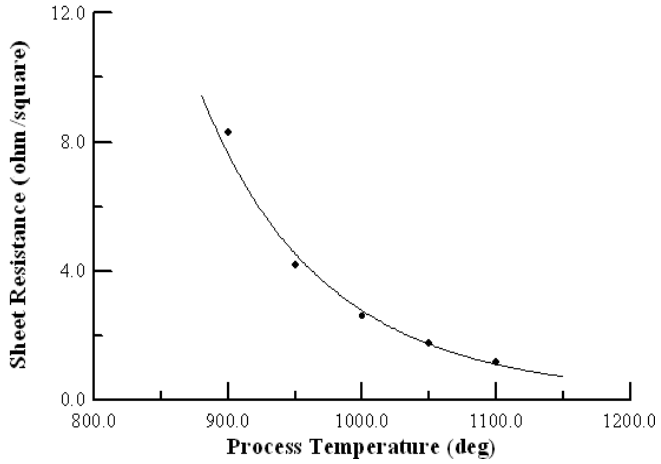


Fig. 2. Effect of diffusion process temperature on the sheet resistance of silicon wafer (with spline curve fitting)

tance of the silicon wafer falls to 2.59 ohm/square, reaching the sheet resistance required for electroforming. When the process temperature is 1100 °C, the sheet resistance of the silicon wafer falls to 1.16 ohm/square, equaling the sheet resistance of a wafer on which the seed layer is made by sputtering copper. Additionally, when the process temperature reaches a certain threshold, and all the donor electrons in the donor lever are excited into the conduction band, increasing the concentration of impurity atoms (phosphorous atoms) to replenish the donor electrons also contributes to the fall in the sheet resistance of the silicon wafer.

Figure 3 plots the measured surface doping concentration of the phosphorous atoms on the silicon wafer due to diffusion of those atoms for 30 min at a process temperature of 900 °C, as determined by secondary ion mass spectrometry (SIMS) [5]. The x-axis represents the depth from the surface of the silicon wafer. The primary y-axis (on the left) represents the concentration of the element; the secondary y-axis (on the right) represent the number of secondary ions. This figure shows that from the surface of the silicon wafer to a depth of 0.4 μm, the density of

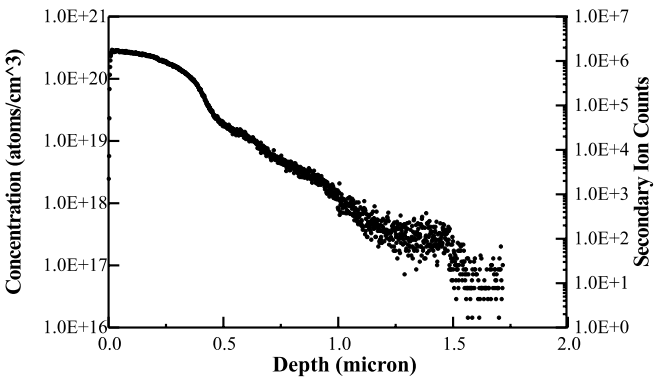


Fig. 3. The measured result of surface doping concentration of phosphorous atoms by using SIMS, with process temperature at 900° and a duration of 30 min

phosphorous atoms is much more than 10^{20} atoms per unit volume (cm^3), so the silicon wafer is sufficiently conductive for electroforming. This finding also implies that, when dry etching is used to etch the structure layer on the silicon wafer, the maximum depth of allowable over-etching is 0.4 μm.

Figure 4 plots the relationship between the temperature of doping and the allowable depth of over-etching. For given duration of the process, a higher temperature produces more deeply doping phosphorous atoms, or enables deeper over-etching to be tolerated.

Figure 5 plots the relationship between the thickness of chromium film, which is prepared by sputtering, and the sheet resistance of the silicon wafer. The sheet resistance of the silicon wafer decreases as the thickness of the chromium film increases. However, in fact, the internal stress should increase with the thickness of the chromium film. Table 1 presents the sheet resistance of the silicon wafer obtained using various methods for forming the seed layer. A seed layer made by the diffusion of phosphorous atoms can exhibit a lower sheet resistance than one

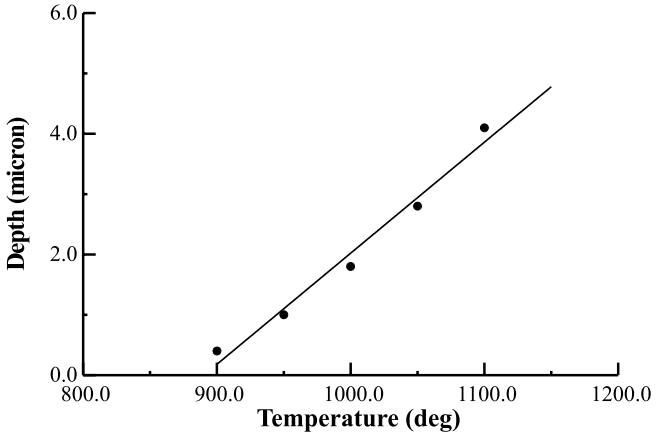


Fig. 4. Diffusion process temperature versus allowable over-etching depth (with least square linear fitting)

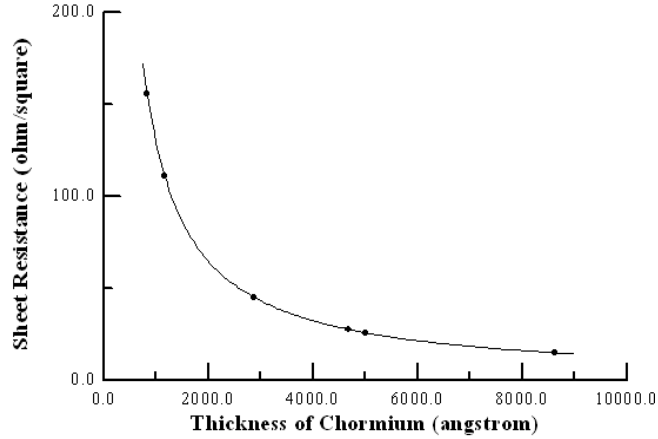


Fig. 5. Thickness of chromium film versus sheet resistance (with spline curve fitting)

Table 1. The sheet resistance of base plate under various fabricating methods

Base plate conditions	Sheet resistance (ohm/square)
Copper sputter 1100 Å	15.36
Copper sputter 2700 Å	1.69
Aluminum evaporate 5000 Å	0.08
Chromium evaporate1160 Å	111.12
Chromium evaporate 4500 Å	27.59
Chromium evaporate 5000 Å	25.79
900°, phosphorous atoms diffuse 30 min	8.90
900°, phosphorous atoms diffuse 60 min	8.29
950°, phosphorous atoms diffuse 60 min	4.18
1000°, phosphorous atoms diffuse 60 min	2.59
1050°, phosphorous atoms diffuse 60 min	1.75
1100°, phosphorous atoms diffuse 60 min	1.16

made by sputtering or evaporating metals. In particular, as well as exhibiting similar electric properties as a seed layer made by sputtering or evaporating metals, the silicon-based seed layer is also compatible with integrated circuit processes.

2.2 Fabricating the structure layer

This work uses plasma enhanced chemical vapor deposition (PECVD) to deposit amorphous silicon as a structure layer on the seed layer. When the structure layer is fabricated using PECVD, the type of seed layer on the base plate can strongly influence the structure layer.

Aluminum and silicon wafers undergo solid-state dissolution at 400 °C, so if the original seed layer for electroforming is prepared by sputtering aluminum on the silicon wafer, then the silicon atoms can migrate into the aluminum and the aluminum can fill the vacancies left by silicon diffusion during the fabrication of the structure layer by PECVD. If follow-up dry etching is performed, then pin residues will remain after dry etching. If titanium is used as the seed layer for electroforming, then it can form a chemical compound called titanium silicon ($TiSi_2$) with silicon at 500 °C during depositing the structure layer by PECVD. Because the adhesion of the electrically conducting titanium to the amorphous silicon structure is strong, even the thickness of the PECVD-deposited amorphous silicon remained at 4 μm; the layer does not peel off. However, the pin residues will remain after dry etching. Chromium used as the seed layer for electroforming yields a higher sheet resistance than aluminum and titanium, and a better result of depositing amorphous silicon by PECVD. Chromium raises the same problem of pin residues as aluminum and titanium in dry etching [6].

Using PECVD to fabricate a structure layer on a silicon-based seed layer, prepared by high-temperature diffusion, has a few advantages over using it to fabricate such a structure layer on a metal seed layer, as described above. The problem of pin residues will not occur when using PECVD to fabricate a structure layer of amorphous silicon on a silicon-based seed layer. Figure 6 plots the variations of internal stress with the thickness of the structure layers which are deposited, by PECVD, on a silicon-based seed layer and a sputtered seed layer of chromium, respectively. Before structure layer is deposited, chromium seed layer has an internal stress of -8×10^2 MPa, which is much higher than that in the silicon-based seed layer. After deposition of the structure layer is finished, the internal stress in the metal seed layer still exceeds that in the silicon-based seed layer.

2.3 Dry etching

After the structure layer is deposited, a photoresist is coated and lithography is used to define the pattern on the structure layer. Then, inductively coupled plasma-reactive ion etching (ICP-RIE) is employed to etch the structure layer of amorphous silicon. In this work, the etching gas is SF_6 and the passivation gas is C_4F_8. Two types of etching masks, photoresist and silicon dioxide, are used. Figure 7a presents the etching results obtained using photoresist as an etching mask material, and Fig. 7b presents the results obtained using silicon dioxide as the etching mask material. These figures reveal that more residues are obtained when photoresist is used as the etching mask; this problem can be solved by increasing the amount of reactive etching gas. Additionally, in narrow openings, sidewall profiles can lead to an uneven surface because of recurring etching and passivation gas exchange. The flow ratio and period of the etching and passivation gases, and the oxygen inflow can be adjusted to solve the problem of uneven surface and residues [7].

3 Electroforming process of metal micromould inserts

Nickel can be electroformed on a silicon-based master following dry etching, for comparing the electroforming property of using a silicon-based seed layer and using a metal seed layer. In this study, the electroforming solution used in nickel electroforming includes 420 ml/L nickel sulfamate, 40 g/L boric acid, 1 g/L saccharin, and 2 ml/L surfactant. Boric acid is used to stabilize the pH of the electroforming solution, and saccharin reduces the

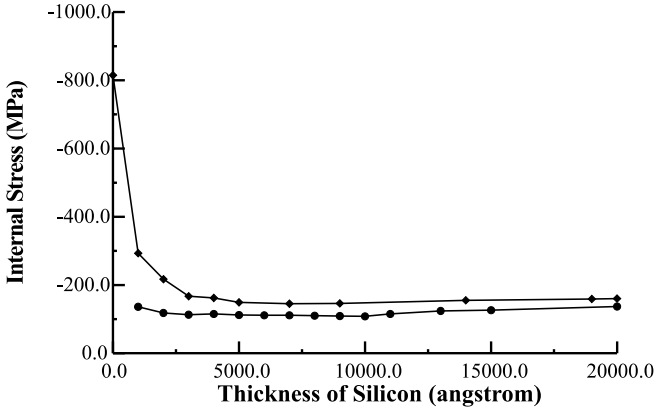
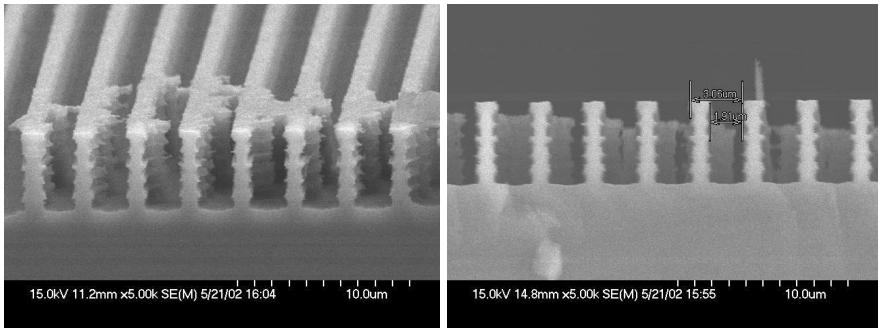
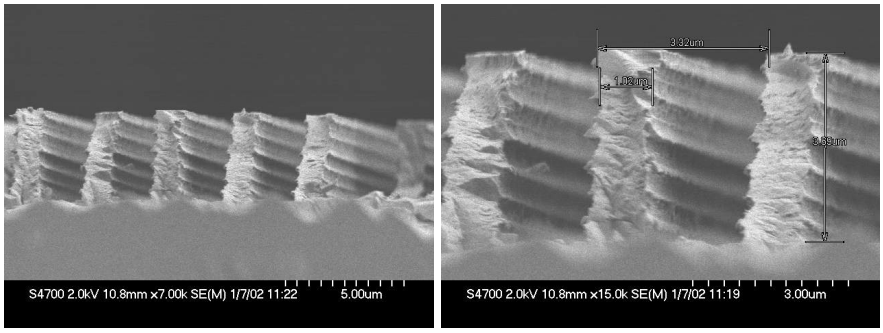


Fig. 6. Thickness of amorphous silicon versus internal stress under various seed layers of electroforming (high temperature diffusion process, traditional chromium process)

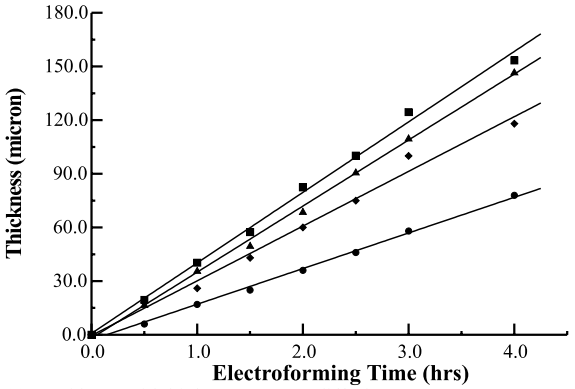


(a) Photoresist used as etching mask.

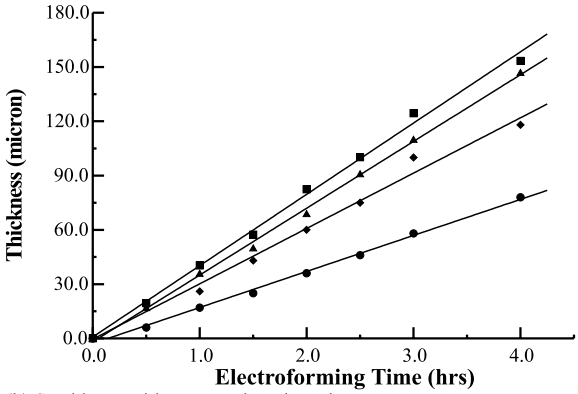


(b) Silicon dioxide used as etching mask.

Fig. 7a,b. The ICP etching results of various etching masks **a** Photoresist used as etching mask **b** Silicon dioxide used as etching mask



(a) Seed layer with high temperature diffusion process.



(b) Seed layer with evaporating chromium.

Fig. 8a,b. Current density versus the thickness of electroformed metal (●1ASD ♦2ASD ▲3ASD ■4ASD) **a** Seed layer with high temperature diffusion process **b** Seed layer with evaporating chromium

stress between the electroforming layers. During electroforming, the current density is maintained at 1 ASD to 5 ASD, the electroforming temperature between 40 and 60°, and the pH value between 3.8 and 5.2.

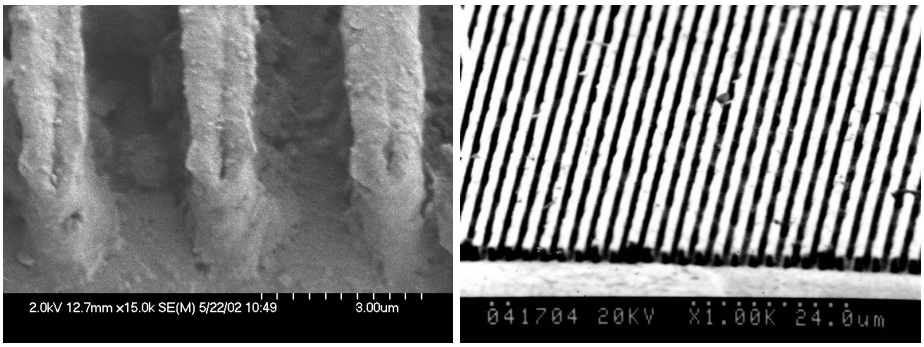
Figure 8 plots the variations of the thickness of the electroforming layers with time, when different types of seed layer are used. According to this figure, the thickness of the electroforming layers is related to the electroforming time and the current density, and is not related to the production method of the seed layer. Both seed layers display similar rates of deposition.

Table 2 plots the adhesive forces measured between various seed layers and electroforming layers under fixed electroforming conditions. Two types of seed layers do not significantly differ with respect to the adhesive force, given the accuracy of the measurement.

Figure 9a presents a top view of electroformed microstructures. This figure indicates that at the beginning of electroforming process, the metal is deposited onto two sidewalls rather than on the bottom surface of the base of the dry-etched microstructures, forming a weld line on the top of the elec-

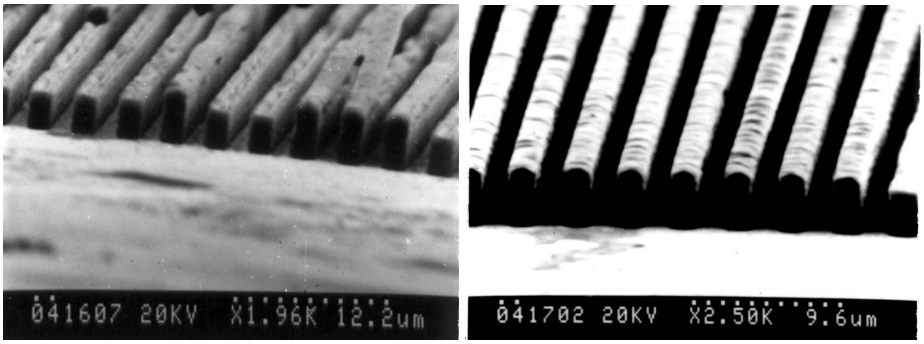
Table 2. Adhesive force existing between the seed layer and the electroforming layer

Seed layer	Current density (ASD)	Electroforming time (h)	Adhesive force (MPa)
Metal	1	8	2.24×10^{-2}
Silicon-based	1	8	2.25×10^{-2}



(a) High magnification (b) Low magnification

Fig. 9a,b. The top view of microstructures after electroforming Process, where the electroforming base plate used is a silicon-based electric conduction base plate **a** High magnification **b** Low magnification



(a) (b)

Fig. 10. The oblique-projection photographs of electroforming microstructures, seed layer used for electroforming is silicon-based

troformed microstructures. This phenomenon is considered to follow from the over-etching of the silicon microstructure and may cause the metal micromould inserts to become mechanically weak. Thus, although the allowable over-etching depth can facilitate dry etching, it should not be abused; parameters of the dry etching process should be accurately controlled. Figure 9b proves that a seed layer formed by high-temperature diffusion can successfully be used to electroform a large area of deep-trench microstructures. Figure 10 displays oblique-projection photographs of the electroformed microstructures obtained in this work. The aspect ratio of these microstructures is 2.78.

At last, the water solution of potassium hydroxide at 75° with a weight percent of potassium hydroxide 25% is used as an etching solution to remove the seed layer. The required etching time is 10 hours; however, it can be reduced to one hour to separate the seed layer from the metal microstructures if the covering metal at the rim of the base plate was already cut off. Figure 11a presents a metallurgical analysis of the cross-section of a nickel micromould insert that is electroformed using a silicon-based seed layer. Many triangles with directionality are observed. These triangles are verified by element analysis and magnified micrography, to be pores created by hydrogen generated during electroforming. Figure 11b depicts the use of an energy dispersive X-ray (EDX) spectrometer to perform an element analysis of the nickel micromould insert. The figure shows that the electroformed structure is pure nickel.

4 Summary

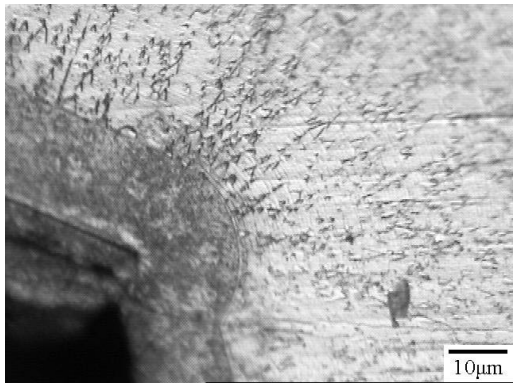
In this study, a silicon-based seed layer was formed and thin-film deposition, lithography, dry etching and electroforming were successfully performed to fabricate metal micromould inserts. The following conclusions are drawn:

(1) Fabricating the seed layer. The effect of the high-temperature diffusion of phosphorous to modify the sheet resistance of a silicon wafer can be altered by controlling the process temperature and increasing the concentration of the impurity atoms. Accordingly, a silicon-based seed layer with a similar or lower sheet resistance than that of a traditional metal seed layer can be obtained. Moreover, SIMS can be used to measure the surface doping concentration produced during high-temperature diffusion. The figure determined by SIMS shows the allowable depth of over-etching in dry etching.

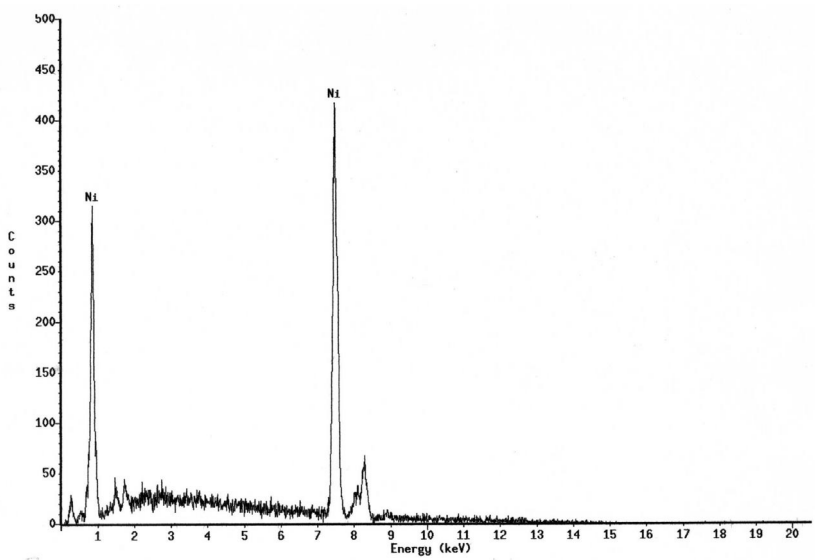
(2) Fabricating the structure layer. When PECVD is used to deposit amorphous silicon as a structure layer on the seed layer, the internal stress between the structure layer and a metal seed layer exceeds that between the structure layer and a silicon-based seed layer. Structure layers on a metal seed layer might peel off.

(3) Dry etching. Under the range of experimental conditions used herein, the sidewalls of the ICP etched microstructures are inclined at an angle of $2.64° \sim 2.67°$ to the vertical and the sur-

Fig. 11a,b. Material analysis of a metal micro mould insert which is electroformed by using silicon-based electric conduction base plate **a** SEM micrograph of the cross-section of a nickel micro mould insert (the dark part at the lower left corner is a cavity left by removing the base plate) **b** EDX analysis



(a) SEM micrograph of the cross-section of a nickel mi cro mould insert. (The dark part at the lower left corner is a cavity left by removing the base plate.)



(b) EDX analysis

face of the sidewall has uneven processing-traces with a depth of 0.2 μm.

(4) Electroforming. A silicon-based seed layer, fabricated by high-temperature diffusion, can yield the same or better electroforming results than obtained using a metal seed layer. Furthermore, in addition to being compatible with semiconductor manufacturing processes, the silicon-based seed layer is easier to be removed after electroforming than that is a metal seed layer produced by sputtering or evaporation. In this study, the microstructures of nickel micromould inserts produced in electroforming are 1 μm wide and 4 μm deep; they exhibited good duplication of silicon master microstructures.

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