THE POWER OF FUNCTIONAL SCALING

Beyond the Power Consumption Challenge and the Scaling Roadmap

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The relentless progress of silicon technology in the last few decades has been astounding, owing to device scaling. The characteristic lengths associated with successive generations of the technology have decreased, producing higher performance devices and circuits. At various times, people have predicted the end of scaling because of apparent barriers, but these barriers have fallen thanks to the ingenuity of the scientists and engineers involved in the technology. This has occurred through developments and changes in device design, the introduction of new materials, improved processing technologies and tools—both engineering and simulation— and other innovative approaches. The resulting increases in the densities of devices and their functionality in circuits now make the issue of power dissipation, both static and dynamic, a serious constraint to future scaling advances. In this article, a new very large scale integration (VLSI) structure is proposed and demonstrated to address these issues, using the three-dimensional (3-D) integration of high performance Ge-on-insulator (GOI) field effect transistors above conventional interconnects and Si devices.

POWER CONSUMPTION AND SCALING LIMIT CHALLENGES IN INTEGRATED CIRCUITS

The basic building-block of silicon technology, the metal-oxide-semiconductor field-effective transistor (MOSFET), shown schematically in Figure 1, has been down-scaled in its dimensions in successive technology generations. This scaling has been remarkably successful and sustained, yielding increased performance and circuit complexity but not at increased cost. Thus, scaling has been the driving force in Si microelectronics and will continue to be so [1], [2]. This has had a significant down side: the enormous capital costs of new state-of-the-art processing lines, which now have to handle 300-mm diameter wafers at a high volume to make them economically viable. Indeed, scaling might ultimately be limited as much by economics as by physics.

Scaling not only yields a higher integration density but also a higher transistor drive current and density for faster switching speeds ($I_d/C_{load}V_d$) in integrated circuits (ICs). The reduction in device dimensions increases the probability of tunneling, for example through the gate oxide, between the source and drain, and between the body and drain. Since the drive current of a sub-100 nm scale MOSFET is proportional to the gate dielectric capacitance/area ($C_{ox} = \varepsilon_0\kappa/t_{ox}$), a higher drive current is obtained by scaling down the oxide thickness t_{ox}. This provides more efficient channel charge control by the gate voltage; i.e., higher transconductance. Unfortunately, this down-scaling of t_{ox} ($\sim$1.2 nm thickness in present technologies) also leads to a higher leakage

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current density, arising mainly from the quantum-mechanical direct tunneling through the gate oxide, as mentioned previously. This leakage current in highly integrated ICs threatens to be a serious problem for further scaling advances due to its exponential dependence on $t_{ox}[\sim\exp(-\beta t_{ox}/V_{ox})]$. Furthermore, the number of devices in a high-performance chip can now number in the millions, so power dissipation is a serious concern [3].

People have predicted the end of scaling due to apparent barriers, but these have fallen due to the ingenuity of the scientists and engineers involved in the technology.

Although there are efforts to reduce the gate leakage problem by using high dielectric constant (κ) dielectrics, other band-to-band tunneling sources become important as the scaling limit of CMOSFETs (<10 nm) is approached. This tunneling can be direct or indirect (between the channel and the body or between the source and drain) and will be unavoidable [3], [4]. These effects depend on the bandgap, which is fixed. The contributions to the tunneling current will also result in significant dc power consumption, similar to that from the gate–dielectric tunneling current. However, scaling below 10 nm is still several technology nodes behind beyond current ($\sim$65 nm transistor gate length) technology. It is worth noting that the ultimate barriers for scaling depend on the type of circuit application being considered; there is no single scaling limit, since the specifications and packaging may be very different for different products. For example, for high-performance (fixed, not mobile) IC applications, a bulky cooling system is feasible to remove the (static) heat arising from the gate leakage current, but this will eventually become less effective and lead to hot spots in the circuits. For mobile, low-power applications, getting rid of the heat is a much more demanding problem. Some relief may be provided in the short term by alternative device designs [1], such as FinFETs, but other approaches such as partially or fully depleted Si-on-insulator (SOI) devices are no panacea for the power dissipation issue.

Static power dissipation, as mentioned previously, is associated only with keeping a circuit on, not for performing any useful operations. For functioning high-density VLSI circuits, the ac power consumption in the parasitic capacitance ($CV^2f/2$) of the MOSFETs and back-end interconnects has to be added to get the total thermal dissipation. The ac power can be restrained by the operational voltage (V) and frequency (f) but this is at the expense of compromised performance. In fact, dynamic power consumption is the dominant factor for high-performance microprocessors, even after solving the dc power leakage from the gate dielectric [5]. Since high-performance circuits are often associated with high-power dissipation, future designers will not, therefore, be driven entirely by the "fastest implementations" but by those that are the most energy efficient implementations, since the highest performance implementation dissipates too much power [6].

The lower part of the schematic in Figure 2 (below the passivation layer) represents a typical 1-Poly-Si-6-Metal (1P6M) Si technology and its interconnects, which are common basic building blocks for modern VLSI ICs. The circuit delays in the interconnects, rather than in the active devices, may dominate the IC speed [7]. These interconnects consume ac power in high density ICs, where the trend is towards increasing operational frequency and interconnect density, especially for microprocessors and communication ICs. Although wireless and optical interconnects have been demonstrated, they mainly work for interchip interconnects [8] rather than addressing the ac power consumption issue. No clear solution or approach has been demonstrated, so far, to address this issue.

In this article, we describe and demonstrate a novel and effective way to address these difficult challenges; by using 3-D integration. Strictly speaking, a standard Si technology is 3-D already, but the active device layer is effectively two-dimensional (2-D) with the interconnects, which are the bulk of the fabricated structure, providing the 3-D aspect of the structure. What is meant here by 3-D integration is that there are active devices in a 3-D stack together with the underlying wafer. The fundamental challenge with such an approach is how to create a top layer of active devices without degrading the lower multiple layers of interconnects and Si MOSFETs. To overcome this problem and demonstrate the idea, we have used a low-temperature-processed GOI layer to fabricate metal-gate/high-κ dielectric/GOI CMOSFETs on top of the interconnects and CMOSFETs of a standard 0.18-μm 1P6M Si process. It is important to notice that, although there are other approaches to realize the 3-D structures, such as using chip-stacking technology (CST) [9] (essentially a packaging approach), the merit of our work is the potential high interconnect density provided by this wafer-level technology, rather than the large size from CST.

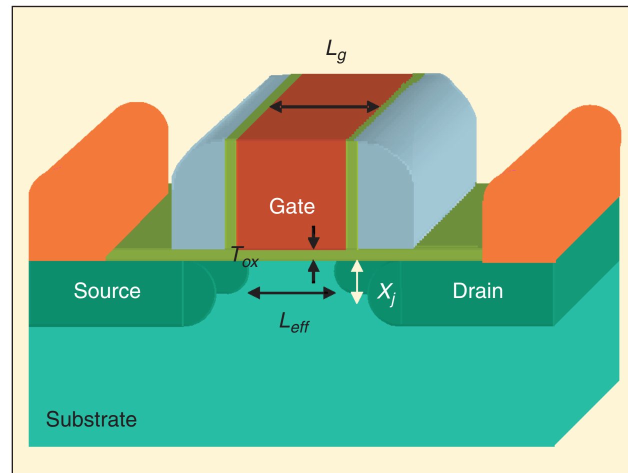
We find that the 3-D GOI CMOSFETs with dual-metal gates and a high-κ gate dielectric can reduce dc power consumption, because of $\sim$4 orders of magnitude lower leakage current. Electromagnetic simulations suggest that the ac power consumption and maximum operation frequency of ICs can also be improved using this 3-D architecture. The 3-D GOI transistors show at least twice the drive current of their Si counterparts. This is equivalent to a scaling of the Si devices, i.e., effectively extending CMOS scaling without confronting some of the difficulties associated with that process. We also believe the 3-D GOI/Si can provide a platform for system-on-chip (SoC) applications, where high-performance and low-loss radio frequency (RF) passive devices, such as transmission lines, inductors, filters, and antennas operating at up to 100 GHz, have been realized on Si. Since creating 3-D GOI/Si ICs is equivalent to down-scaling, it provides a potential solution for certain applications where developing a new processing line is exceedingly costly.

REDUCTION IN DC POWER CONSUMPTION USING NOVEL GATE-STACK MATERIALS

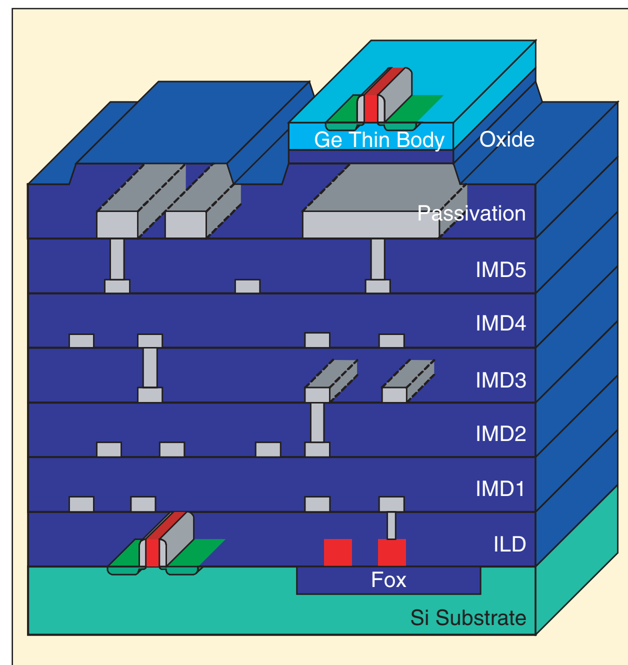
To overcome the dc power consumption and continue downscaling of the gate oxide thickness, use of a high κ metal-oxide instead of SiO_2 has been proposed [10]–[18]. Many laboratories are working on developing such materials to replace SiO_2, but it is a difficult challenge. Such materials can achieve a high $C_{ox}(\varepsilon_0\kappa/t_{ox})$ for high drive current, together with a low-leakage current, even for a relatively thick t_{ox}. An equivalent-oxide thickness (EOT = $t_{ox} \times \kappa_{SiO2}/\kappa_{dielectric}$) below 1 nm [11], [12], [19] has been reported using high-κ dielectrics, together with a several orders of magnitude lower leakage current. This reduction in the leakage current lowers dc power consumption and preserves the continuation of scaling. Figure 3 shows an example of $I_d - V_d$, $I_g - V_g$, and $C - V$ characteristics of self-aligned metal-gate/high-κ/Si CMOSFETs, using a high-κ $LaAlO_3$ gate dielectric and novel IrO_2 and IrO_2/Hf dual-metal gates. Since gate depletion increases the effective capacitative thickness, metal gates are an advantage as they do not show such depletion. The IrO_2 gate electrode has low resistivity and also a high work function. This is an alternative metal gate to fully silicided [16], [20], [21] and metal-nitride [18], [19] gates. Good $I_d - V_d$ characteristics for such CMOSFETs are shown in Figure 3(a). The gate dielectric leakage current in Figure 3(b) is ~4 orders of magnitude lower than SiO_2 at the EOT of 1.4 nm—as obtained from the $C - V$ measurement shown in Figure 3(c). This demonstrates the successful reduction of the dc power consumption arising from the gate leakage current, through the use of a high-κ gate dielectric and a metal gate. These devices are fully process-compatible with current VLSI technology.

$LaAlO_3$ is a novel high-κ gate dielectric with the unique property of retaining a high κ value ($\kappa = 25.1$), close to that for La_2O_3, even after combining the latter with Al_2O_3 ($\kappa = 10$). This is in contrast with a reduced κ value ($\kappa \sim 10$–15) for HfAlO(N) [13] and HfSiON [14], where HfO_2 ($\kappa \sim 22$) is combined with the relative lower κ Al_2O_3 or SiN ($\kappa \sim 7$). The $LaAlO_3$ is also widely available for superconductor applications. The addition of Al, Si, or N into HfO_2 helps improve the transistors' bias-temperature instability (BTI) [13], [14]. BTI is the undesirable increase of the threshold voltage (V_t) of a MOSFET during continuous operation at a temperature elevated by the thermal dissipation in the IC. The source of the BTI improvement may be the stronger bonding in these oxide or nitrides compared with ionic Hf-O bonds. We have found good BTI for the high-κ $LaAlO_3$ CMOSFETs, which indicates an allowable operation voltage of 1.2 V for a ten-year lifetime at 85 °C ambient temperature [17]. This meets the required 1-V operational requirement for nanometer-scaled CMOSFETs. The unique high-κ value and good BTI suggest that the $LaAlO_3$ ternary compound is one of the best high-κ gate dielectric choices.

The novel IrO_2 and IrO_2/Hf gate structures on $LaAlO_3$/Si CMOSFETs provide not only low leakage current [Figure 3(b)], but also appropriate work functions. Figure 4 shows the flat-band voltage (V_{fb}) as a function of EOT for IrO_2 and IrO_2/Hf dual gates on $LaAlO_3$/Si MOS capacitors. The 5.1 eV work function of the IrO_2 gate on a $LaAlO_3$/Si p-MOSFET is close to the value for Ir and to that for p^+ poly-Si gates. By combining Hf (work function: 3.5 eV) with IrO_2 on $LaAlO_3$/Si n-MOSFETs, the work function can be reduced to 4.4 eV. A challenge for metal-gate technology is the metallic out-diffusion into the gate dielectric. Metallic contamination of the SiO_2 gate dielectric on Si is well known to increase the dielectric leakage current and weaken the SiO_2 matrix. The low-leakage current in IrO_2/$LaAlO_3$/Si devices may arise from the



1. Schematic diagram of a MOSFET where some of the critical dimensions are reduced by scaling in successive technology generations. Typical requirements for MOSFETs are high drive current, low leakage current and high integration density.



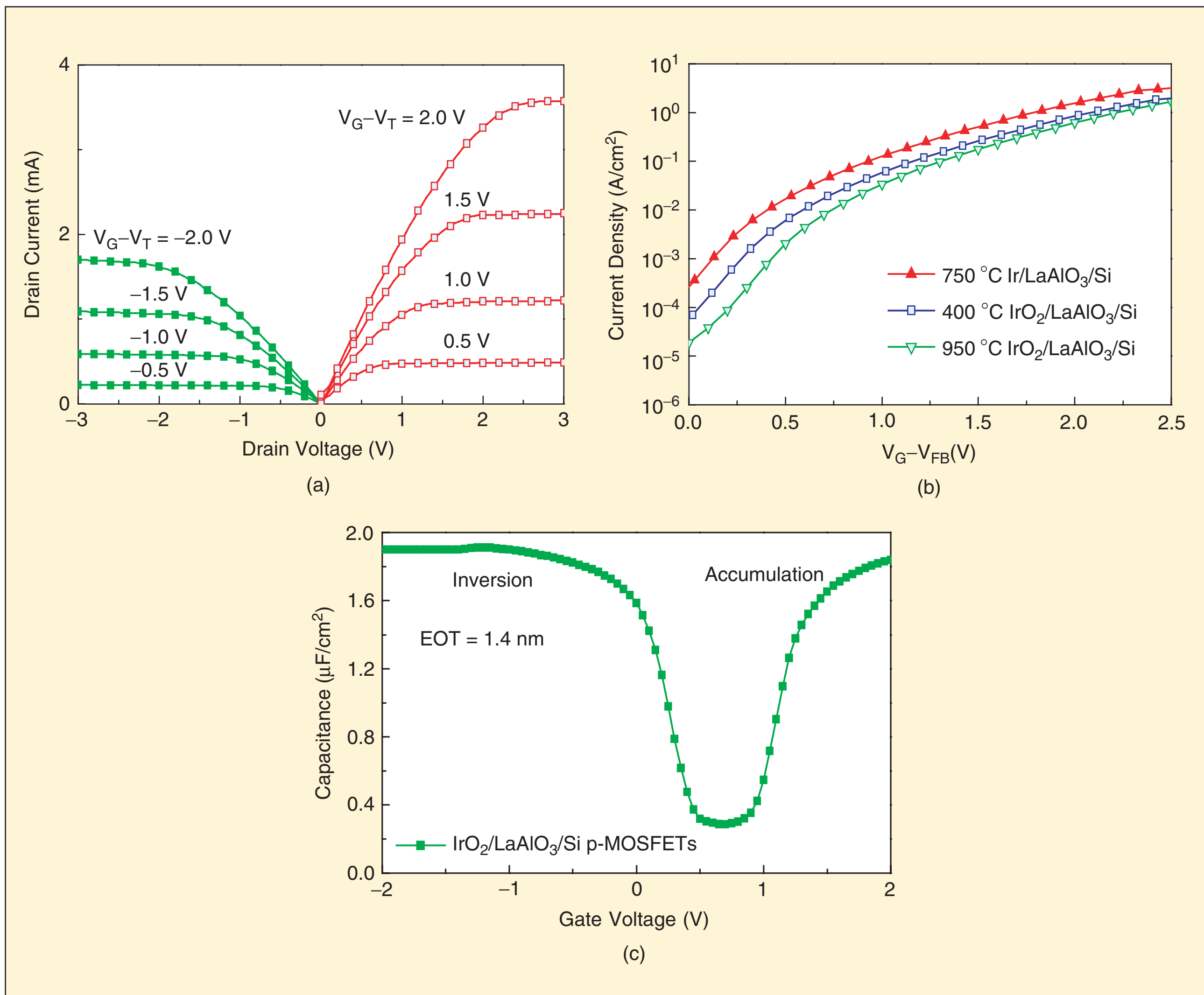
2. Schematic diagram of an IC structure with lower layer 1-Poly-Si-6-Metal Si CMOSFETs and top interconnect layers, below the passivation layer. The 3-D integration of a top metal-gate/high-κ/GOI CMOSFETs can address the challenges of dc power consumption from the gates leakage current, AC power consumption in the interconnects, and the scaling limits of 2-D CMOSFETs.

good match of the oxide-gate electrode and the oxide-gate dielectric, as well as the excellent metal diffusion barrier provided by IrO_2 [22]. This is shown by the $\sim 10 \times$ lower leakage current for an IrO_2 gate compared with a pure Ir gate [Figure 3(b)] and the four orders of magnitude lower gate leakage current compared with SiO_2 at an EOT of 1.4 nm.

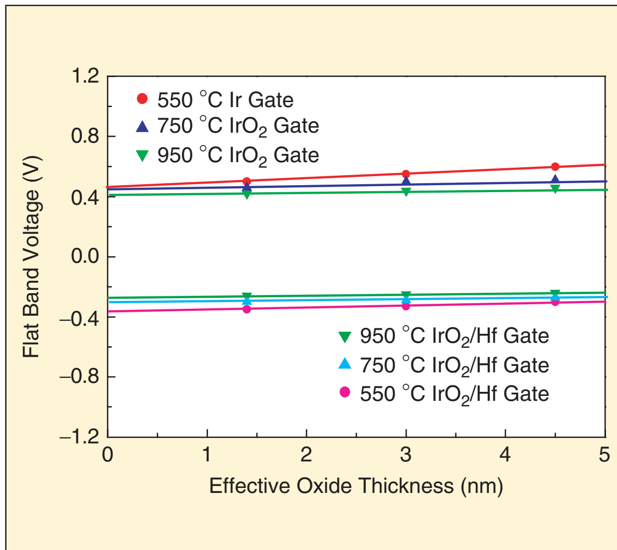
After implementing metal gates and high-κ dielectrics in future MOSFETs, the source-drain leakage current will be a dominating factor in dc power consumption. This can be mitigated by moving to FinFET device structures [2].

REDUCTION IN AC POWER CONSUMPTION BY 3-D INTEGRATION

Even after the dc power consumption from the gate leakage current of CMOSFETs has been reduced, the ac power then becomes a difficult challenge. The ac power consumption arises from both the MOSFET switching and the back-end capacitance ($CV^2f/2$). The reduction of the dynamic switching power of MOSFETs can be achieved by using an SOI wafer, permitting the junction capacitance to be reduced. For the ac power consumed in the back-end interconnects, we suggest that 3-D integration can help address this issue. We have used two parallel lines to simulate the parasitic capacitance effects in the complicated local and global interconnects, which are known to be the limiting factors for dynamic circuit switching speed. These effects become more severe with the scaling down of the interconnect distance. Figure 5(a) shows the schematic of a 3-D IC chip, where the interconnect distance, shown by the red lines, is reduced to 1/2 or even 1/4 by folding the 2-D IC into a 3-D structure once or twice. We have used an electromagnetic method to calculate the ac power consumption of the 3-D IC structure shown in Figure 2, where an additional layer of metal gate/high-κ/GOI CMOSFETs is fabricated above the 1P6M interconnects and lower layer Si devices. Figure 5(b) and (c) shows the calculated signal coupling loss (S_{21}) and power loss ($1 - |S_{21}|^2 - |S_{11}|^2$) from the scattering parameters. The highest IC operation frequency is determined by the 3-dB (50%) loss of the signal coupling or



3. DC characteristics such as (a) $I_d - V_d$, (b) $I_g - V_g$, and (c) $C - V$ characteristics for [IrO_2-IrO_2/Hf]/$LaAlO_3$/Si 2D CMOSFETs. The gate length was 10 μm.



4. *The flat-band voltage and EOT plot for IrO_2 and IrO_2/Hf gate on $LaAlO_3$/Si, after different RTA conditions, from 550–950°C.*

by the ac power consumption of high-density parallel metal lines. The operation frequency from the signal coupling loss decreases with decreasing line spacing, which then limits the interconnect density at high frequencies. We have used a 1-mm long line fabricated in a foundry with a 0.5-μm spacing to imitate complicated high-density interconnects. For this simulation, a maximum operating frequency of $<$20 GHz was obtained using the 3-dB signal coupling criteria. For further down-scaling, the interconnect spacing will become smaller and unacceptable in high density and high frequency 2-D IC, due to the coupling loss and cross-talk. The maximum IC operation frequency is also limited, by the ac power consumption, to 20 GHz for the 1-mm long, 0.5-μm spaced parallel lines. However, this can be increased to 40 GHz if a 3-D architecture, with an additional IC layer, is used. A much greater improvement of the ac power consumption—down to $\leq$0.25 dB at 40 GHz—can be achieved by using two additional IC layers above the lower 1P6M interconnects and Si CMOSFETs. This 3-D integration technology is the only known approach

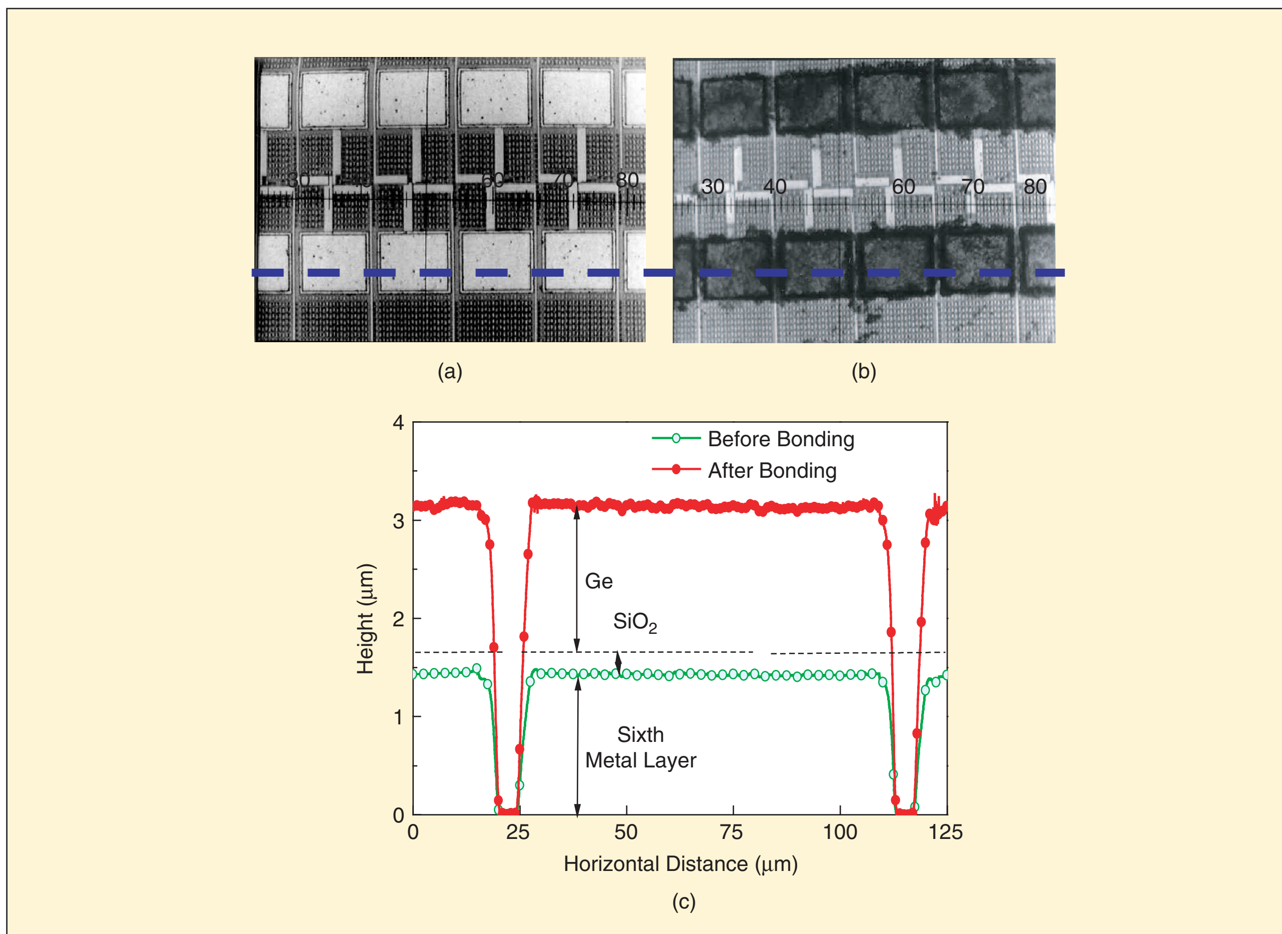
5. *(a) The schematic diagrams of a 3-D IC, (b) the coupling loss, and (c) the ac power loss from a 3-D electromagnetic calculation of 1-mm long parallel lines with various spacings and different lengths. The 3-D integration can decrease the 1P6M interconnect distance by 1/2 and 1/4, using one and two layers of GOI above the lower Si MOSFETs, respectively.*

to address the ac power consumption in the back-end interconnects, which is governed by the physics described by the term $CV_d^2 f/2$.

Increasing device densities in circuits have made power dissipation an issue that may seriously constrain future scaling advances.

The technological challenge is how to fabricate such 3-D ICs, as shown schematically in Figure 2, with a low thermal budget and small impact on the lower layer interconnects and Si devices. The metal-gate/high-κ/GOI CMOSFETs [15]–[17], with their 500 °C process, can meet the required low thermal budget; thus, it is ideal for creating the 3-D ICs on Si devices and multilayered interconnect structures. Therefore, we have fabricated self-aligned (IrO_2–IrO_2/Hf)/$LaAlO_3$/GOI CMOSFETs on 1P6M interconnects and 0.18-μm Si CMOSFETs. Figure 6(a) and (b) shows the top view and surface profile of a selectively formed thin-body GOI on the Si technology. The dark area on the probing pad after bonding and "smart cut" is the thin-body Ge layer, where a thickness of 1.6-μm was measured by surface profiling. The "smart cut" of the SiO_2/Ge is done using a 200-KeV hydrogen implant, which permits the separation/break at the peak of the implant damage concentration by using a mechanical stress, after heating the bonded Ge/SiO_2 on SiO_2/1P6M/0.18-μm Si CMOSFETs to 300–400 °C [15]–[17]. This method is widely used in SOI manufacturing.

We have measured the dc characteristics ($I_d - V_d$ and $I_d - V_g$) of the lower 0.18-μm Si CMOSFETs, which were beneath the 1P6M interconnects and found little degradation in their performance, since the GOI CMOSFETs are fabricated in a low-temperature process [17]. The $I_d - V_d$ characteristics for the 3-D (IrO_2–IrO_2/Hf)/$LaAlO_3$/GOI CMOSFETs are shown in Figure 7. In addition to good transistor characteristics, the drive currents of the 3-D metal-gate/high-κ/GOI n- and p-MOSFETs are 2.2 and 2.4 × higher than the Si CMOSFETs [Figure 3(a)], for the same 1.4-nm EOT metal-gate/high-κ structure. The higher drive current is especially important for achieving higher IC switching speeds ($I_d/C_{load}V_d$). The increase in a transistor's drive current is a significant factor in increasing the opera-



6. (a) The plan view of a 1.6-μm thin-body Ge that was scanned along the line and (b) the surface profile before and after Ge/SiO_2 bonding and "smart-cut."

tional frequency of ICs, under the same capacitive load (C_{load}) and drive voltage conditions.

It is important to note that the 500 °C processing is still too high for advanced back-end interconnects, which use low-κ dielectrics and Cu technology. Further reduction of the process temperature in the 3-D GOI approach could be achieved by using Schottky source-drain technology [23], which is currently under development.

Table 1. Comparison of GOI with SOI, SSDOI, HOT, and Intel's strained Si (local and mechanical strained Si).

	Mobility (IC Speed & Cost)	GaAs RF & Photonics & Defect	Added Cost
SOI	degraded	unable	none
SSDOI	improved	unable	Required epitaxy + yield issues from observed dislocations
HOT	improved, only in pMOS	unable	Selective epitaxy + mask
Intel's strained Si	improved, especially in pMOS (>50%)	unable	Source-drain epitaxy + mask
GOI	largely improved even with high-κ dielectric	ideal	Ge wafer bonding in GOI

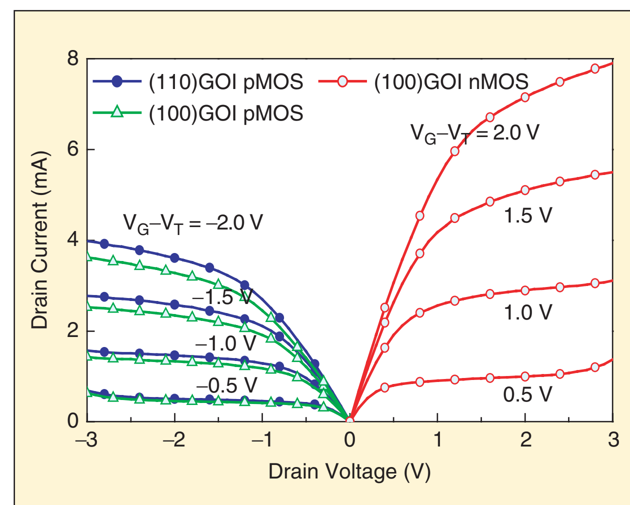
SCALING PERFORMANCE AND DENSITY WITHOUT TRANSISTOR SCALING

In Figure 8(a) and (b), we show, respectively, the electron and hole mobilities for IrO_2–IrO_2/Hf gates on high-κ $LaAlO_3$ dielectric and on 3-D GOI or 2-D Si CMOSFETs. In Si, both mobilities are lower than the universal values, which is typical for metal-gate/high-κ CMOSFETs [12]–[18]. The universal mobilities are those for SiO_2/Si CMOSFETs, which are limited by fundamental scattering mechanisms such as charge-, phonon-, and interface-roughness scattering. Note that the oxide-charge scattering of [IrO_2–Hf/IrO_2]/$LaAlO_3$/Si CMOSFETs arises from a charge density of $\sim 10^{11}$ cm^{-2}, as derived from the slope of the flat-band voltage and thickness plot in Figure 4. This low oxide-charge is comparable with that of the best metal-gate/HfO_2 MOSFETs [19]. Therefore, the mobility degradation is mainly due to an intrinsic property of the high-κ dielectric and the soft phonon scattering [19]. This arises from the ionic nature of the metal-oxide, which also provides the required higher κ value compared with that for SiO_2.

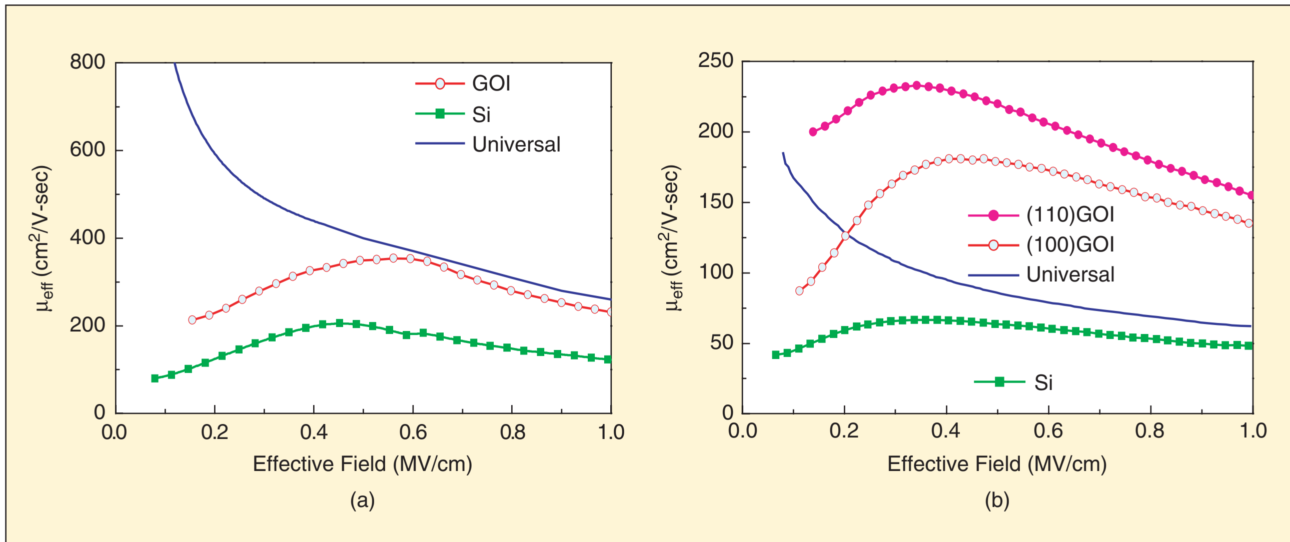
Strain can improve the electron and hole mobilities of Si MOSFETS [19], [21], [24]. For example, $\sim$50% increase in hole mobility has been reported for oxynitride gate dielectric p-MOSFETs [24] and 35% higher electron mobility in high-κ HfO_2 n-MOSFETs [19]. These higher mobilities are vital to achieve higher operation speeds and cheaper ICs [24]. Higher drive currents can also be obtained by down-scaling the CMOSFETs. Therefore, achieving higher mobility (mobility scaling) provides an alternative way of improving the transistor's drive current [12].

Higher electron (1.8×) and hole (2.7×) mobilities can be obtained in 3-D GOI CMOSFETs, compared with their Si counterparts having the same metal-gate/high-κ structure. The hole mobility can be increased even further (3.5×) using a (110) Ge substrate. This is similar to the hybrid- orientation technology (HOT) approach, which employs two differently oriented substrates [25]. These improvements for our high-κ gate dielectric CMOSFETs exceed those for strained Si [19], HOT [25], and strained-Si-directly-on-insulator (SSDOI) [26]. The higher electron and hole mobilities in GOI CMOSFETs can also provide the mobility scaling necessary to improve the switching speed and economics of ICs. The GOI structure reduces the off-state leakage current [17] arising from the small bandgap of Ge, which occurs in bulk Ge CMOSFETs. This is reminiscent of the lower off-state current in thin-body SOI devices. A low transistor off-state leakage current of 9×10^{-10} A/μm was obtained [17], which is still lower than the gate leakage current of modern ultra-thin gate dielectrics.

In Table 1, we compare various technologies for mobility enhancement. The HOT approach is better than strained Si and SSDOI, but does not improve the electron mobility. For the GOI method, both the electron and hole mobilities are improved, similar to SOI but without additional epitaxy, mask step, or dislocations. The GOI seems ideally-suited for integration with III-V RF and opto-electronic devices [32], [33], which are used in wireless and optical communications. Another inherent merit of GOI is its low processing temperature (500–550 °C), providing an excellent candidate for high-κ gate dielectric integration. In contrast, the much higher rapid thermal annealing (RTA) temperature (1,000–1,050 °C) for ion implantation activation of the source-drain of Si CMOSFETs produces difficulties for the successful integration of high-κ dielectrics.



7. The $I_d - V_d$ characteristics of the 3-D [IrO_2-IrO_2/Hf]/$LaAlO_3$/GOI CMOSFETs with a 1.4 nm EOT $LaAlO_3$ gate dielectric. The drive currents of the 3-D metal-gate/high-κ/GOI CMOSFETs are higher than those of the 2-D devices on Si [shown in Figure 3(a)] using the same metal-gate/high-κ structure. The gate length is 10 μm.



8. (a) The electron and (b) hole mobilities of IrO_2/15 nm-Hf/$LaAlO_3$ n-MOSFETs and IrO_2/$LaAlO_3$ p-MOSFETs on Si or GOI. The 3-D GOI CMOSFETs have 1.8 × larger electron mobility and higher hole mobility of 2.7 × for (100) Ge, or 3.5 × for (110) Ge compared with their 2-D Si counterparts.

The higher 3-D integration density and better transistor drive current of the top layer GOI CMOSFETs are similar to the results of a down-scaling process. The 3-D integration, with its lower interconnect density, cannot only reduce the ac power consumption but is equivalent to a continuation of CMOS scaling. Therefore, the 3-D integration scheme is an alternative to transistor scaling, which has rapidly increasing costs associated with it.

ICs WITH INCREASED FUNCTIONALITY

Future ICs that incorporate high-performance, low-power consumption device technology, will also be multifunctional. This will require the integration of RF as well as opto-electronic capabilities into the technology. Integration of the optical capability can be achieved by 3-D GOI; for instance, high-speed, high-efficiency photodetectors have already been demonstrated using GOI [27] The architecture of integrating 3-D metal-gate/high-κ/GOI devices on Si can also be used for high performance RF SoC applications, such as the integration of an RF transceiver with a CPU and chipset to produce a fully integrated solution. However, this requires high performance active MOSFETs [28] and passive RF devices [29]; although, the latter suffer from the substrate loss and poor quality-factor due to the low resistivity (10 Ω-cm) VLSI-standard Si substrates, which are far worse than semi-insulating GaAs substrates ($\sim 10^7$ Ω-cm) [29]–[30].

Because the 3-D GOI on Si architecture can use high resistivity Si (HRS) substrates to reduce the large substrate loss [31], high performance RF passive devices can be fabricated on the 3-D GOI/Si platform with the top Ge etched away. A drawback of this is that 12-in (300-mm) HRS substrates are not available. This can be overcome by using ion-implanted semi-insulating Si (10^6 Ω-cm) [29]–[30]. (The insulating characteristics arising from this technique are from the high trap density and deep trap energy produced in the Si substrate by the ion-implantation.) By incorporating high-RF performance passive devices, sub-terahertz aplications should be possible using the 3-D GOI/Si platform.

CONCLUSIONS

We have discussed the power dissipation problem in high-performance devices and ICs and shown that 3-D integration of novel Ge-based devices with standard Si devices can provide potential ways to address the dc and ac power consumption issues in advanced ICs. The higher 3-D integration density and higher drive currents obtained by using 3-D GOI CMOSFETs are equivalent to down-scaling of 2-D CMOSFETs. This approach may avoid some of the scaling limits. Low-cost 3-D integration can also address the rapidly increasing capital costs associated with sub-100 nm scaling. The low processing temperature of 3-D GOI and its excellent lattice-match with GaAs permits integration with III-V microwave and opto-electronic devices. We also suggest that the 3-D architecture of GOI/Si CMOSFETs may be suitable for high performance RF and SoC applications. Interest in pursuing the GOI approach has now been shown by IMEC, IBM, Applied Materials, Soitec and Silicon Genesis [32].

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