Flexible and Low Cost Design for a Flyback AC/DC Converter With Harmonic Current Correction

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***Abstract*—This study presents a new simple flyback ac/dc converter with harmonic current correction and fast output voltage regulation. In the proposed ac/dc converter, an extra winding wound in the transformer provides two key advantages. The size of the bulk inductor used in the conventional boost-based power factor correction cell can be significantly reduced in the proposed converter. The voltage across bulk capacitor can be held under 450 V by tuning the transformer winding ratio even though the converter operates in a wide range of input voltages (90 V∼265 V/ac). This new converter complies with IEC 61000-3-2 under the load range of 200 W, and can achieve fast output voltage regulation.**

***Index Terms*—IEC 61000-3-2 regulations, power factor correction (PFC), switching mode power supplies.**

I. Introduction

AC/DC converters can be designed to have high power transfer efficiency. This characteristic enables ac/dc converters to be used as the primary power supplies in modern electronic products, such as personal computers, computer peripherals, and test instruments. Furthermore, to suppress the quantities of harmonic current emissions, the ac/dc converters must embed a function with power factor correction or harmonic current correction.

There are at least four main demands when designing the converters in wide range input (90∼265 Vrms): 1) the line current harmonics must satisfy agency standards, 2) the primary side dc bus voltage should be less than 450 V/dc to reduce the size of the dc bus capacitor, 3) the feedback control bandwidth should cover the line frequency to minimize low frequency output ripples and advanced dynamic response, and 4) the circuit should be simple and flexible to enhance reliability in practical applications.

In recent years, many studies have presented techniques regarding harmonic current correction in ac/dc converters. These proposed solutions can be classified into two classes. One class yields sinusoidal input line current [1] while the other yields nonsinusoidal input line current [2]. The class with sinusoidal line current has almost a unity power factor but requires a complex topology or control circuit [1], [3]. Fig. 1 schematically shows an ac/dc converter belonging to the sinusoidal input line current class.

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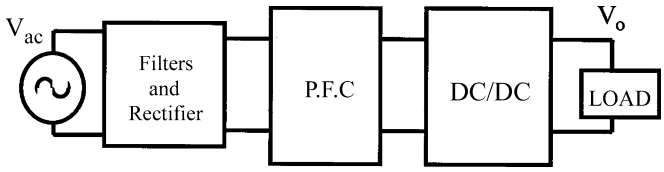

Fig. 1. Classical ac/dc converter with PFC function.

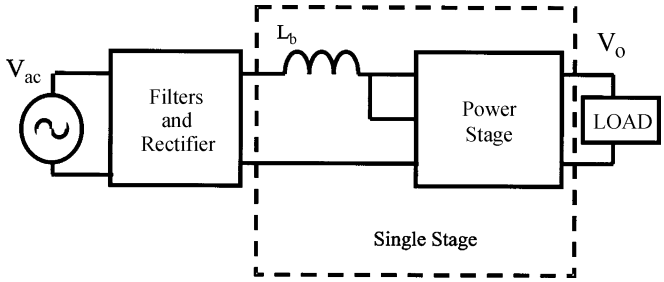

Fig. 2. Prior single stage ac/dc PFC converter.

The other one with nonsinusoidal line current has a simple topology based on a single-stage single-switch. Although they [5]–[9] lacks unity power factor, it complies with IEC 61 000-3-2 [4]. A family of such circuits was described in [5]–[9]. The family circuits often have a common configuration, a boost circuit applied in a dc/dc converter, as shown in Fig. 2. This feature successfully simplifies a conventional two-power-stage with power factor corrector into a one-power-stage corrector.

This study proposes a new converter with the configuration shown in Fig. 3. The new converter satisfies the input harmonic current constraints given by IEC 61 000-3-2 and provides a fast output regulating response. A multi-winding transformer is employed in the proposed converter. This arrangement has three advantages. First, the size of the bulk inductor can be further reduced. Second, the line harmonic currents can be reduced. Third, the phase difference between the fundamental component of the line current and line voltage closely approaches zero. Furthermore, the voltage across the bulk capacitor can be arranged to a reasonable value under 450 V/dc by adjusting the turn-ratio of two primary windings. Therefore, this design can adapt to large line voltage variation. The structure and operation principal of a new converter is explained in the following section, and the practical experimental results are shown in Section V.

II. Proposed Circuit

Fig. 4 shows the proposed new flyback ac/dc converter with harmonic current correction function and tight output regulation. The circuit is a single-stage single-switch ac/dc

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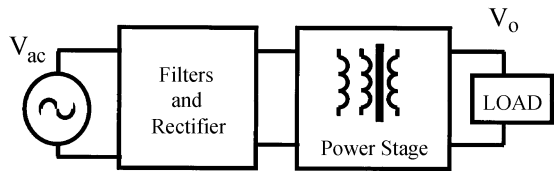

Fig. 3. Proposed single stage ac/dc PFC converter.

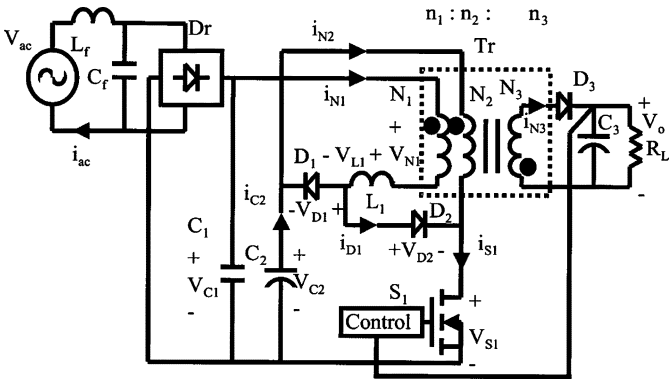

Fig. 4. Proposed simple flyback ac/dc converter.

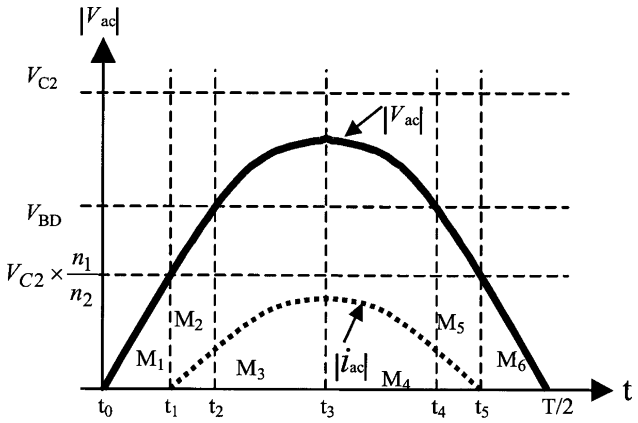

Fig. 5. Operation modes.

converter, which comprises single switch S_1, an input filter L_f, C_f, and C_1, a bulk capacitor C_2, a soft-switching inductor L_1, and a transformer with two primary windings N_1 and N_2. The winding N_1, inductor L_1, diode D_1 and D_2, switch S_1, and bulk capacitor C_2 comprise a boost circuit. The winding N_2 and N_3, bulk capacitor C_2, switch S_1, diode D_3, and output capacitor C_3 form a flyback converter.

The function of inductor L_1 in the proposed circuit is different from that of the boost inductor presented in the converters of [2]–[10]. Actually, L_1 provides partial soft switching functions for diodes D_1 and D_2, to suppress the harmonic current by increasing the conduction time for $i_{\rm ac}$ from time t_1 to t_5 in Fig. 5, and to reduce the voltage V_{C2} across the bulk capacitor.

The inductor L_1 has a soft-switching function on D_1 and D_2, as mentioned in [10]. Fig. 6 shows that when S_1 turns off, D_2 changes to reverse bias and proceed soft off since the current i_{N1} has gradually reduced to zero at the reverse bias time $t_{1,M3}$ or $t_{1,M2}$. Therefore, to overcome the problem of the reverse recovery effect of D_2, a suitable inductance of L_1 must be selected. Contrarily, D_1 softly turns on when the current i_{N1} gradually increases from zero at time $t_{2,M2}/t_{2,M3}$.

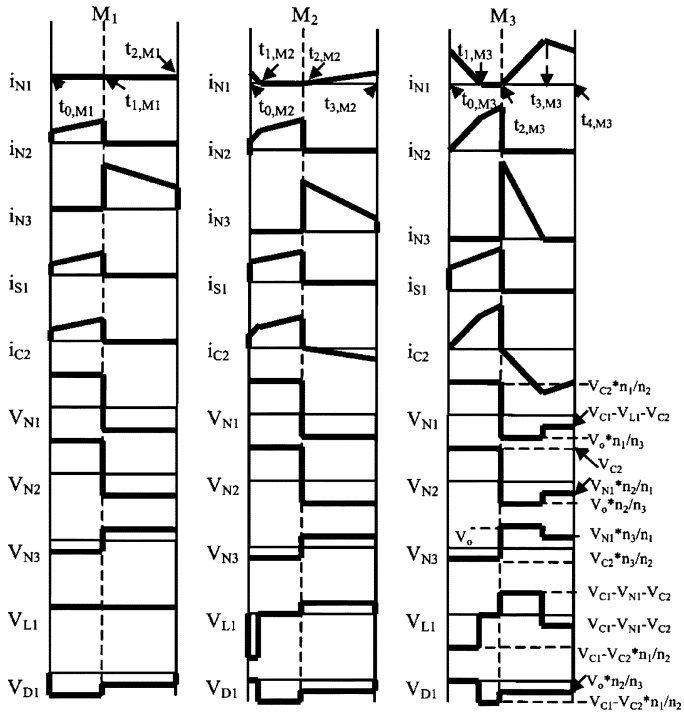

Fig. 6. Current and Voltage waveforms in M1∼M3.

The winding N_1 provides the voltage-boost function for bulk capacitor C_2 during the period from t_1 to t_5, as illustrated in Fig. 5. During this period, when S_1 turns off, D_1 turns on and the charge current flows from the power line source to C_2 through N_1, L_1, and D_1. At this moment, the residue magnetic energy stored in the transformer will also induce current i_{N3} as a falling ramp waveform, as illustrated in Fig. 6. Furthermore, the increasing current i_{N1} keeps storing the magnetic energy in L_1. The magnetic energy stored in L_1 passes to winding N_2 through winding N_1, and induces a portion of current i_{N2} when S_1 is turned on.

The turns-ratio, N_1/N_2, of the transformer can determine not only the starting conduction angle of the line current but also the voltage across a bulk capacitor C_2. Furthermore, the inductance and volume of L_1 are significantly smaller than the primary windings N_1 or N_2 of the transformer.

The control circuit can be designed by using a fixed-frequency simple voltage-mode control or a conventional peak-current control. The experiment results have demonstrated that even using a simple control method, the line current of the proposed ac/dc converter can comply with the standard IEC 61 000-3-2, and the converter also provides fast load dynamic response.

III. Basic Operation Theories

The fundamental operating principle of the proposed converter is to store the magnetic energy in windings N_2 when switch S_1 turns on, and then to deliver it to bulk capacitor C_2 and secondary winding N_3 when switch S_1 turns off. The entire operation principle of the circuit can be explained in three operation modes. Fig. 5 shows six operation modes in a line cycle. Only three modes are left after combining the similar modes,

namely M_1/M_6, M_2/M_5 and M_3/M_4. Fig. 6 shows the main current and voltage waveforms in every mode.

A. Operation Modes $M_1(t_0, t_1)$ and $M_6(t_5, T/2)$

This mode holds when $0 < |V_{\rm ac}| < V_{c2} - V_o \times (n_1/n_3)$. Currents $|i_{\rm ac}|$ and i_{N1} have not yet been induced. The converter operates as a conventional flyback converter. Fig. 7 shows the current conducting path in mode M_1/M_6 with S_1 turned on and off. Fig. 7 shows that the transformer does not sink the current from the power line. Rather, the converter sinks the current from the bulk capacitor C_2. V_{C2} shows the voltage across on C_2 and is approximated to a constant value during a line cycle in the steady state and can be obtained as

$$V_{C2} \le |V_m| + V_o \times \frac{n_1}{n_3} \tag{1}$$

where $|V_{\rm ac}| = V_m|\sin(\omega t)|$.

The voltage-second balance criteria is applied to the flyback transformer, and thus the total voltage-second should be zero in one time period in steady state. Additionally, another required assumption is that the flyback transformer operates in the CCM mode such that

$$V_{C2} = \frac{n_2 V_o(1-D)}{n_3 D} \quad \text{Or} \quad D = \frac{V_o \times n_2}{V_o \times n_2 + V_{C2} \times n_3} \tag{2}$$

where n_1, n_2, and n_3 are the number of turns used in winding N_1, N_2, and N_3.

From (1) and (2), the boundary time of M_1 can be obtained by

$$\omega t_1 = \sin^{-1}\left[\frac{V_o}{V_m} \times \frac{n_2}{n_3}\left(\frac{1-D}{D} - \frac{n_1}{n_2}\right)\right]. \tag{3}$$

Let

$$k = \frac{i_{N3}(t_{2,M1})}{i_{N3}(t_{1,M1})}. \tag{4}$$

Then k is in the range, $0 < k < 1$.

Integrating the winding inductor voltages of V_{N2} and V_{N3} over the duty on and off periods yields

$$i_{N2} = \begin{cases} i_{N2}(t_{0,M1}) + t \times \frac{V_{C2}}{L_{N2}}, & t_{0,M1} < t \le 1t_{1,M1} \\ 0, & t_{1,M1} < t \le t_{2,M1} \end{cases} \tag{5}$$

$$i_{N3} = \begin{cases} 0, & t_{0,M1} < t \le t_{1,M1} \\ i_{N2}(t_{1,M1}) \times \frac{n_2}{n_3} & \\ \quad -(t - t_{1,M1}) \times \frac{V_o}{L_{N3}}, & t_{1,M1} < t \le t_{2,M1} \end{cases}. \tag{6}$$

B. Operation Modes $M_2(t_1, t_2)$ and $M_5(t_4, t_5)$

This mode holds when $V_{c2} - V_o \times (n_1/n_3) < |V_{\rm ac}| < V_{BD}$. In the duty on period, D_2 turns on and current i_{N1} flows through the winding N_1, L_1, D_2, and S_1. Simultaneously, C_2 discharges via winding N_2 and S_1. The conducting paths are as shown in Fig. 8(a) and (b) since the induced voltage V_{N1} exceeding $|V_{\rm ac}|$, i_{N1} is none zero current initially, as displayed in Fig. 8(a) and

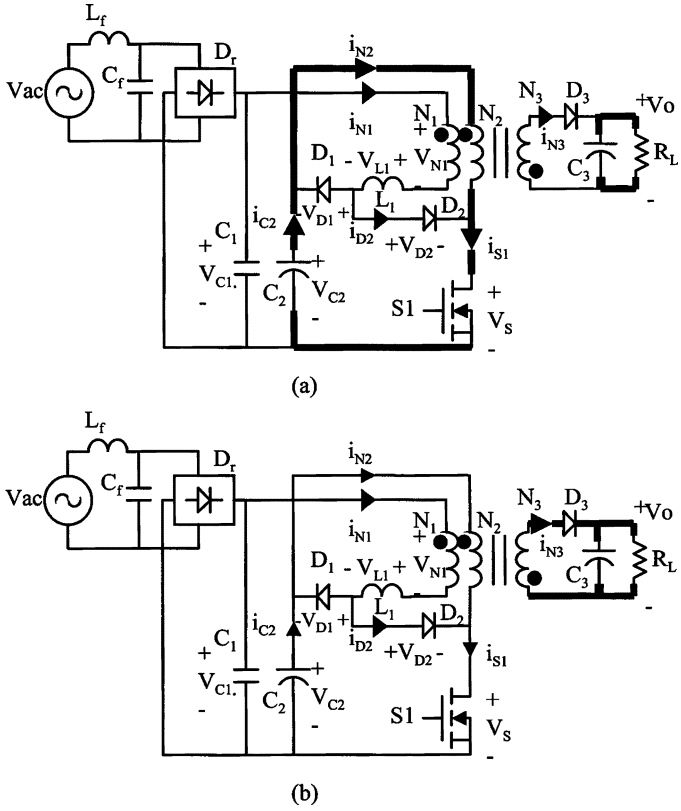

Fig. 7. Current loop in mode M_1: (a) $t_{0,M1} < t \le t_{1,M1}$, S_1 turns on and (b) $t_{1,M1} < t \le t_{2,M1} S_1$, turns off.

reduces to zero linearly and then continues to be zero, as shown in Fig. 8(b).

When S_1 turns off, V_{N1} causes i_{N1} to flow via winding N_1, L_1 and D_1 and to charge the bulk capacitor C_2. Simultaneously, D_3 turns to on state and delivers the magnetic power to the output circuit, as shown in Fig. 8(c). The conduction of D_3 causes the output capacitor connected to two terminals of winding N_3. Therefore, the output current i_{N3} linearly reduces during the duty off period. In this operation, i_{N3} is nonzero even at the end of the duty-off period. Consequently, in mode M_2 the current i_{N3} of winding N_3 operates in the continuous current mode, denoted by CCM. Based on the CCM of i_{N3} and voltage-second balance, the duty ratio D is the same as that in mode M_1/M_6.

Integrating the voltages of the winding inductors of V_{N1}, V_{N2}, and V_{N3} yields the following winding currents:

$$i_{N1} = \begin{cases} i_{N1}(t_{0,M2}) + (t - t_{0,M2}) & \\ \quad \times \frac{V_{C1} - V_{N1}}{L_1}, & t_{0,M2} < t \le t_{1,M2}. \\ 0, & t_{1,M2} < t \le t_{2,M2} \\ (t - t_{2,M2}) & \\ \quad \times \frac{V_{C1} + \frac{n_1}{n_3} \times V_o - V_{C2}}{L_1}, & t_{2,M2} < t \le t_{3,M2} \end{cases} \tag{7}$$

$$i_{N2} = \begin{cases} i_{N2,M2}(t), & t_{0,M2} < t \le t_{1,M2} \\ i_{N2,M2}(t_{1,M2}) & \\ \quad + (t - t_{1,M2}) \times \frac{V_{C2}}{L_{N2}}, & t_{1,M2} < t \le t_{2,M2} \\ 0, & t_{2,M2} < t \le t_{3,M2} \end{cases} \tag{8}$$

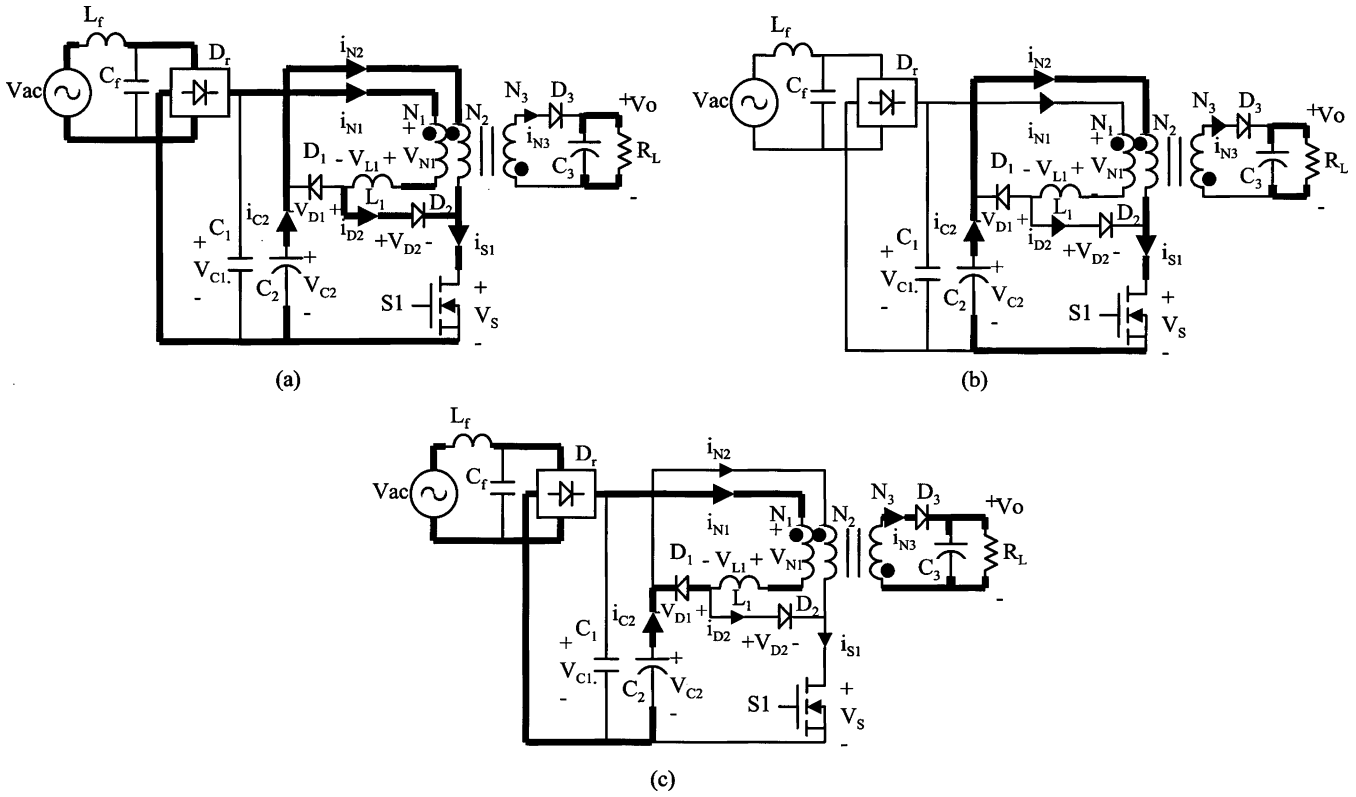

Fig. 8. Current loop in mode M_2: (a) $t_{0,M2} < t \le t_{1,M2}$ S1 turns on, (b) $t_{1,M2} < t \le t_{2,M2}$ and S1 turns on, and (c) $t_{2,M2} < t \le t_{3,M2}$ S1 turns off.

where

$$i_{N2,M2}(t) = (t - t_{0,M2}) \times \left[\frac{V_{N1} - V_{C1}}{L_1} \times \frac{n_1}{n_2} + \frac{V_{C2}}{L_{N2}}\right] + \frac{n_3}{n_2} \times i_{N3}(t_{3,M2})$$

$$i_{N3} = \begin{cases} 0, & t_{0,M2} < t \le t_{2,M2} \\ i_{N3,M2}(t), & t_{2,M2} < t \le t_{3,M2} \end{cases} \quad (9)$$

where $i_{N3,M2}(t) = i_{N2}(t_{2,M2}) \times (n_2/n_3) - (t - t_{2,M2}) \times (V_o/L_{N3}) - i_{N1} \times (n_1/n_3)$.

C. Boundary Condition Between CCM and DCM

The boundary between CCM and DCM occurs just as i_{N3} reaches zero at the end of the switching period. Since the capacitance of C_2 is large, the value of the voltage V_{C2} is almost kept constant. Throughout the M_2 period, when S_1 is in the off period, the N_1 current generated by the line power increases, and accelerates the decrease of i_{N3} according to Ampere's law. If the duty ratio remains unchanged in Mode M_2, then the current $i_{N1}(t_{3,M2})$ at the end of M_2 equals the current $i_{N3}(t_2, M_1) \times (n_3/n_1)$ at the end of mode M_1. This approximation yields

$$\begin{aligned} i_{N1}(t_{3,M2}) &= T_s \times (1 - D) \times \frac{V_{BD} + \frac{n_1}{n_3} \times V_o - V_{C2}}{L_1} \\ &= i_{N3}(t_{2,M1}) \times \frac{n_3}{n_1} \\ &= I_o \times \frac{2}{1 - D} \times \frac{k}{1 + k} \times \frac{n_3}{n_1} \end{aligned} \quad (10)$$

where I_o is the load current

$$I_o = (1 - D)\left[I_{pk}\frac{(1 + k)}{2}\right].$$

At the boundary, $|V_{\rm ac}|$ is denoted by V_{BD}, which can be obtained by

$$\begin{aligned} V_{BD} &= V_m \sin(\omega t_2) \\ &= V_{C2} - V_o \times \frac{n_1}{n_3} + I_o \times \frac{2kL_1 \times n_3}{T_s(1 - D)^2(1 + k)n_1} \end{aligned} \quad (11)$$

where

$$k = \frac{i_{N3}(t_{2,M1})}{i_{N3}(t_{1,M1})}.$$

Then k is in the range $0 < k < 1$.

D. Operation Modes $M_3(t_2, t_3)$ and $M_4(t_3, t_4)$

This mode holds when $V_{BD} < |V_{\rm ac}| < V_m$. The large current i_{N1} increases the rate of decay of i_{N3}. The current i_{N3} falls to discontinuous current mode (DCM) in this operational mode. Fig. 9 shows four different current flow paths in a switching cycle. The energy stored in winding N_2 during the duty on period of S_1 are distributed to the winding N_1 and winding N_3 in the duty off time period. During a switching cycle, i_{N1} and i_{N2} are ruled as in mode M_2/M_5. However, i_{N3} reduces to zero before the end of the duty off period of S_1.

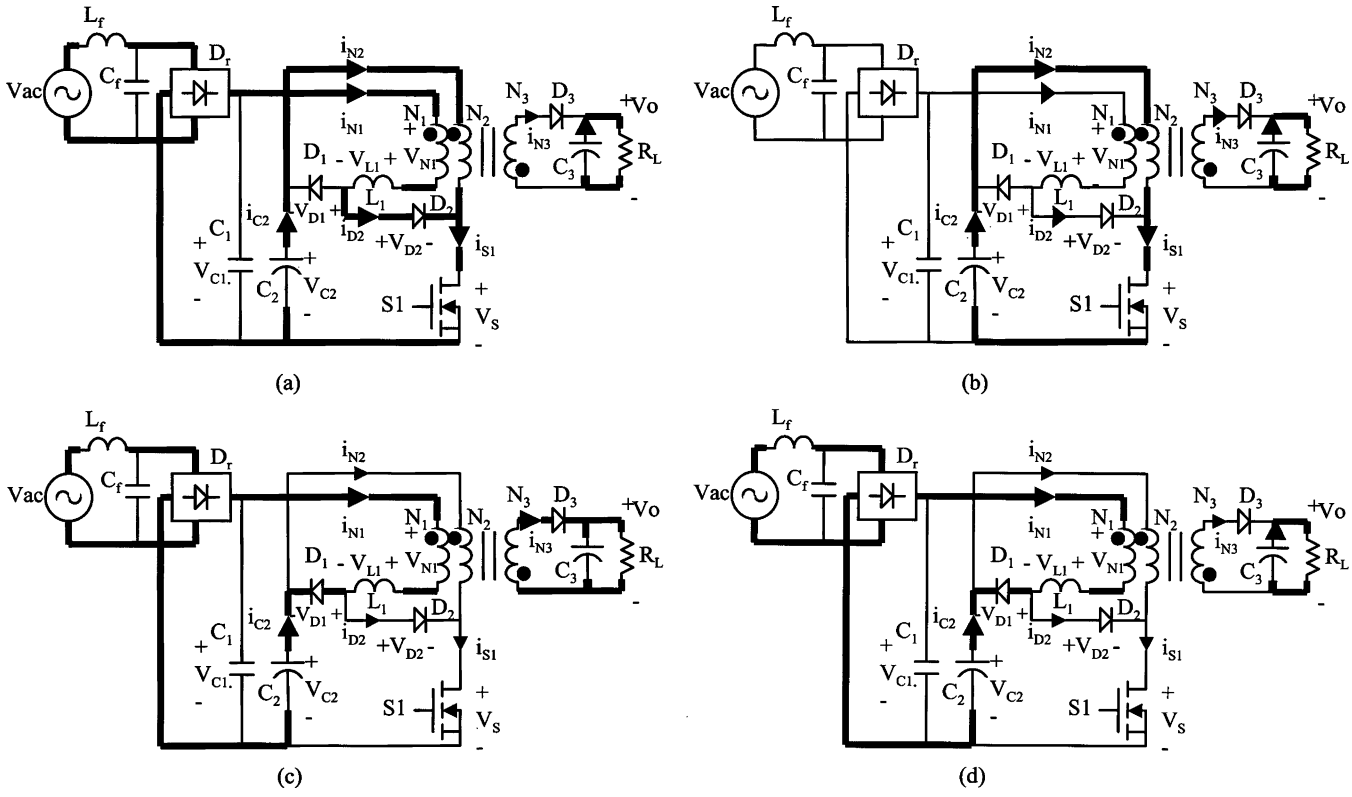

Fig. 9. Current loops in mode M_3: (a) $t_{0,M3} < t \le t_{1,M3}$, S_1 turns on, (b) $t_{1,M3} < t \le t_{2,M3}$, S_1 turns on, (c) $t_{2,M3} < t \le t_{3,M3}$, S_1 turns off, and (d) $t_{3,M3} < t \le t_{4,M3}$, S_1 turns off.

The winding currents and voltages of inductor L_1 and transformer are given as

$$i_{N1}=\begin{cases} i_{N1}(t_{0,M3})+t \\ \quad \times\frac{V_{C1}-V_{N1}}{L_1}, & t_{0,M3}<t<t_{1,M3} \\ \quad 0, & t_{1,M3}<t<t_{2,M3} \\ (t-t_{2,M3}) & \\ \quad \times\frac{V_{C1}+\frac{n_1}{n_3}\times V_o-V_{C2}}{L_1}, & t_{2,M3}<t<t_{3,M3} \\ i_{N1}(t_{3,M3})+(t-t_{3,M3}) & \\ \quad \times\frac{V_{L1}}{L_1}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{12}$$

$$i_{N2}=\begin{cases} i_{N2,M3}(t), & t_{0,M3}<t\le t_{1,M3} \\ i_{N2}(t_{1,M3})+(t-t_{1,M3}) & \\ \quad \times\frac{V_{C2}}{L_{N2}}, & t_{1,M3}<t\le t_{2,M3} \\ \quad 0, & \text{otherwise} \end{cases} \tag{13}$$

where

$$i_{N2,M3}(t)=(t-t_{0,M3})\times\frac{V_{N1}-V_{C1}}{L_1}\times\frac{n_1}{n_2} +(t-t_{0,M3})\times\frac{V_{C2}}{L_{N2}}$$

$$i_{N3}=\begin{cases} i_{N2}(t_{2,M3})\times\frac{n_2}{n_3}-i_{N1}(t) & \\ \quad \times\frac{n_1}{n_3}-(t-t_2)\frac{V_o}{L_{N3}}, & t_{2,M3}<t\le t_{3,M3} \\ \quad 0, & \text{otherwise} \end{cases} \tag{14}$$

$$V_{N1}=\begin{cases} V_{C2}\times\frac{n_1}{n_2}, & t_{0,M3}<t\le t_{2,M3} \\ -Vo\times\frac{n_1}{n_3}, & t_{2,M3}<t\le t_{3,M3} \\ V_{C1}-V_{L1}-V_{C2}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{15}$$

$$V_{N2}=\begin{cases} V_{C2}, & t_{0,M3}<t\le t_{2,M3} \\ -Vo\times\frac{n_2}{n_3}, & t_{2,M3}<t\le t_{3,M3} \\ V_{N1}\times\frac{n_2}{n_1}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{16}$$

$$V_{N3}=\begin{cases} -V_{C2}\times\frac{n_3}{n_2}, & t_{0,M3}<t\le t_{2,M3} \\ V_o, & t_{2,M3}<t\le t_{3,M3} \\ -V_{N1}\times\frac{n_3}{n_1}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{17}$$

$$V_{L1}=\begin{cases} V_{C1}-V_{N1}, & t_{0,M3}<t\le t_{1,M3} \\ 0, & t_{1,M3}<t\le t_{2,M3} \\ V_{C1}-V_{N1}-V_{C2}, & t_{2,M3}<t\le t_{3,M3} \\ \frac{V_{L_1,3-4}}{(1-D-\tilde{F})}, & t_{3,M3}<t<t_{4,M3} \end{cases} \tag{18}$$

where

$$V_{L_1,3-4}=\left[V_{C2}\frac{n_1}{n_2}-V_{C1}\right]\tilde{D}-\left[V_{C1}+V_o\frac{n_1}{n_3}-V_{C2}\right]\tilde{F}.$$

Employing the voltage-second balance theorem for winding N_2 and N_3 in mode M_3 in steady state, all of (15)–(18) give the

$$V_{C2}\times D=\frac{n_2}{n_3}V_o\times\tilde{F}-\frac{n_2}{n_1}(V_{C1}-V_{C2})\times(1-D-\tilde{F}) +\frac{n_2}{n_1}\left(\frac{n_1}{n_2}V_{C2}-V_{C1}\right)\tilde{D}-\frac{n_2}{n_1}\left(V_{C1}+\frac{n_1}{n_3}V_o-V_{C2}\right)\tilde{F}.$$

Simplifying the above equation, the duty ratio D can be obtained by

$$D=\frac{\tilde{D}\left(\frac{n_2}{n_1}V_{C1}-V_{C2}\right)+\frac{n_2}{n_1}(V_{C1}-V_{C2})}{\frac{n_2}{n_1}V_{C1}-V_{C2}\left(1+\frac{n_2}{n_1}\right)} \tag{19}$$

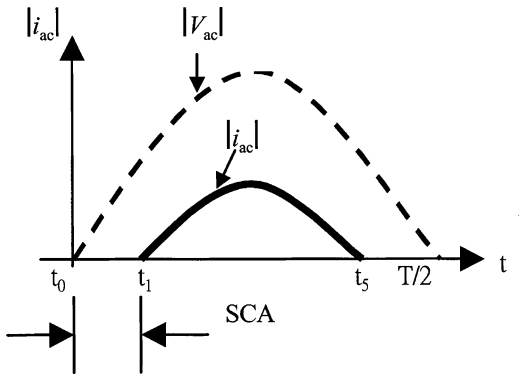

Fig. 10. Starting conduction angle.

where

$$\tilde{D} = \frac{t_{1,M3} - t_{0,M3}}{Ts}$$
$$\tilde{F} = \frac{t_{3,M3} - t_{2,M3}}{Ts}$$

and $V_{C1} = |V_{\rm ac}| = |V_m \sin(\omega t)|$ in $M_2/M_5 \sim M_3/M_4$.

IV. Analysis of Converter Operation

A. Primary Current i_{N1} and Duty Ratio D

In the converter circuit the filter capacitance C_1 is designed as a low pass filter to bypass the switching signal to ground and to pass the line power signal to the converter. Consequently, the primary component of $|i_{\rm ac}|$ approximates to the primary component of i_{N1}. From (7) and (12), i_{N1} and V_{C1} display a linear relation when the angle of the line power signal exceeds the conduction angle. Therefore, $i_{\rm ac}$ can be controlled to be linearly related to $V_{\rm ac}$ during the conduction periods.

The secondary winding N_3 of the transformer operates in CCM during modes M_1 and M_2 and in DCM during mode M_3. The calculation of duty ratio can be simply obtained from (2), when winding N_3 operates in modes M_1 and M_2. However, the duty ratio becomes more complicate as given in (19) for mode M_3, since the current i_{N3} enters DCM. The value of duty ratio in mode M_3 is smaller than in modes M_1 and M_2. Furthermore, the duty ratio will be smallest when the peak $V_{\rm ac}$ presents, since $\tilde{D}$ increases and $\tilde{F}$ decreases when $|V_{\rm ac}|$ increases from zero to the peak value.

B. Starting Conduction Angle

The value $\omega(t_1 - t_0)$ is called a starting conduction angle (SCA), as shown in Fig. 10. A smaller SCA leads to higher power factor and lower THD. Equation (3) shows that the SCA increases with increasing product of V_o/V_m and N_2/N_3. This phenomenon implies that power factor or THD decreases with increasing V_o/V_m or N_2/N_3. Fig. 11 shows the relationship between V_o/V_m and SCA under various duty ratios D and two different winding ratios of n_1/n_2.

C. Voltage Across Bulk Capacitor

Equation (1) shows that the voltage across bulk capacitor, V_{C2}, varies with V_m, SCA, V_o, and n_1/n_3 but does not vary with the output load. In most applications, all the design calculations are always based on the given values of V_m and V_o. Thus, the voltage V_{C2} can be determined by selecting the preferred n_1/n_3, SCA, or n_2/n_3. In practical applications, the voltage V_{C2} is kept under 450 v for commercial considerations. Fig. 12 provides designers with a convenient graphical design aid for obtaining the eclectic selections of n_1/n_3, SCA, and V_{C2} for certain line voltage ranges.

According to Fig. 5, the current i_{N1} is zero in model M_1 because the sum of V_{C1} and V_{N1} is smaller than V_{C2} when S_1 is in the off state. The diode D_1 continues off until the sum of V_{C1} and V_{N1} exceeds V_{C2}. Therefore, SCA decreases with decreasing V_{C2}. Two methods can be used to reduce V_{C2}. One method uses a smaller number of winding turns for n_1, and the other uses a larger inductance in L_1. The larger inductance L_1 can resist i_{N1} to charge V_{C2}, thus achieving lower V_{C2}.

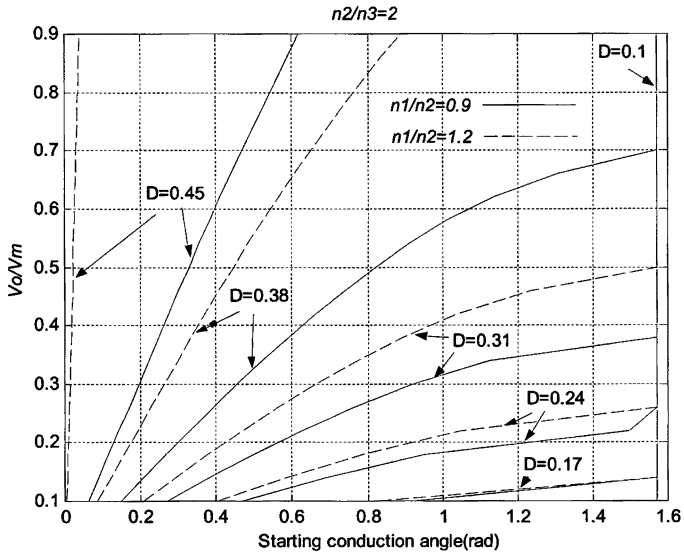

Fig. 11. Curve of starting conduction angle, V_o/V_m, D and N_1/N_2 at $N_2/N_3 = 2$.

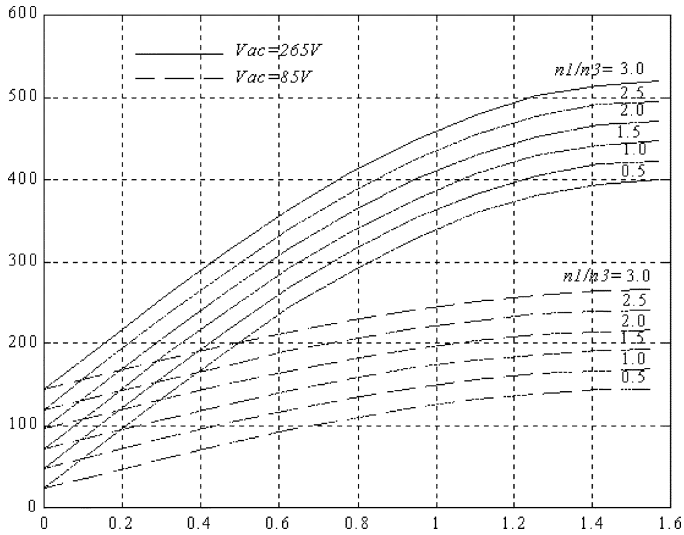

Fig. 12. Curve of starting conduction angle, V_{C2}, and n_1/n_3 at $Vo = 48$ V.

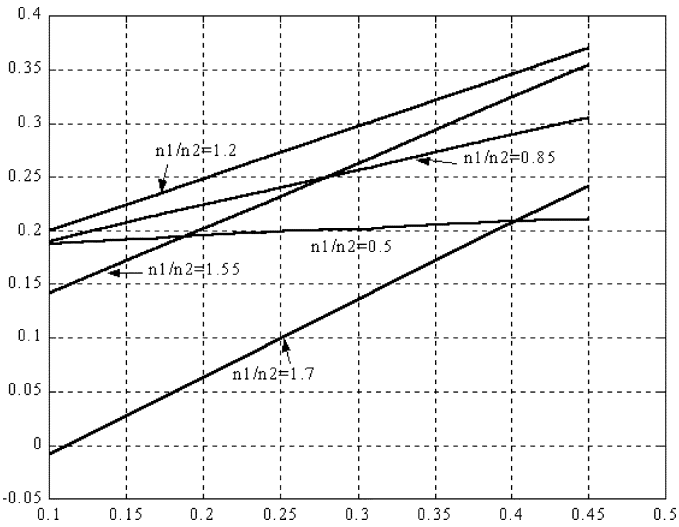

Fig. 13. Max L_1/L_{N2} and duty cycle.

D. Inductor L_1

The inductor L_1 is designed to provide the partially soft-switching function for diodes D_1 and D_2. When the current i_{N1} decreases, inductor L_1 causes the current i_{N1} to linearly decrease to zero, and the diode D_2 turns off without any switching-loss. Furthermore, the inductor L_1 causes i_{N1} to increase linearly from zero, and the diode D_1 turns on without switching-loss. To guarantee the partial soft-switching, functions above, current i_{N1} must reduce to zero before switch S_1 turns off.

Employing the voltage-second theorem in L_1 for one switching cycle, (15)–(18) in mode M_3 yields

$$(V_{N1}-V_{C1})(t_{1,M3}-t_{0,M3})+V_{L1,3-4}\times T_s = (V_{C2}+V_{N1}-V_{C1})(t_{3,M3}-t_{2,M3}) \quad (20)$$

let $t_{1,M3}-t_{0,M3}=DT_S$ and $V_{C1}=V_m$. Then simplifying (20) can give (21). The T_S is a period of switching cycle

$$L_1 \le L_{N2}\times\frac{n_3}{n_2}\times\frac{V_m+\frac{n_1}{n_3}\times V_o-V_{C2}}{2V_o} \times\left[\frac{V_m}{V_{C2}}\times\left(D\times\frac{n_2}{n_1}+D\times\frac{n_3}{n_1}-\frac{n_3}{n_1}\right) +D\times\frac{n_3}{n_2}+\frac{n_3}{n_2}+1-\frac{n_2}{n_1}\right]-\frac{n_1}{n_2} \times\frac{\frac{n_1}{n_3}\times V_o-V_m}{V_{C2}}. \quad (21)$$

Fig. 13 provides the designer a selection aid of L_1 to guarantee the partially soft-switching function working to D_1 and D_2.

V. Experimental Results

An experimental prototype has been established to demonstrate the circuit operation and the analysis results presented above. The experimental circuit can operate in 85 $\sim$ 265 V/ac input voltage range and generate an output voltage of 48 v/dc and an output power of 96 W. The turn ratio of $n_1/n_2/n_3$ is 2.38/2/1 and the inductance ratio of L_1/L_{N1} is 0.17, where

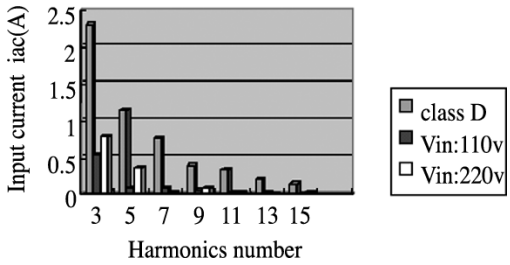

Fig. 14. Harmonic main contents of the line current.

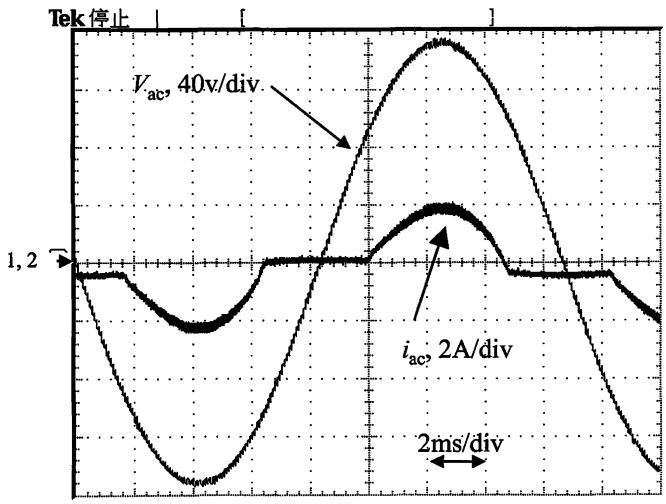

Fig. 15. Line current and line voltage waveforms at $\mathrm{Vac}=110$ V and ouput= 48 V/2 A.

$L_1=30\ \mu$H and transformer core PQ32/20 is used. The transformer core employed in previous similar converter should be EER35 in [6], [7]. Although some previous similar converters have similar transformer core size to the proposed converter for similar output power and switching frequency, the values of the boost inductors, 58 $\sim$ 240 μH in [6] or 1.4 mH in [7], are several times greater than the value of L_1 in the proposed converter. The sizes of the boost inductors employed in [6], [7] thus are several times greater than that of L_1 when flowing through a similar line current. The converters in [8] or [9] use similar smaller boost inductor 30 μH, but the line current harmonic distribution is higher than that produced by the proposed converter. Fig. 14 shows that the detailed harmonic distributions of the experimental circuit using two different power line voltages are significantly below the levels required by class D.

Fig. 15 shows the line current in a line-cycle, revealing that its harmonic distribution complies with a standard of IEC 61 000-3-2. Fig. 16 shows the dynamic response from a 3/8 to 3/4 full load in 110 v/ac input voltage. The output voltage of prototype shows a fast response and stable regulation. Fig. 17 shows the voltages across bulk capacitor for different input voltages at full load. The experimental results demonstrate that the bulk capacitor voltage was ranged between 60$\sim$70% higher than the line voltage. Furthermore, a lower percentage can be achieved by carefully selecting the winding ratio. The voltage of the bulk capacitor is shown to depend on both V_{ac} and turn ratio n_1/n_3, but irrelative to load current.

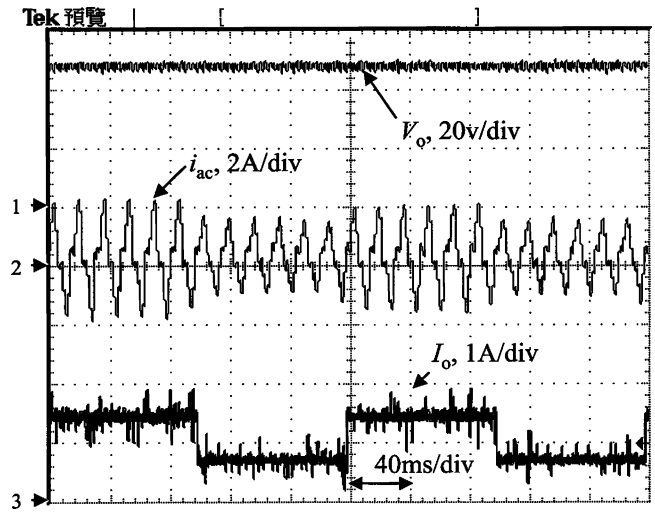

Fig. 16. Dynamic response waveforms for output voltage Vo, line current iac, output current Io: Ch1 → Vo = 48 V, Ch2 → iac, Ch3 → Io = 0.75 A/1.5 A.

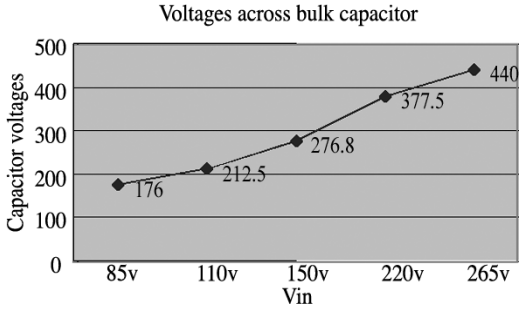

Fig. 17. Voltage rating of bulk capacitor and line voltage.

VI. Conclusion

This study introduces an ac/dc converter with a new structure. The proposed converter has harmonic current correction, fast dynamic response and tight voltage regulation. The new converter is implemented using a single-stage single-switch and simple control loop. Therefore, the proposed structure is simple. Conventional S^4IP^2 converters use a two primary winding transformer. However, the proposed design incorporates an additional primary winding to replace the primary function of the bulk inductor. This change achieves a nearly 50% saving in magnetic material volume and weight while comparing to the one of two-stages approach (PFC plus dc/dc) shown in Fig. 1. The experimental results have demonstrated that the current of the proposed converter line complies with standard IEC 61 000-3-2 and there is tight voltage regulation under load change. The voltage across the bulk capacitor can be kept under 450 V by adjusting the turn-ratio n_1/n_3 in a full range operation (85 V∼265 V/ac). This new structure can also be extended to other converters, such as forward converters.

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