Journal of The Electrochemical Society, **152** (2) G158-G162 (2005)
0013-4651/2005/152(2)/G158/5/$7.00 © The Electrochemical Society, Inc.

Improvement of Junction Leakage by Using a Zr Cap Layer on a 30 nm Ultrashallow Nickel-Silicide Junction

Tsung Lin Lee,[z] Ming Zhen Lee, Tan Fu Lei, and Chung Len Lee

Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan

This paper investigates the effects of Zr capping on nickel silicided n^+/p shallow junctions. Although nickel silicide possesses many benefits compared with titanium and cobalt silicide, some potential problems still need to be addressed for ultrashallow junction applications. In this work, a Zr protective cap is used to preserve the silicide from oxygen contamination and to suppress the increase of junction leakage during the silicidation process. Due to the suppressed leakage current and the appropriate series resistence, formation of a 30 nm ultrashallow junction can be accomplished.
© 2005 The Electrochemical Society. [DOI: 10.1149/1.1851052] All rights reserved.

Manuscript submitted February 20, 2004; revised manuscript received June 2, 2004. Available electronically January 12, 2005.

As metal oxide semiconductor field effect transistor (MOSFET) scaling continues to achieve a dense and high speed integrated circuit, formation of an ultrashallow junction is essential for device performance and suppression of short channel effects (SCE).[1,2] Along with the shrinkage of device dimensions, the contact resistance of source and drain is increased correspondingly. Moreover, such resistance deterioration is also encountered in local interconnects. As a result, the technique of metal silicides for poly gate and source/drain has been developed to reduce their contact resistance and the parasitic junction resistance as well.[3] In nanometer MOSFET fabrication, a silicidation process incorporation compatible with the presence of shallow junctions is indispensable. Therefore, how to form a shallow silicided junction without increasing junction leakage is considered as a critical module for the nanoscale complementary metal oxide semiconductors (CMOSs).

Currently, the most widely used metal silicides include $TiSi_2$, $CoSi_2$, and NiSi. For $TiSi_2$, even though it possesses good thermal stability, high silicidation temperature is still required for the phase transformation (from a high-resistivity C49 phase to a low-resistivity C54 phase), thus limiting its use with an ultrashallow junction.[4-9] However, as the line-width below 350 nm, the phase transformation from C49 to C54 phase becomes harder because the enlarged silicide grain size is restricted.[10,12] Beyond the 0.35 μm technology node, titanium is replaced by cobalt due to its less line-width effect. However, the large amount of silicon consumption, rough $CoSi_2$/Si interface, and local spiking of junctions will lead to the increase of junction leakage.[11-13] For ultrashallow junction, nickel silicide consumes fewer silicon atoms than cobalt silicide and is believed to be a potential candidate for future silicide technologies. In addition, its relatively small film stress is another merit.[14] Although nickel silicide possesses lower resistivity, lower silicon consumption, only one annealing step, and negligible degradation on narrow linewidth, its poor thermal stability must be improved in CMOS process application.[15,16,24] Recent studies of nickel silicide have shown that the formation of NiSi is extremely sensitive to interfacial native oxide on a silicon surface or oxygen contamination during the silicidation process.[10,17-20] In our previous work, it was found that the silicide depth can be well controlled by a Zr capping layer on nickel silicides, and at the same time a smooth interface between silicides and silicon substrate can be maintained.[21] Moreover, thermal stability is dramatically improved by Zr capping. In this work, we compare the effect of this Zr cap with the behavior of a conventional Ti cap layer in terms of the leakage characteristics of ultrashallow nickel-slilicide junction.

Experimental

Figure 1 shows the process flow for the fabrication of the n^+/p silicided junction in our experiment. Following a standard RCA cleaning process, a 500 nm thick field oxide was thermally grown on the p-type (100) oriented Si wafer with 3-5 Ω cm at 1050°C for 1 h. After isolation oxide formation, the active regions were defined by photolithography and etched by buffer oxide etcher (BOE) solution. Subsequently, an RCA clean was performed for eliminating the contamination. Then, the PH_3 plasma immersion was used to form an n^+/p junction with RF power of 50 W for 5 min. After plasma immersion, rapid thermal annealing (RTA) was carried out on the formed n^+/p junctions for 30 s at 950°C in nitrogen ambient. Then, the samples were loaded into a dual electron-beam evaporation system following a dilute HF dip. A 10 nm thick nickel film was first deposited onto n^+/p junctions at a base pressure of 1×10^{-6} Torr with a deposition rate of 1 Å/s, and immediately a titanium and zirconium film of about 5 nm was sputtered as a capping layer onto the nickel layer. After metal deposition, the silicidation procedure was carried out by the rapid thermal process, and the annealing temperature was varied from 550 to 850°C in N_2 ambient. In order to integrate into the ultrashallow junction formation, the silicidation time is shortened to be 10 s. Then, the unreacted metal was removed by wet etching. Before final metallization, a thin TaN of about 25 nm was deposited as a barrier layer. Eventually, aluminum was used for both the front and back side electrode.

Table I shows four different groups of samples that were fabricated in this experiment. As the reference, nonsilicided samples are simple n^+/p junctions only. The other samples are nickel silicide junctions. Among those silicide samples, noncapped NiSi samples

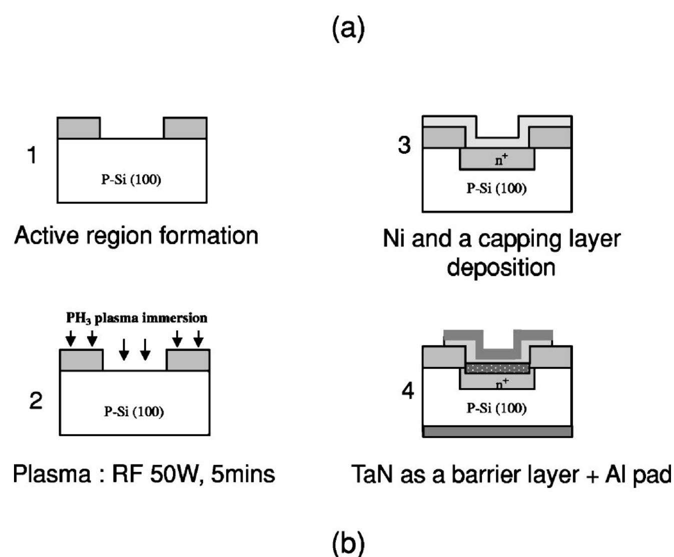


Figure 1. (a) The simple process flow of n^+/p junction formation. (b) The schematics of n^+/p junction fabrication.

[z] E-mail: tsunglinlee.ee87g@nctu.edu.tw

Downloaded on 2014-04-26 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Table I. n^+/p junction formation by PH_3 plasma immersion with and without nickel silicide in different capping conditions. The nickel and the capping layer are about 10 and 5 nm, respectively.

Structure	Nonsilicide samples	Noncapped NiSi samples	Ti capped on NiSi samples	Zr capped on NiSi samples
Doping to junction	PH_3 plasma immersion: RF 50 W, 5 min			
Silicide metal		Nickel: 10 nm		
Capping metal			titanium 5 nm	zirconium 5 nm

and Ti capped on NiSi samples are designed for comparison. Also the experimental samples are capped by Zr.

Results and Discussion

Sheet resistance and SIMS analysis for PH_3 plasma junction.—Sheet resistances of all samples were examined with a four-point probe. Figure 2 shows the sheet resistance of PH_3 plasma immersion junction with different activation conditions. In order to form low-resistivity junctions, the control sample was activated with RTA condition of 950°C for 30 s. Figure 3 shows the secondary ion mass spectroscopy (SIMS) result of the phosphorus profile of PH_3 plasma doping junction after the activation condition of 950°C for 30 s. From this plot, a shallow n^+/p junction formation of about 30 nm depth can be demonstrated.

The sheet resistances of those nickel silicided junction are displayed in Fig. 4. From Fig. 4, the degradation in sheet resistance of noncapped nickel silicide samples may be due to agglomeration and phase transformation from NiSi to $NiSi_2$ at the high annealing temperature as reported in Ref. 9 and 23. However, Ti capped and Zr capped the NiSi samples are improved in their sheet resistance due to the capping layer, which can suppress the oxidation of silicide films during the RTA process.[10,16-20] Especially for Zr capped NiSi samples, the sheet resistance degradation can be obviously suppressed compared with other cases even after the annealing temperature reached 850°C.

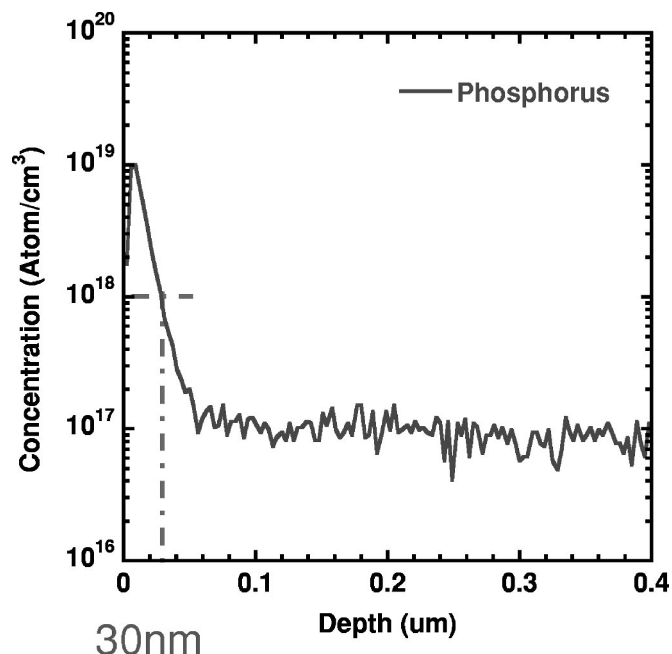


Figure 3. SIMS profile of n^+/p junction by PH_3 plasma doping. The dopant activation condition is 950°C for 30 s.

Reverse bias junction leakage characteristics.—In addition, the current-voltage characteristics of the PH_3 plasma-doped junction is shown in Fig. 5, and the junction area size is about 1000×1000 μm^2. The reverse leakage current of the silicided junctions were measured using a Hewlett-Packard 4156 semiconductor parameter analyzer. In this figure, the I-V characteristics of nickel silicide and nonsilicide n^+/p junctions are compared. Figure 6 shows the cumulative leakage current distribution of all junction samples. From these two plots, the samples with a Zr cap layer with a silicidation condition of 650°C have the smallest leakage current in all silicided n^+/p junctions. Figure 7 is a group of Weibull plots illustrated with

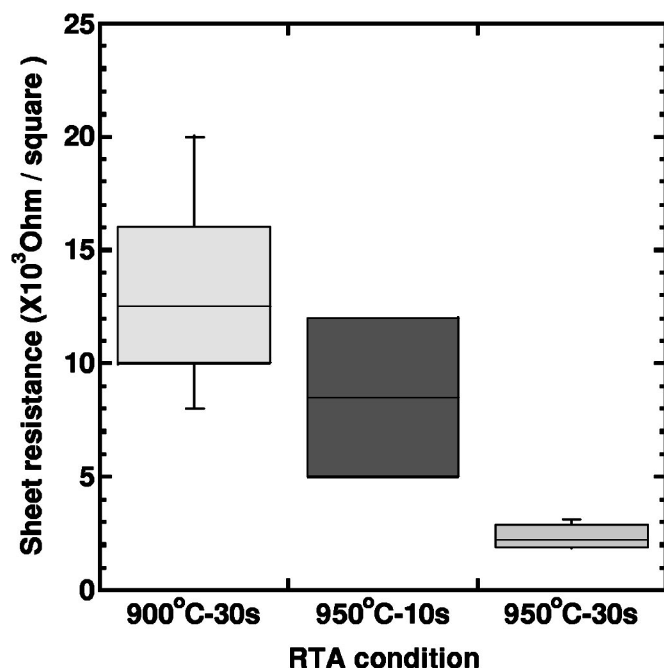


Figure 2. Sheet resistance *vs.* the annealing temperature for PH_3 plasma junction.

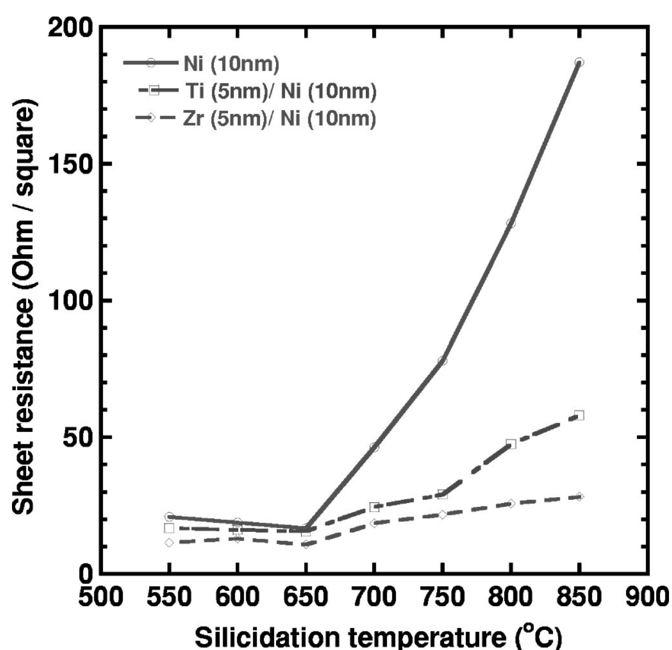


Figure 4. Sheet resistance *vs.* the silicidation condition for Ni/Si, Ti/Ni/Si, and Zr/Ni/Si nickel silicide systems (as indicated in the figure).

Downloaded on 2014-04-26 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

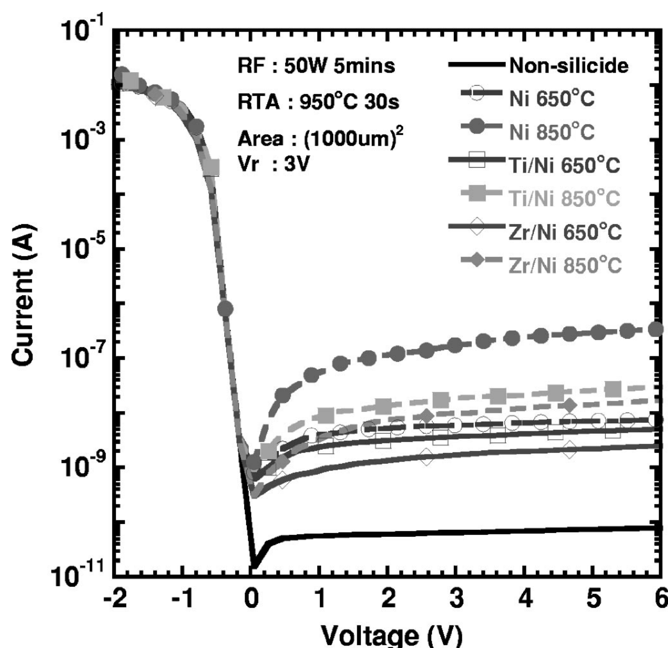


Figure 5. Reverse current-voltage characteristics of PH_3 plasma junctions with and without nickel silicide.

the leakage current at reverse bias of 3 V for different capping conditions. In Fig. 7a-c, all nickel silicide samples exhibit the lowest leakage level at the RTA condition of 650°C. We have indeed concluded that using a cap layer can avoid the increase of junction leakage and also confine the cumulative leakage distribution within a narrow window of values. These effects are more pronounced for the samples with Zr, that was attributed to the presence of a smooth interface between silicide and substrate.[21]

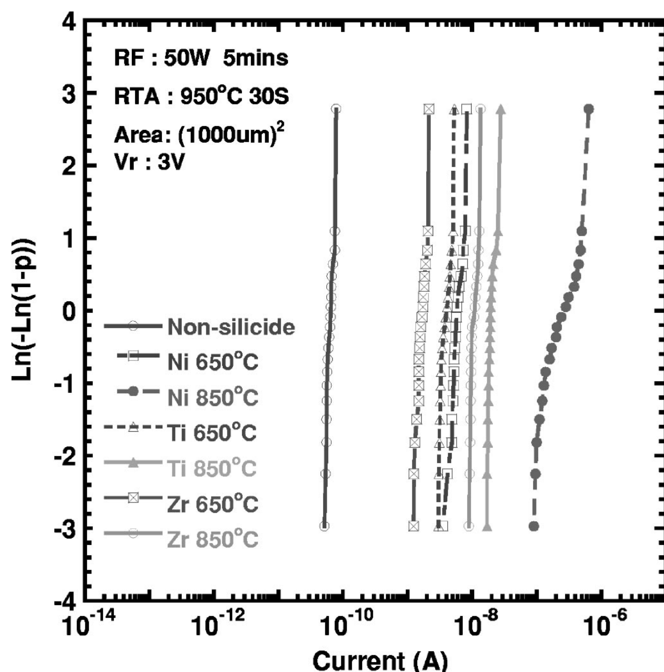
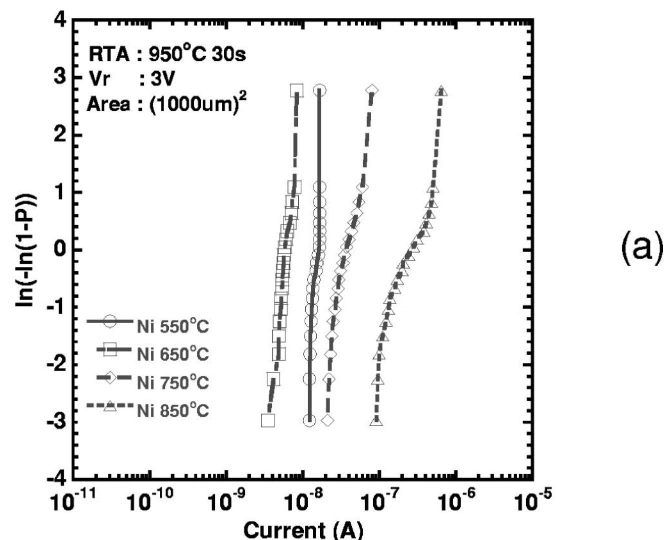
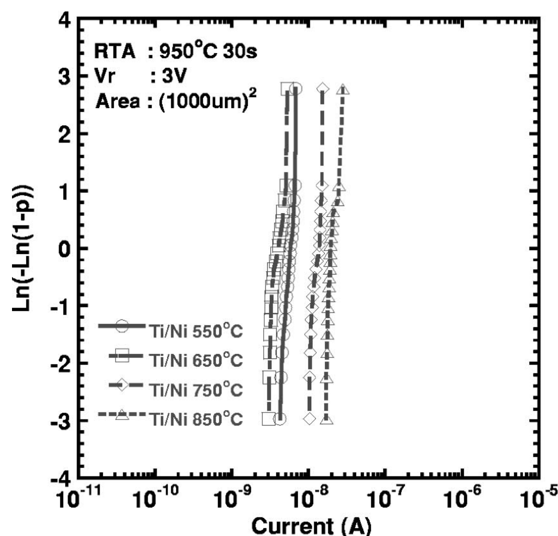


Figure 6. Weibull plots of the leakage current of all nickel silicide samples at silicidation temperatures of 650 and 850°C respectively. The size of the junction area is 1000 × 1000 μm^2.





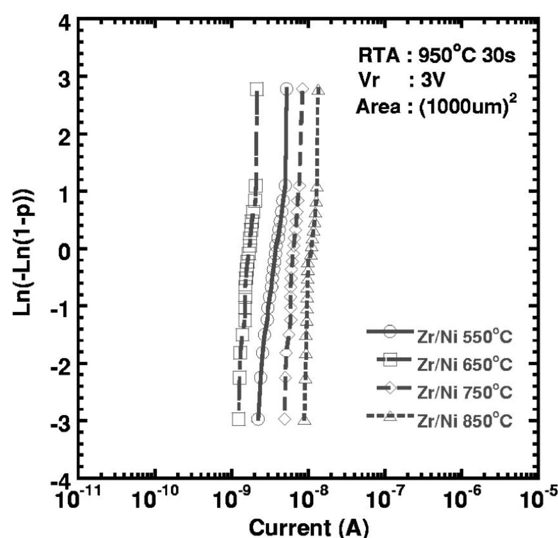


Figure 7. Cumulative leakage current distribution for different silicidation conditions and silicide-structures. (a, top) Cumulative leakage distribution for a simple nickel silicided junction with the annealing temperature varied from 550 to 850°C. (b, center) The Weibull plot of leakage current density for nickel silicided junction with Ti capping after being annealed from 550 to 850°C. (c, bottom) Samples with a Zr capping layer annealed ranging from 550 to 850°C.

Downloaded on 2014-04-26 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

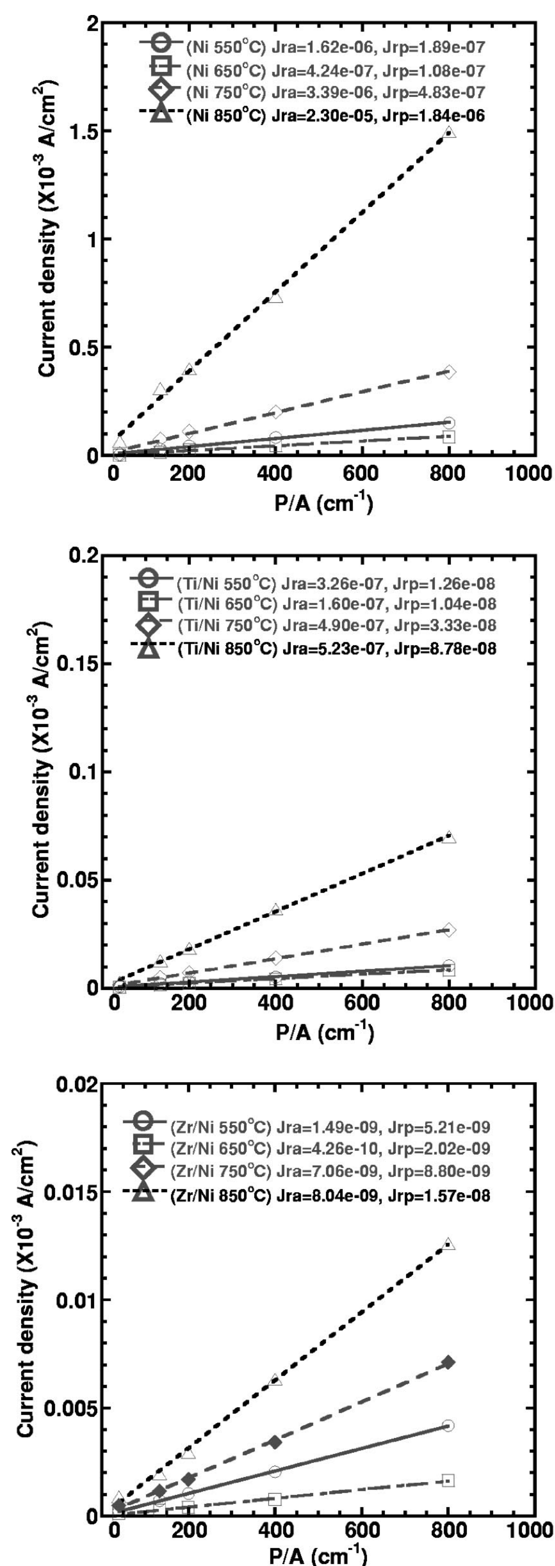


Figure 8. Comparison of reverse junction leakage current density *vs.* periphery to area ratio (P/A ratio) for (a, top) noncapped NiSi samples, (b, center) Ti-capped on NiSi samples, (c, bottom) Zr-capped on NiSi samples.

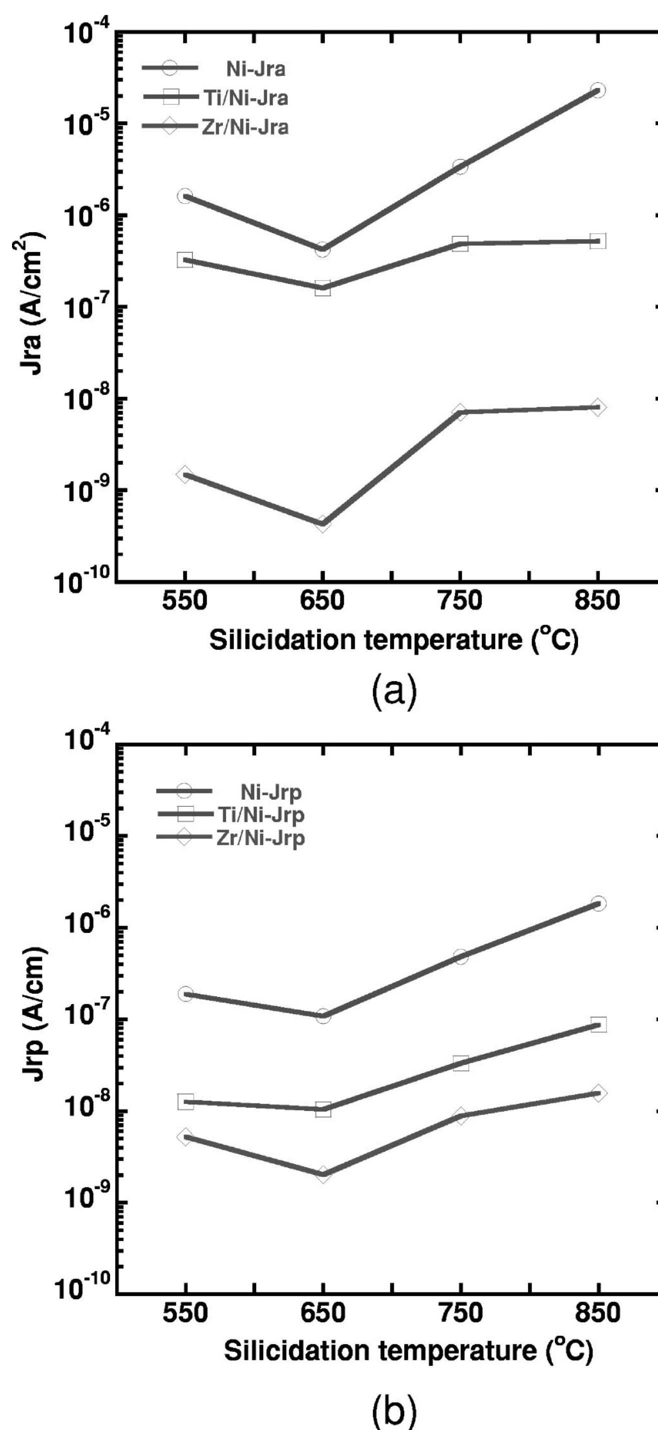


Figure 9. Reverse junction (a) area leakage and (b) periphery leakage *vs.* the RTA temperature for all nickel silicide samples in different capping conditions.

Effects of Zr capping on junction periphery and area leakage characteristics.—It is well known that the leakage current (I_r) in p-n junction is composed of two major components including junction area leakage (I_{ra}) and junction periphery leakage (I_{rp}). That is

$$I_r = I_{ra} + I_{rp} = J_r(A) = J_{ra}(A) + J_{rp}(P) \quad [1]$$

$$J_r = J_{ra} + J_{rp}(P/A) \quad [2]$$

Those two components of leakage current can be separated by Eq. 2.[22] Figure 8a-c are plots of the leakage current density *vs.* the ratio of junction periphery (P) and area (A) for all silicided samples. The slope stands for the junction periphery leakage density, while the intersection with y axis represents the junction area leakage density. The smallest periphery and area leakage could be observed at the

Downloaded on 2014-04-26 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

annealing temperature of 650°C in all three groups. Effects of capping conditions on junction leakage from periphery and area are also shown in Fig. 9. The samples with a capping structure can remain at the level low leakage even after a high RTA temperature. The values of J_{ra} and J_{rp} have been shown in Fig. 9a and b as a function of T and the cap type to illustrate that junction leakage from the area and periphery can be reduced by using a Zr cap.

Conclusions

In summary, nickel silicide with a cap layer can achieve better thermal stability and can improve junction leakage characteristics as well. Especially for the Zr cap layer, it can effectively suppress the enormous degradation of NiSi sheet resistance due to the phase transformation after a high annealing temperature (~850°C) and can significantly reduce the increase of reverse junction leakage. With this Zr cap layer, low resistance and smooth interface nickel silicide can be obtained and integrated into the 30 nm ultrashallow junction formation.

Acknowledgment

The authors thank the National Science Council of the Taiwan for partially supporting this research under contract no. NSC 92-2215-E-009-022.

National Chiao-Tung University assisted in meeting the publication costs of this article.

References

1. B. Yu, Y. Wang, H. Wang, Q. Xiang, C. Riccobene, S. Talwar, and M. R. Lin, *Tech. Dig. - Int. Electron Devices Meet.,* **1999**, 509.
2. D. Lenoble, A. Grouillet, F. Arnaud, M. Haond, S. B. Felch, Z. Fang, S. Walther, and R. B. Liebert, in *Proceedings of Ion Implantation Technology Conference 2000*, 468 (2000).
3. G. Verma, C. Gelatos, S. Talwar, and J. C. Bravman, *IEEE Trans. Electron Devices,* **49**, 42 (2002).
4. J. F. DiGregorio and R. N. Wall, *IEEE Trans. Electron Devices,* **47**, 313 (2000).
5. K. B. Thei, W. C. Liu, H. M. Chuang, K. W. Lin, C. C. Cheng, C. H. Ho, C. W. Su, S. G. Wuu, and C. S. Wang, *IEEE Trans. Electron Devices,* **48**, 1740 (2001).
6. P. Liu, T. C. Hsiao, and C. S. Woo, *IEEE Trans. Electron Devices,* **45**, 1280 (1998).
7. C. Y. Lu, J. J. Sung, R. Liu, N. S. Tsai, R. Singh, J. Hillenius, and C. Kirsch, *IEEE Trans. Electron Devices,* **38**, 246 (1991).
8. G. G. Bentini, R. Nipoti, A. Armigliato, M. Berti, A. V. Drigo, and C. Cohen, *J. Appl. Phys.,* **57**, 270 (1985).
9. A. Lauwers, P. Besser, T. Gutt, A. Satta, M. de Potter, R. Lindsay, N. Rodlandts, F. Loosen, S. Jin, H. Bender, M. Stucchi, C. Vrancken, B. Deweerdt, and K. Maex, *Microelectron. Eng.,* **50**, 103 (2000).
10. W. L. Tan, K. L. Pey, Simon Y. M. Chooi, J. H. Ye, and T. Osipowicz, *J. Appl. Phys.,* **91**, 2901 (2002).
11. B. S. Chen and M. C. Chen, *IEEE Trans. Electron Devices,* **43**, 258 (1996).
12. K. Goto, J. Watanabe, T. Sukegawa, A. Fushida, T. Sakuma, and T. Sugii, in *Proceedings of IEEE Annual International Reliability Physics Symposium*, p. 363 (1998).
13. T. Morimoto, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, H. Okano, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, *Tech. Dig. - Int. Electron Devices Meet.,* **1991**, 653.
14. L. W. Cheng, S. L. Cheng, L. J. Chen, H. C. Chien, H. L. Lee, and F. M. Pan, *J. Vac. Sci. Technol. A,* **18**, 1176 (2000).
15. J. S. Maa, Y. Ono, D. J. Tweet, F. Zhang, and S. T. Hsu, *J. Vac. Sci. Technol. A,* **19**, 1591 (2001).
16. R. Pantel, D. Levy, D. Nicolas, and J. P. Ponpon, *J. Appl. Phys.,* **62**, 4319 (1987).
17. Y. Murakami, Y. Satoh, H. Furuya, and T. Shingyouji, *J. Appl. Phys.,* **84**, 3175 (1998).
18. C. J. Choi, Y. W. Ok, S. S. Hullavarad, T. Y. Seong, K. M. Lee, J. H. Lee, and Y. J. Park, *J. Electrochem. Soc.,* **149**, G517 (2002).
19. J. G. Yun, S. Y. Oh, H. H. Ji, B. F. Huang, Y. H. Park, J. S. Wang, and H. D. Lee, in *Proceedings of 4th International Workshop Junction Technology*, 131 (2004).
20. T. H. Hou, T. F. Lei, and T. S. Chao, *IEEE Electron Device Lett.,* **20**, 572 (1999).
21. T. L. Lee, J. W. Lee, M. C. Lee, T. F. Lei, and C. L. Lee, *Electrochem. Solid-State Lett.,* **6**, 66 (2003).
22. C. J. Choi, T. Y. Seong, K. M. Lee, J. H. Lee, Y. J. Park, and H. D. Lee, *IEEE Electron Device Lett.,* **23**, 188 (2002).
23. P. S. Lee, K. L. Pey, D. Mangelinek, J. Ding, D. Z. Chi, and L. Chan, *IEEE Electron Device Lett.,* **22**, 568 (2001).
24. Q. Xiang, C. Woo, E. Paton, J. Foster, B. Yu, and M. R. Lin, in *Proceedings of Symposium on VLSI Technology*, p. 76 (2002).

Downloaded on 2014-04-26 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).