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# Stress Migration and Electromigration Improvement for Copper Dual Damascene Interconnection

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Stress migration (SM) and electromigration (EM) were widely used to study the performance of interconnection process of metal/via formation in copper dual damascene of wafers. Necking and voids at the via bottom were important in causing failures in tests of stress migration and electromigration. In this report, the contamination of the bottom of via, which results in poor step coverage, the adhesion of seed layers, and poor copper grain formation are identified to be the underlying causes of the necking and void formation after the first EM and SM tests are performed. The contamination of the via formation processes included via etching, trench etching, and barrier/seed layer depositions. A well-shaped via profile can be optimized using three methods, the first involves Cu/SiN interface stress, the second involves Cu grain growth, and the third involves post via etching clean study. Eliminating the contamination of the via bottom and optimizing step coverage and adhesion of the barrier seed layers improve the EM and SM performance from time-to-fail = 13 to 59 s, in the copper-related processes for fabricating 300 mm wafers using technology that is beyond 0.13 μm technology.
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Copper (Cu) has been adopted in deep submicrometer ultralarge scale integration (ULSI) metallization and interconnection because it has low resistivity and better reliability than other metals.[1-4] A dual damascene process has been used for fabricating copper interconnections. Via/trenching etch, tantalum nitride (TaN) deposition, copper seed layer deposition, Cu electrochemical plating (ECP), and copper chemical mechanical polishing (CMP) are the major processes in the fabrication of dual damascene. Stress migration (SM) and electromigration (EM) tests are usually used to qualify the performance of the interconnection process associated with metal/via formation in copper dual damascene of wafers. Ogawa *et al.*[5] explained electromigration in terms of mass transport. Fischer *et al.*[6] established a strong correlation of electromigration failure with local defects from processes such as liner deposition, preclean, or trench etches. Tokei *et al.*[7] claimed that electromigration was influenced by argon preclean. Suzuki *et al.*[8] showed that the failure rate of stress migration depends on both the line width and via diameter. Ishikawa *et al.*[9] revealed that stress migration of Cu interconnects depends strongly on the adhesive strength of the barrier metal/Cu interface and the step coverage. Alers *et al.*[10] explained copper contamination of via sidewalls and interlevel dielectric (ILD) damage during sputter preclean affects stress migration. Ogawa *et al.*[11] showed stress-induced void formation under the via because grains of copper grew without thorough annealing. This brief review reveals that neither EM nor SM are clearly understood, because the contamination of via formation processes, including via etching, trench etching, and barrier/seed layer deposition, result in poor step coverage, poor adhesion of the seed layers, and poor copper grain formation. The contaminating material has not been analyzed.

This study introduces necking and voids in the EM and SM tests to identify the weak point of the copper process. The mechanisms of contamination in the dual damascene interconnections were investigated thoroughly. Clearly, eliminating the contamination at the via bottom improves the EM/SM. The weak point in the current copper interconnect process is addressed.

## Experimental

The testing structures consisted of metal chains that were 3.5 μm wide and 55 μm long with via holes 0.5 μm wide variously arranged for SM and EM, as shown in Fig. 1. Two film deposition and barrier TaN (TaN/Ta deposition with a Ta thickness of 1-15 nm) properties were examined to elucidate the effect of the interface between the SiN film and the Cu lines shown in Fig. 2. The nitride film was deposited with different plasma intensities. All experimental results were obtained with 0.13 μm technology and shallow trench isolation (STI), the cobalt-salicide process, dielectric deposition with fluorosilicate glass (FSG), and an etching stop layer with SiN and Cu damascene metallization. In SM testing, these samples were capped with plasma-enhanced chemical vapor deposition (PECVD) FSG, and then stored in a vacuum oven at 100-300°C for three weeks. In EM testing, the via arrangements were stressed at a constant current of 5 MA/cm$^2$ at 450°C. Cu voids, via bottom necking, and the adhesion between Cu and barrier TaN/SiN were observed by focused ion beam (FIB), scanning electron microscopy (SEM), and transmission electron microscopy (TEM) for Cu interconnect processes.

## Results and Discussion

SM is the phenomenon of metal voiding under tension in the stress of thermal processing. The voids grow until they sever a metal line, causing circuit failure.[12] Currently, IC manufacturers have no standard methodology of testing for SM. The failure criteria are usually specified increases, such as 10% in resistances. Figure 3 plots cumulated stress migration failure results. The failure analysis revealed that a void in the via was made by the copper pulled up. It was found after the SM test. The poor interface adhesion between the cap nitride and copper seed layers was the underlying cause shown in Fig. 4.

The basic flux equation for electromigration is given by[12-14]

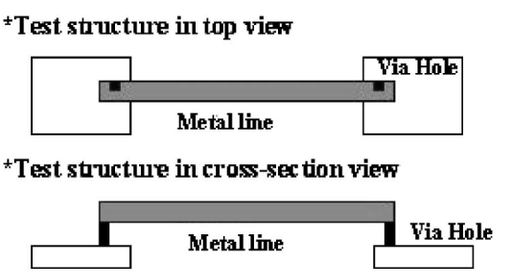


**Figure 1.** Testing structures consisted of metal chains 3.5 μm wide and 55 μm long and via hole 0.5 μm wide interconnected by differing arrays for stress migration.

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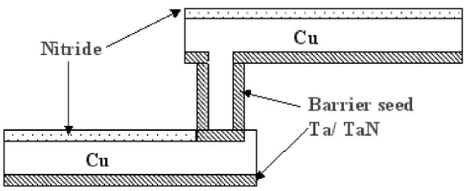


**Figure 2.** Dual damascene via scheme with TaN as barrier and Cu as metal material.

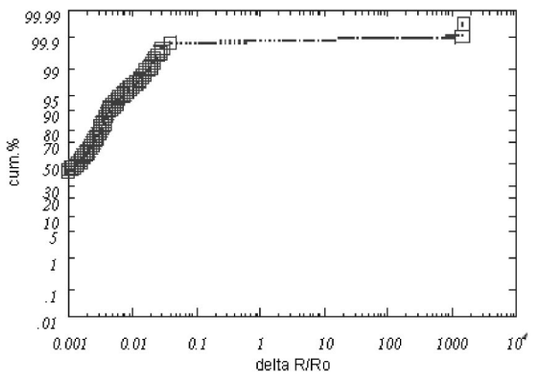


**Figure 3.** The cumulative plot of stress-migration points out via failure.

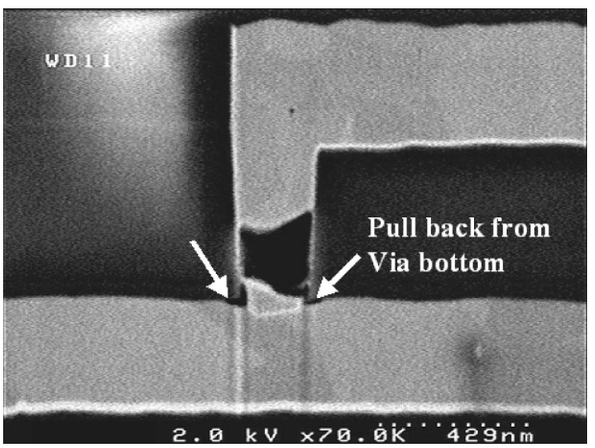


**Figure 4.** SEM image cross section analyzed via void because of copper pulled up due to poor interface adhesion between nitride and copper after stress migration test.

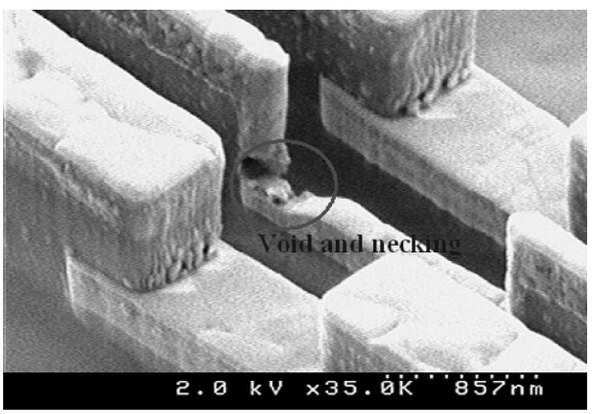


**Figure 5.** Top view of SEM failure analysis for electromigration failure site.

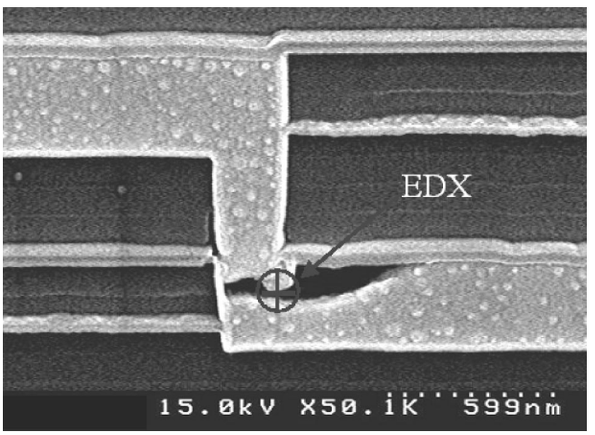


**Figure 6.** SEM image cross-sectional analysis for electromigration failure site.

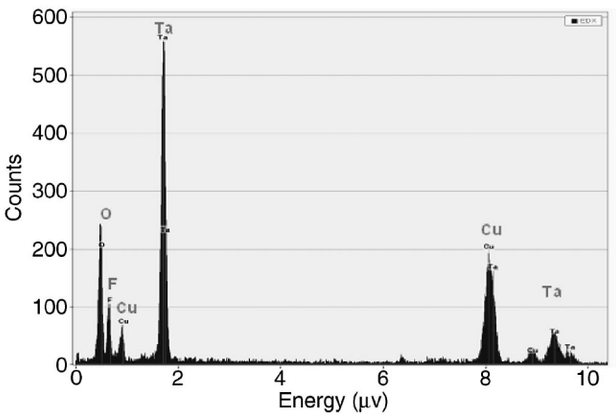


**Figure 7.** The EDX analysis showed the contamination with fluorine impurity at bottom via.

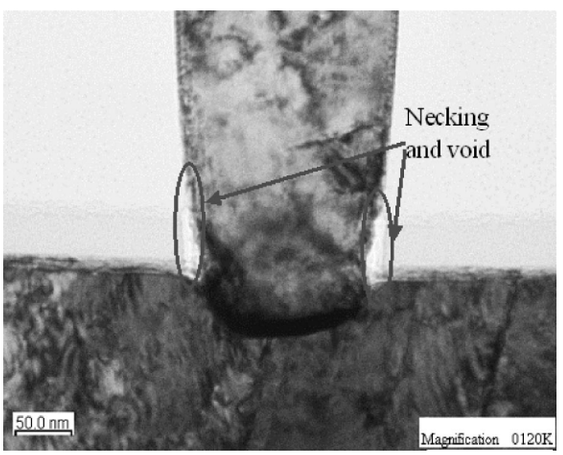


**Figure 8.** Necking and voiding vias were found because of the contamination.

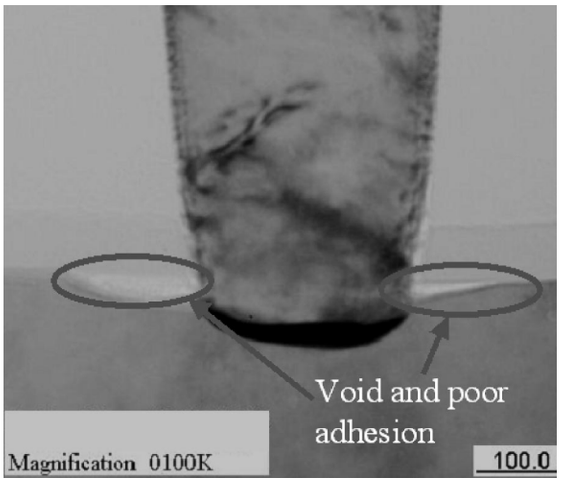


**Figure 9.** TEM cross-sectional photo shows via voids exists below nitride film and poor interface adhesion also made wafer reliability fail.

$$F_m = ND_o/kT(Z^*q\mathbf{E})\exp(-E_a/kT) \quad [1]$$

where $F_m$ is the ion flux, $N$ is the density of atoms, $D_o$ is the diffusion coefficient, $T$ is temperature, $k$ is the Boltzmann constant, $Z^*q$ is the effective ionic charge, **E** is the electric field, and $E_a$ is the activation energy distributed from 0.6 to 1.0 eV.[5,6] The EM of a metal interconnect is commonly determined by performing a lifetime experiment on a set of lines, to determine the time to failure (TTF). Black presented the general TTF expression[15,16]

$$TTF = AJ^{-n}\exp(E_a/kT) \quad [2]$$

where $A$ is a material constant based on the microstructure and geometric properties of the conductor, $J$ is the current density, and $E_a$ and $kT$ are as defined already. The TTF is usually plotted on a lognormal graph. The values of $T_{0.1}$ (time for 0.1% of the line to fail) and $T_{50}$ (time for 50% of the line to fail) are obtained from the fitted plot. Figure 5 and 6 show a voiding metal line at via bottom caused by poor gap filling of Cu that grows between the via and the metal after the EM test. Energy dispersive X-ray (EDX) analysis reveals that the voids in Fig. 6 retained contamination and impurities, especially fluorine, as shown in Fig. 7. Contamination with fluorine at the bottom of a via influences the stability of the interface, the step coverage, the adhesion of barriers, and the formation

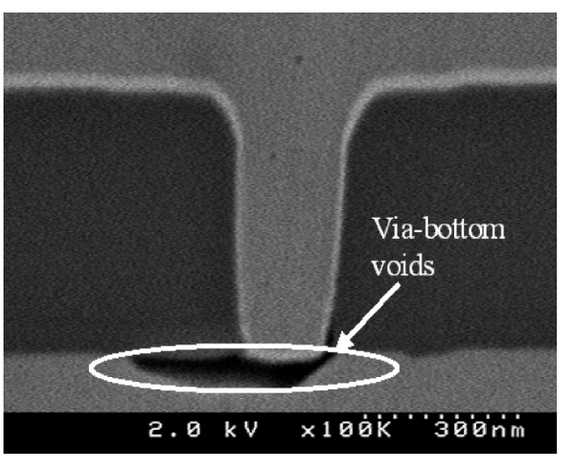


**Figure 10.** Contamination and impurities cause via voids.

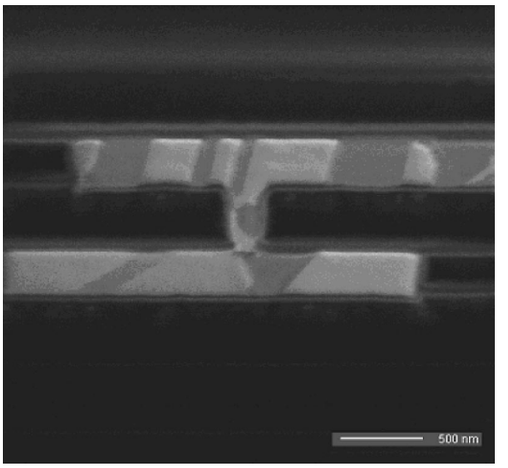


**Figure 11.** FIB cross section shows poor copper grain conformity that proceeded from polymer residue.

of copper grains causing necking, and yielding a void via as shown in Fig. 8-10. Cu dual damascene process integration degrades the via/metal contact resistance, causing SM to fail. Via necking and voids represent weak points in the dual damascene of Cu metal/via interconnection, which are associated with a key failure mode after SM and EM tests; as shown in Fig. 4-6, and 11. Fluorine contamination may come from the gases that react during the deposition of dielectric film (FSG film) at intermetal or the etching of the via/trench (carbon fluoride), and so is hard to prevent. Therefore, adequate via-cleaning is required to eliminate the contamination and impurities at the bottom of a via during via formation. Typical residues from etch and postetch treatments are nonwater soluble complexes with high fluorine, oxygen, and copper/metal contents. Hydrogen in water is the source of proton for the $Cu_xO_y$ bonds in the residue and allows the $F^-$ and $NH_4^+$ ions from the fluorine source to react with Cu molecules. Chelating compounds may be applied as passivating agents to block further reaction of the fluoride and hydroxyl ions in the solution to which the metal surfaces are exposed. Complexation with chelating compounds in the solution generates various soluble oligimers and dimers, enabling contaminating fluorine to be removed without damaging Cu

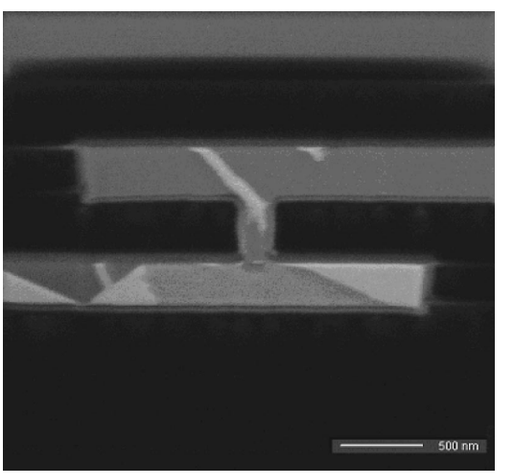


**Figure 12.** FIB cross section shows copper grain growth and formation after using sufficient etch-cleaning approach.

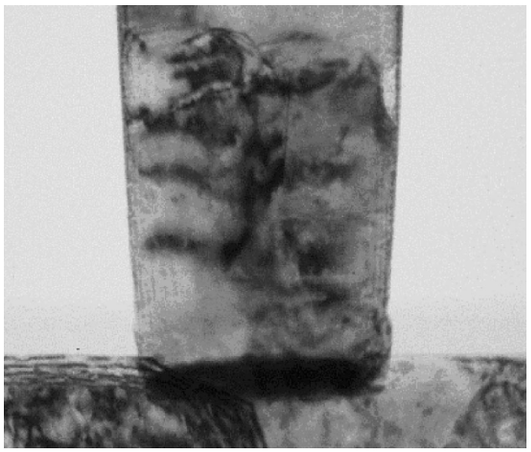

**Figure 13.** TEM analysis shows via structure without necking and void after using sufficient etch-cleaning approach.

$$Cu_xO_yH_zF_a + R\text{-}CO_2^- + H_2O + F^- \rightarrow CuF(OH)(C) + Cu_4F_6(H_2O)_2(C)_2 + \cdots \quad [3]$$

where $Cu_xO_yH_zF_a$ is left as a residue after via etching, $R\text{-}CO_2^-$ is chelating compounds.

The relationship between Cu grain growth and via void formation is crucial. Cu ECP involves Cu grain formation that is governed by grain size and conformity.

Lingk *et al.*[17,18] and Brongersma *et al.*[19] stated that electroplated Cu undergoes recrystallization and self-annealing at room temperature, in a process that is related to the presence of organic and inorganic additives in the plating bath affecting the formation of Cu grains. The experimental results reveal that the conformity of via grain may be improved by adequate via cleaning, which eliminates the inorganic contamination and the impurities as shown in Fig. 11 and 12. Figure 13, 15, 16, and 17 present that necking and voiding of the via are eliminated by adequate postetch cleaning, yielding good copper grain conformity. Figure 14 plots the cumulative failure *vs.* time for the EM test without (before) and with (after) adequate via cleaning, based on the parameters $n = 2$,[12] $E_a = 0.83$ eV,[6] and

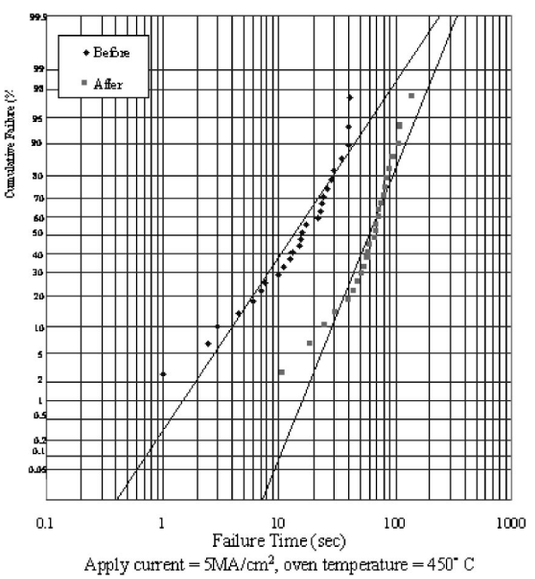


**Figure 14.** EM test result indicates that TTF may increase from 13 to 59 s.

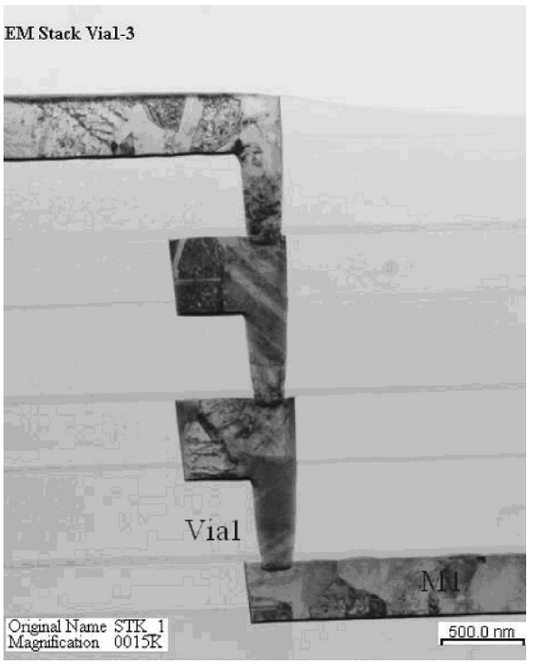


**Figure 15.** Stack via under TEM shows that it is void free.

$T = 450$ K in Eq. 2. The values of $t_{50}$ and $t_{0.1}$ are then obtained from the cumulative plot. Table I reveals that a fall in the amount of impurities leads to increasing TTF. Figure 14 and Table I reveal that the TTF in the EM test increases rapidly from 13 to 59 s, which trend is similar to that observed with adequate via cleaning.

Voiding occurs in the Cu via because of copper deficiency on the interface of TaN under the via. Impurities are critical to preventing Cu atom flux from fast diffusing along the Cu/barrier interface, thus eliminating void formation during EM testing. Therefore, the step coverage of barrier TaN, which is affected by impurities of via bottom, must be well controlled. Cu flux is considered to be discontinuous at the via bottom because impurities were attached to the barrier layer.

## Conclusion

This study addresses the effect of barrier film step coverage, adhesion, and Cu grain formation, and is a feasible candidate for

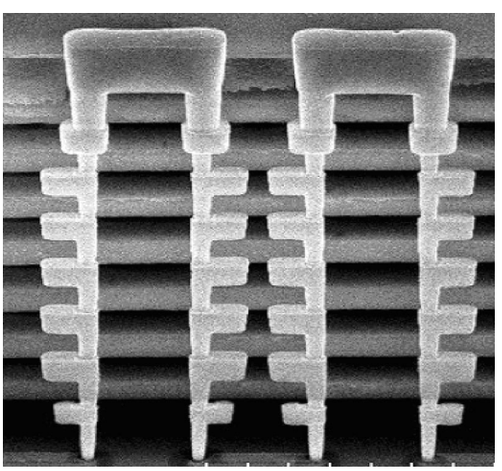

**Figure 16.** Structures of stack via are designed for via process certification. No voids appear.

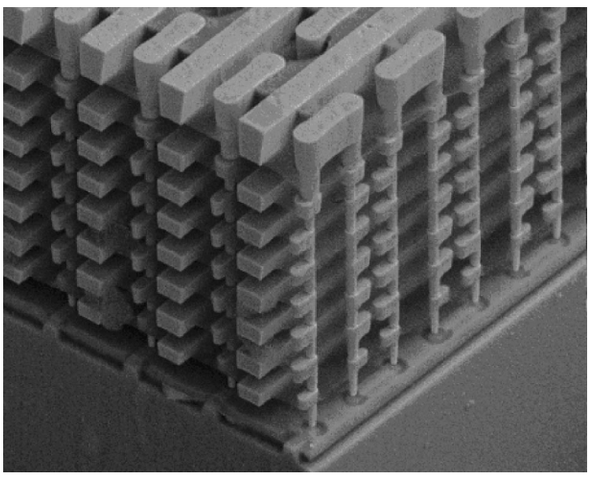

**Figure 17.** 3D view shows no voids existing for full process stack metal structure.

further integration into current copper metallization beyond 0.13 μm technology. Contaminating impurities were analyzed as being responsible for early failure; the same contamination was observed under several reliability testing conditions, indicating that EM and SM occur. Necking and voids at the via bottom were the main factors that caused the failure of SM and EM testing. Fluorine contamination may come from the gases that react in dielectric film deposition (FSG film) at intermetal layer or via/trench etching (carbon fluoride), and is hard to prevent. Therefore, adequate via cleaning is required to eliminate the contamination and impurities at the via bottom. Contamination occurred during via formation processes, including via etching, trench etching, and barrier/seed layer deposition. The EM test revealed that the TTF increases rapidly from 13 to 59 s when adequate via cleaning is applied.

**Table I. The EM performance showed that TTF was improved from TTF 13-59 s.**

| Results | Before | After |
|---|---|---|
| Sigma | 0.94 | 0.56 |
| $t_{50}$ (s) | 13.31 | 59.16 |
| $t_{0.1}$ (s) | 0.73 | 10.33 |
| $J_{max}$ (mA) | 0.301 | 1.129 |

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