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Bias-Temperature Instability on Fully Silicided-Germanided Gates/High-*k* Al_2O_3 CMOSFETs

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We have studied bias-temperature instability (BTI) on fully nickel-silicided (NiSi) and germanided (NiGe) gates on high-*k* Al_2O_3 n metal oxide semiconductor field effect transistors (MOSFETs) and pMOSFETs, respectively. At an equivalent oxide thickness of 1.7 nm, the NiSi/Al_2O_3 pMOSFETs and NiGe/Al_2O_3 nMOSFETs have a comparable threshold voltage (V_t) change of −34 and 33 mV at 85°C and 10 MV/cm stress for 1 h. This result is different from the more severe negative BTI (NBTI) degradation measured in oxynitride pMOSFET than positive BTI (PBTI) in nMOSFET. The extrapolated maximum voltage for 10 years' lifetime is 1.16 and −1.12 V from NiSi-NiGe/Al_2O_3 complementary MOSFETs (CMOSFETs) that can barely meet the required 1 V operation with 10% safety margin. Further improvement is still required because the 1.8 nm oxynitride CMOSFETs have higher 10 years' lifetime operation voltages of 2.48 and −1.52 V for PBTI and NBTI, respectively.
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The continuous scaling down of metal oxide semiconductor field effect transistor (MOSFET) devices to the sub-100 nm scale requires oxynitride or metal oxide high-*k* gate dielectrics, with an ultrathin equivalent oxide thickness (EOT), to replace the conventional SiO_2 to reduce the gate dielectric leakage current. To further increase the drive current in the MOSFET, a metal gate is integrated with these high-*k* gate dielectrics.[1-5] However, one of the main concerns of such metal gate/high-*k* MOSFETs is the poor bias-temperature instability (BTI).[1,6-8] In particular, the negative BTI (NBTI) of pMOSFETs is becoming an increasingly serious problem for complementary metal oxide semiconductor (CMOS) reliability. The NBTI of oxynitride gate dielectric pMOSFETs is mainly related to, *e.g.*, nitrogen traps,[9-12] hydrogen,[13,14] moisture (H_2O),[14] and impurity diffusion.[6] Both NBTI and positive BTI (PBTI) are even worse in metal oxide high-*k* CMOSFETs than in oxynitride devices.[1,6-8] In this paper, we have studied the BTI effect on fully silicided-germanided (NiSi-NiGe) dual gates on high-*k* Al_2O_3 CMOSFETs[5,15-19] and compared the results with those of benchmark oxynitride devices. The fully silicided gate has the advantage of full process compatibility to current very-large-scale integrated fabrication technology. The Al_2O_3 gate dielectric has a reasonably high *k* and good thermal stability for the amorphous type up to 1000°C.[5,12,15-21] In contrast to the worse NBTI than PBTI found in oxynitride devices, the NBTI and PBTI are close in fully NiSi-NiGe gate/Al_2O_3 CMOSFETs. At 1.7 nm EOT, the extrapolated maximum operation voltage ($V_{max\text{-}10\ years}$) for 10 years' lifetime, with 50 mV threshold voltage (V_t) change at 85°C, is 1.16 and −1.12 V from PBTI and NBTI, respectively. These results are comparable with or better than the reported HfAlON[6] and HfSiON data.[7] The high $V_{max\text{-}10\ years}$ and close value for both NBTI and PBTI may be due to the processes without hydrogen and H_2O that were used during high-*k* HfAlON and HfSiON deposition by atomic layer deposition using NH_3 and H_2O sources.[6] However, the inferior PBTI of NiSi-NiGe/Al_2O_3 CMOSFETs to that of oxynitride devices suggests that further improvement of the high-*k* dielectric quality is required.

Experimental

Standard n- and p-type Si(100) wafers with a typical resistivity of ~10 Ω-cm were used in this study. After standard cleaning, the device active region was formed by thick field oxide and patterning. The source and drain regions were implanted by 35 keV phosphorus or 25 keV boron for nMOSFETs or pMOSFETs, respectively, followed by a 950°C rapid thermal anneal (RTA) activation. Then the ~3.9 nm Al_2O_3 was formed by physical vapor deposition, 400°C oxidation for 20 min, and 400°C anneal for 20 min. From the capacitance-voltage (C-V) measurement, a *k* value of 8.9 and an EOT of 1.7 nm were obtained. The slightly lower *k* value than that for the bulk Al_2O_3 ($k = 10$) is due to the oxidation of Si during

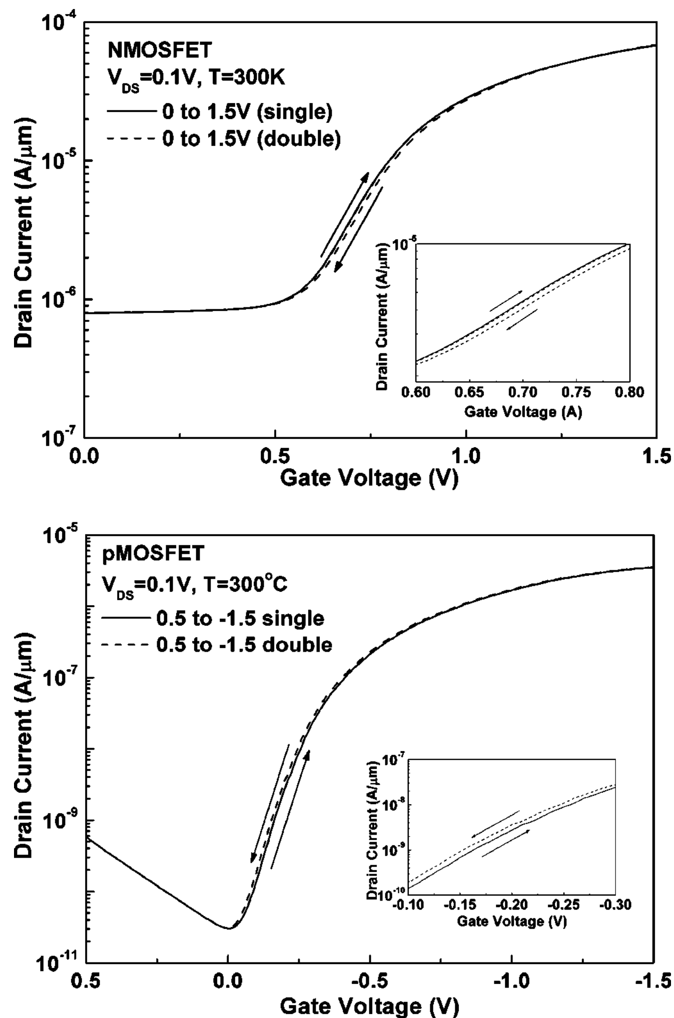

Figure 1. Room-temperature I_{ds}-V_{gs} characteristics of (top) NiSi/Al_2O_3 nMOSFETs and (bottom) NiGe/Al_2O_3 pMOSFETs under double sweep measurements. Insets are enlarged views to show hysteresis.

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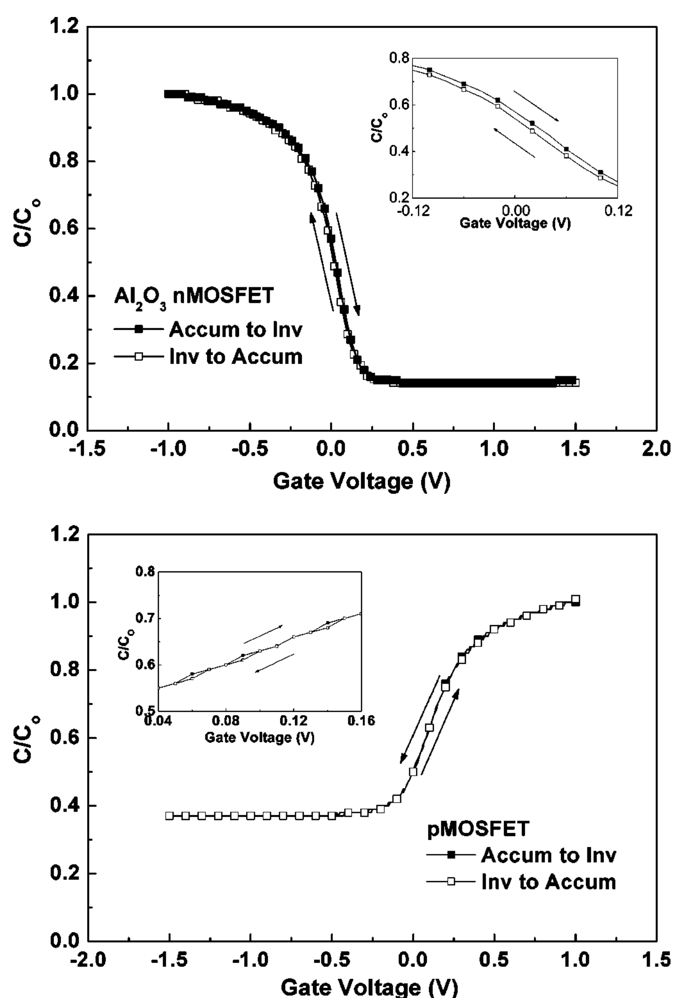

Figure 2. Room-temperature C-V characteristics of (top) $NiSi/Al_2O_3$ nMOS and (bottom) $NiGe/Al_2O_3$ pMOS capacitors under double sweep measurements. Insets are enlarged views to show hysteresis.

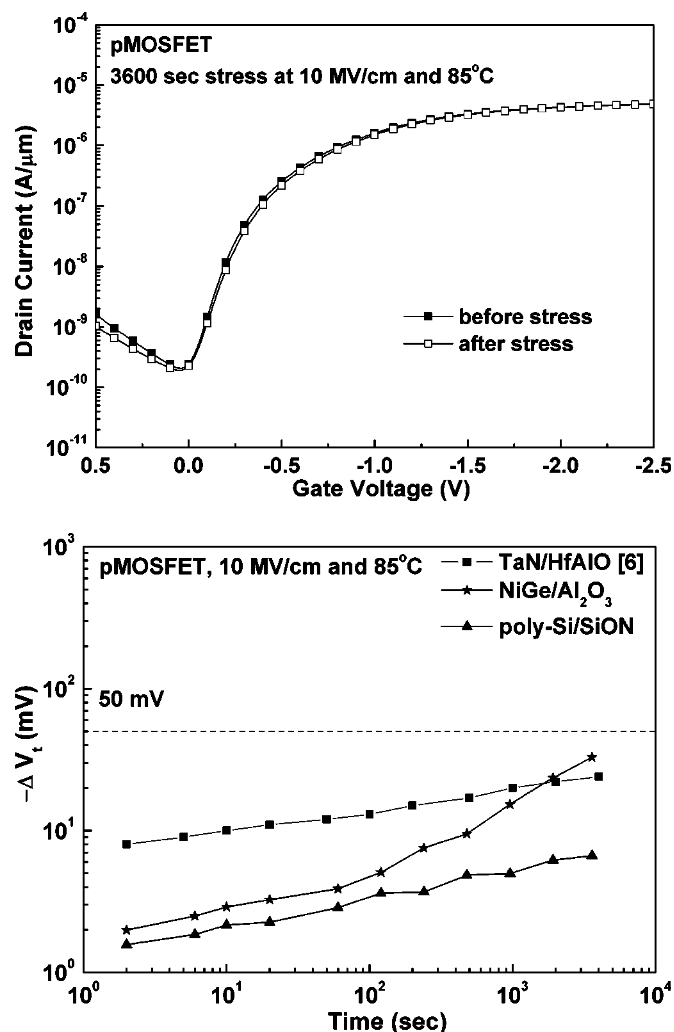

Figure 3. (Top) I_{ds}-V_{gs} and (bottom) ΔV_t changes of $NiGe/Al_2O_3$ pMOSFETs stressed at 85°C and 10 MV/cm for 1 h. For comparison, data from poly-Si/SiON and TaN/HfAlO (from Ref. 6) are also included under the same stress condition.

postdeposition annealing. The fully NiSi and NiGe gates were formed by depositing 15 nm amorphous Si or Ge on Al_2O_3, 15 nm Ni for both n- and p-devices, and then silicidation and germanidation at 400°C RTA for 30 s.[5,15-19] For comparison, a control oxynitride was formed by decoupled plasma nitridation[22] on a 1.8 nm SiO_2 that was grown by oxygen at 700°C for 12 min. The formed oxynitride has a peak N concentration of 9% near the polygate interface, following a postdeposition annealing. The fabricated CMOSFETs were further characterized by C-V, current-voltage (I-V), and bias-temperature (BT) measurements.

Results and Discussion

We first measured the I_{ds}-V_{gs} characteristics to examine the hysteresis effects in Al_2O_3. Figure 1(top) and (bottom) shows the measured hysteresis on $NiSi/Al_2O_3$ nMOSFETs and $NiGe/Al_2O_3$ pMOSFETs, respectively. For fully silicided/high-k nMOSFETs, the double sweep of gate voltage from 0 to 1.5 V results in V_t shifted positive by +10 mV. This result suggests the generation of negative charge traps in nMOSFET. For pMOSFETs, the double sweep of gate voltage from 0.5 to − 1.5 V results in V_T shifted negative by −10 mV, which also indicates generation of positive charge traps in the bulk Al_2O_3 and the Al_2O_3/Si interface. These amounts of charge trappings may cause NBTI in pMOSFETs and PBTI in nMOSFETs. The poor I_{off} in nMOS is due to the insufficient high-temperature of the annealing (only 950°C RTA) for ion-implanted damage. The limited RTA temperature also gives a relatively poor subthreshold swing because of the insufficient annealing of high-k dielectric defects. Further improving the leakage current and subthreshold swing can be done by increasing the RTA temperature to a typical 1000-1050°C or by using an $LaAlO_3$ high-k dielectric.[23,24]

We have also used C-V to measure the hysteresis effects. Figure 2 (top) and (bottom) show the CV hysteresis characteristics, measured at 500 kHz, on $NiSi/Al_2O_3$ nMOSFETs and $NiGe/Al_2O_3$ pMOSFETs, respectively, where conventional bidirectional sweeps from inversion to accumulation were applied to these transistors. A double sweeping hysteresis of +10 and ∼0 mV is measured for the nMOS and pMOS capacitors, respectively. The smaller flatband voltage shift of the pMOS capacitor than the V_t shifts of the I_{ds}-V_{gs} curves in the $NiGe/Al_2O_3$ pMOSFETs may be due to the relatively slower and deeper traps that were unable to follow the AC signal.[25] A similar effect is also observed in other high-k dielectrics from the quasi-static to the radio-frequency range.[26-29]

Figure 3 (top and bottom) shows the NBTI characteristics of I_{ds}-V_{gs} and V_t change (ΔV_t), respectively, for $NiSi/Al_2O_3$ pMOSFETs stressed at 10 MV/cm electric field and 85°C ambient for 1 h. This stress condition was chosen for comparison with published data in the literature.[6,7] For reference and comparison, the ΔV_t of SiON pMOSFETs and the data of TaN/HfAlO[6] are also plotted in Fig. 3(bottom). After 1 h stress at 10 MV/cm and 85°C, a ΔV_t of

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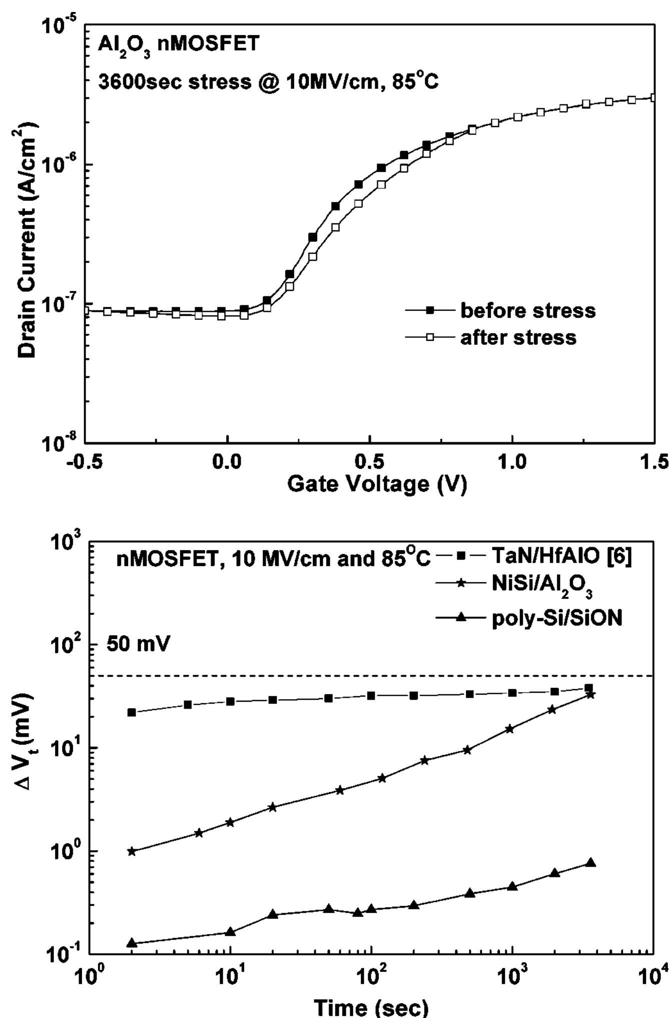

Figure 4. (Top) I_{ds}-V_{gs} and (bottom) ΔV_t changes of NiSi/Al_2O_3 nMOSFETs stressed at 85°C and 10 MV/cm for 1 h. For comparison, the data from poly-Si/SiON and TaN/HfAlO (from Ref. 6) are also included under the same stress condition.

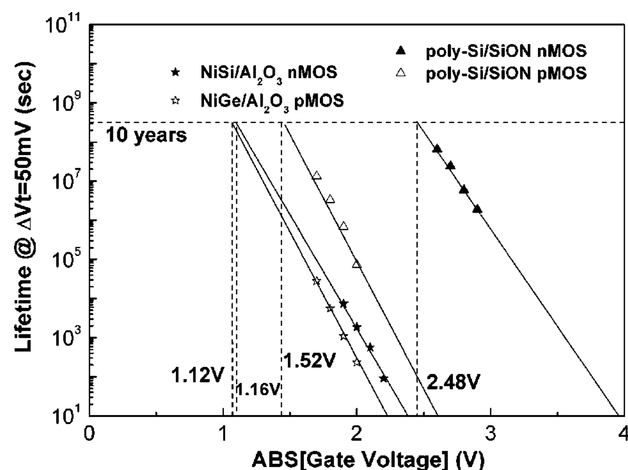

Figure 5. Extrapolated maximum operation voltage for 10 years' lifetime of NiSi/Al_2O_3 nMOSFETs and NiGe/Al_2O_3 pMOSFETs under failure condition of 50 mV change in V_t at 85°C. Data from oxynitride is also added for comparison.

−33 mV is measured, suggesting that the NBTI is one of the most serious reliability issues for fully NiSi gate/high-*k* Al_2O_3 pMOSFETs. The measured ΔV_t changes are comparable with or better than the published data for HfAlON[6] [also plotted in Fig. 3(bottom)], HfSiON,[7] and HfTaO,[1] where additional Al, N, Si, or Ta must be added to HfO_2 for BTI reliability improvement. However, the measured ΔV_t is still larger than that of oxynitride devices with plasma-generated N at the top poly-Si/oxynitride interface. A possible reason for the inferior NBTI is the degraded interface of Al_2O_3/Si and the bulk oxide change in Al_2O_3; the oxygen-riched SiN interface on Al_2O_3 is a possible solution for this important reliability issue.[10,12]

Figure 4(top) and (bottom) shows the PBTI characteristics of I_{ds}-V_{gs} and ΔV_t, respectively, for NiGe/Al_2O_3 nMOSFETs stressed at 10 MV/cm electric field and 85°C for 1 h. The ΔV_t data of SiON nMOSFETs and TaN/HfAlO[6] are also included in Fig. 4(bottom) for comparison. After 1 h BT stress, a ΔV_t of 34 mV is measured for PBTI, which is close to the $|-33 \text{ mV}|$ value for NBTI. In sharp contrast, an NBTI of only 0.76 mV is measured in poly-Si/oxynitride (9% peak at poly-Si interface) nMOSFETs after the same BT stress; this is lower than the 6.6 mV change in oxynitride pMOSFETs. The better PBTI than NBTI is normal for oxynitride MOSFETs, where the mechanism is attributed to hole injection to break the H-Si bonds and create interface traps.[9-14] However, the measured NBTI and PBTI values are less than that of HfO_2,[7,8] which may be due to the strong Al-O bond and consistent with the results in HfAlO.[6] The close PBTI and NBTI absolute values after BT stress in Al_2O_3 MOSFETs are related to the higher number of interface and bulk traps, which is normal for high-*k* gate dielectrics, and is the main reason for the larger $|\Delta V_t|$ change in high-*k* gate dielectrics than in oxynitride devices.

We also measured the BTI at other gate electric fields for 10 years' lifetime projection, where the lifetime at each gate voltage was defined by a $|\Delta V_t| = 50$ mV change during stress. Such a high gate voltage or electric field is especially required for poly-Si/SiON CMOS due to the excellent reliability. Figure 5 shows the lifetime as a function of V_{gs} for nMOSFETs and pMOSFETs, respectively. The 10 years' lifetime $V_{\text{max-10 years}}$ is from the extrapolation of measured data at high gate voltage. The extrapolated $V_{\text{max-10 years}}$ values are 1.16 and −1.12 V for Al_2O_3 nMOSFETs and pMOSFETs, respectively. Theses values can barely meet the BTI requirement at 1 V operation with additional 10% safety margin to 1.1 V. Note that a degraded PBTI is also reported in HfAlON gate dielectric MOSFETs,[6] which is even worse than the NBTI and attributed to gate impurity diffusion. The close $V_{\text{max-10 years}}$ for PBTI and NBTI in Al_2O_3 MOSFETs simply occurs because no impurity,[6] hydrogen annealing,[13,14] or processing water[6,14] was added to the fully NiSi-NiGe/Al_2O_3 CMOSFETs. Unfortunately, these values are lower than the 2.48 and −1.52 V for PBTI and NBTI, respectively, extrapolated for oxynitride MOSFETs at close EOT. The main mechanism for NBTI degradation in poly-Si/SiON pMOS is due to the trap generation by energetic holes in the bulk oxide and interface. In contrast, the poorer BTI in high-*k* Al_2O_3 MOSFETs may be directly related to the existing high bulk and interface traps. Therefore, further technological development to reduce these traps or the use of an oxygen-rich SiN interface beneath the high-*k*[10,12] is a key factor for metal gate/high-*k* CMOS BTI reliability.

Conclusion

We have studied the NBTI and PBTI of 1.7 nm EOT NiSi-NiGe/Al_2O_3 CMOSFETs, with baseline characteristics of 10 mV hysteresis. The comparable V_t change of −34 and 33 mV for respective NBTI and PBTI, after 10 MV/cm and 85°C stress for 1 h, is probably due to the lack of impurities in the NiSi or NiGe gate and the fact that no hydrogen or water is used in the device process. The amount of V_t change and the extrapolated $V_{\text{max-10 years}}$ of 1.16 and −1.12 V in NiSi-NiGe/Al_2O_3 CMOSFETs are comparable with or better than the reported BTI data of HfSiON and HfA-

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lON, suggesting a good high-*k* device integrity. Although the $V_{max\text{-}10\ years}$ of NiSi-NiGe/Al_2O_3 CMOSFETs can barely meet the 1 V operation requirement, better performance is found in oxynitride CMOSFETs with a higher $V_{max\text{-}10\ years}$ of 2.48 and −1.52 V for PBTI and NBTI, respectively. In addition to having almost the same NBTI and PBTI values in NiSi-NiGe/Al_2O_3 CMOSFETs, comparison with oxynitride CMOSFETs suggests that the bulk and interface oxide traps in high-*k* Al_2O_3 dielectric play a dominant role for BTI. Therefore, further improving the device performance is required for metal gate/high-*k* CMOSFETs including BTI and mobility degradation effects.

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