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Effects of Channel Width and NH_3 Plasma Passivation on Electrical Characteristics of Polysilicon Thin-Film Transistors by Pattern-Dependent Metal-Induced Lateral Crystallization

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This work studied the effects of channel width and NH_3 plasma passivation on the electrical characteristics of a series of pattern-dependent metal-induced lateral crystallization (PDMILC) polysilicon thin-film transistors (poly-Si TFTs). The performance of PDMILC TFTs improves as each channel width decreasing. Further, PDMILC TFTs with NH_3 plasma passivation outperforms without such passivation, resulting from the effective hydrogen passivation of the grain-boundary dangling bonds, and the pile-up of nitrogen at the SiO2/poly-Si interface. In particular, the electrical characteristics of a nanoscale TFT with ten 67 nm wide split channels (M10) are superior to those of other TFTs. The former includes a higher field effect mobility of 84.63 cm^2/V s, a higher ON/OFF current ratio ($>10^6$), a steeper subthreshold slope (SS) of 230 mV/decade, and an absence of drain-induced barrier lowering (DIBL). These findings originate from the fact that the active channels of the M10 TFT have exhibit the most poly-Si grain enhanced to reduce the grain boundary defects and the best NH_3 plasma passivation. Both effects can reduce the number of defects at grain boundaries of poly-Si in active regions for high performances.
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The major attraction of applying polycrystalline silicon thin-film transistors (poly-Si TFTs) in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility (larger than 10 cm^2/V s) in poly-Si film and the capability of integrating the pixel switching elements, the panel array, and the peripheral driving circuit on the same substrate,[1-3] bring the era of system-on-panel (SOP) technology. For making high performance poly-Si thin film transistors (TFTs), low-temperature technology is required for the realization of commercial flat-panel displays on inexpensive glass substrates, which the maximum process temperature is limited to less than 600°C. There are three major low-temperature amorphous-Si crystallization methods to achieve high performance poly-Si thin film: solid phase crystallization (SPC),[4] excimer laser crystallization (ELC),[5] and metal-induced lateral crystallization (MILC).[6-10] MILC technology was initially developed as a low-temperature crystallization technique compared to other low-temperature poly-Si technologies such as ELC or conventional SPC. MILC is superior because, unlike ELC, it is a low-cost batch process and, unlike SPC, a better quality poly-Si thin film can be obtained. In addition, the presence of poly-Si grain boundary defects in the channel region of TFTs drastically affects the electrical characteristics, especially when the device dimension is scaled down. Therefore, reducing the number of polysilicon grain boundary defects will improve the performance of poly-Si TFTs. The poly-Si TFTs with several multichannels have been reported to effectively reduce grain boundary defects.[11,12] Thus, we demonstrate a practicable method to reduce the poly-Si grain boundary defects by using a structure modulation MILC process (*i.e.*, PDMILC) to fabricate the high performance TFTs. Moreover, NH_3 plasma passivation[13] has been reported to reduce the number of trap states in poly-Si grain boundaries, yielding high-performance poly-Si TFTs. Therefore, in this work the effects of channel width and NH_3 plasma passivation on the electrical characteristics of a series of multichannels with different widths PDMILC poly-Si TFTs were investigated.

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Device Structure and Fabrication

In this work a series of PDMILC TFTs, with a gate length of 5 μm, consisting of ten strips of multiple 67 nm wire channels (M10) TFT, five strips of multiple 0.18 μm channels (M5) TFT, two strips of 0.5 μm channels (M2) TFT, and a single-channel structure (S1) with width of 1 μm TFT, were fabricated, as listed in Table I. Figure 1a shows a schematic plot and Fig. 1b shows a top view of PDMILC TFT with source, drain, gate, nanowires channels and MILC seeding window. Figure 1c shows the cross-section view of PDM-TFT, which was a conventional top-gate, offset metal-oxide-semiconductor field-effect transistor (MOSFET) structure.

The 6 in. p-type single crystal silicon wafers were coated with 400 nm thick SiO_2 as the starting materials. Undoped 50 nm thick amorphous-Si (a-Si) layer were deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C. Then the active islands, including source, drain, and ten nanowire channels were patterned by electron beam lithography (EBL) and transferred by reactive ion etching (RIE). After defining the active region, the 25 nm thick tetraethylorthosilicate (TEOS) SiO_2 was deposited by LPCVD as gate insulator. Then, 150 nm thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100 nm thick TEOS-SiO_2 layer used as a passivation layer was deposited by LPCVD. The poly-Si gate sidewall TEOS-SiO_2 formed a self-aligned offset spacer with a width of 0.1 μm, as shown in Fig. 1c. Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Then, a thin 10 nm thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550°C for 48 h in an N_2 ambient. The average lateral crystallization length was about 30 μm, as shown in Fig. 2b (inset). After annealing for a long time, the unreacted nickel on passivative TEOS-SiO_2 were removed by a H_2SO_4 solution at 120°C within 10 min. Phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted through the passivative TEOS-SiO_2 to form the n+ gate, the source/drain regions and the self-aligned offset region were formed in the same process step, as shown in Fig. 1c. Next, the dopants were activated by rapid thermal annealing at 850°C with 30 s. The 300 nm thick aluminum (Al) layer was de-

Table I. Devices dimension of S1, M2, M5, and M10 PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 25 nm.

Device name	Gate length, L (μm)	Channel number	Each channel width, W (μm)	Effective channel width, W_{eff} (μm)
S1	5	1	1	1
M2	5	2	0.5	1
M5	5	5	0.18	0.9
M10	5	10	0.067	0.67

posited by PVD and patterned for source, drain, and gate metal pads. Then, the finished devices were sintered at 400°C for 30 min in an N_2 ambient. Finally, each device was passivated by a NH_3 plasma treatment for 2 h at 300°C.

Results and Discussion

Figure 2a presents an after etching investigation scanning electron microscope (SEM) photograph of the poly-Si active region of the M10 TFT, including the source, the drain, ten multiple nanowire channels, and the MILC seeding window. The inset plot of Fig. 2a presents a magnified area of the multiple nanowire channels in the M10 TFT, each of which is 67 nm wide. Figure 2b presents a SEM photograph of the MILC poly-Si grains in the active region of the proposed TFTs. The average grain size in the poly-Si channel formed by MILC is approximately 250 nm. The inset optical microscopy photography depicts a MILC length of 30 μm, which is longer than 16 μm (Fig. 1a), to ensure that the whole active channel was crystallized by the MILC process.

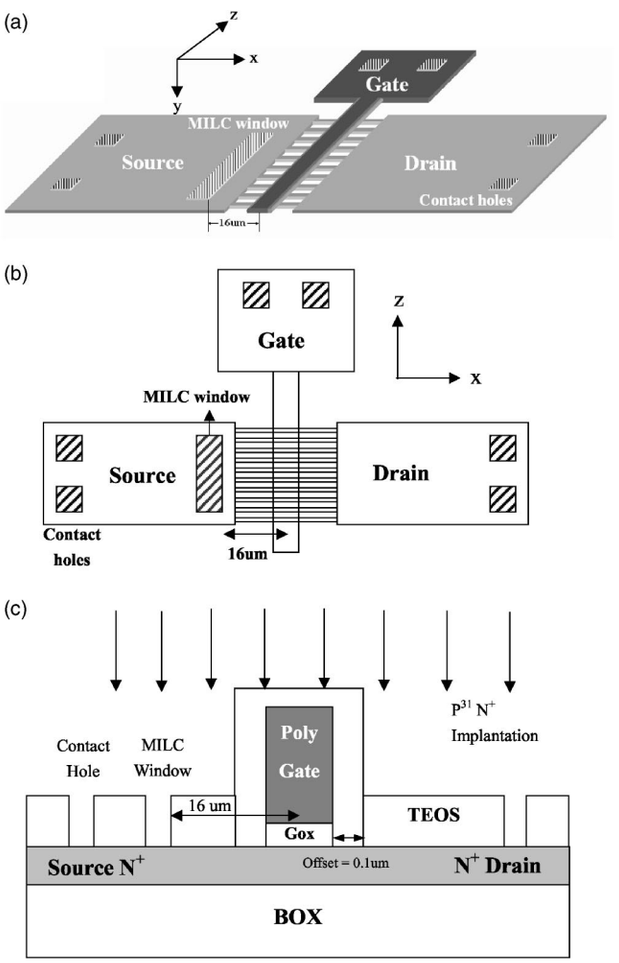

Figure 1. (a) Schematic plot of PDMILC poly-Si TFT with source, drain, gate, ten nanowires channels, contact holes and MILC seeding window. (b) Top view of PDMILC poly-Si TFT. The key process flows are active region pattering, gate patterning, MILC seeding window and contact holes patterning, and all metal pads pattering. (c) Cross-sectional view of PDMILC poly-Si TFT, which was a conventional MOSFET with offset structure.

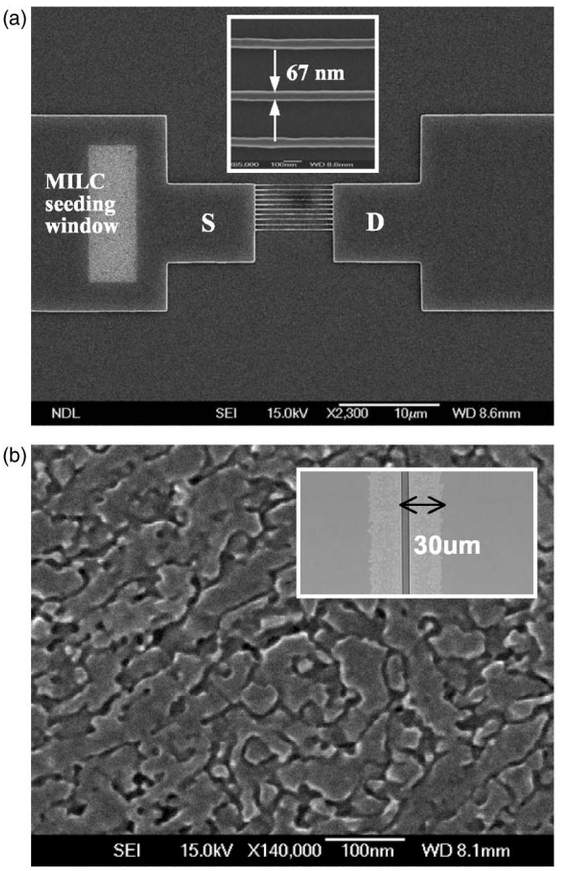

Figure 2. (a) SEM photography of active pattern with the source, the drain, ten nanowire channels and MILC seeding window. The inset plot shows the each nanowire width of 67 nm. (b) SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm. The inset optical microscopy photography depicts a MILC length of 30 μm.

Figure 3a-d shows that the S1, M2, M5, and M10 PDMILC TFTs transfer characteristics with and without NH_3 plasma passivation. These results reveal that device performance was enhanced with a decrease in each channel width. Meanwhile, the device that had undergone NH_3 plasma passivation outperforms that without NH_3 plasma passivation. The former has a higher field effect mobility (μ_{FE}), a higher ON/OFF ratio, a lower threshold voltage (V_{th}), a lower subthreshold slope (SS), and a lower drain-induced barrier lowering (DIBL). The device parameters *vs*. multichannels with different widths are plotted to elucidate the effect of NH_3 plasma passivation on each of the dimensions of PDMILC TFTs.

Figure 4 plots the μ_{FE} of the PDMILC TFTs *vs*. the multichannels with different widths, with and without NH_3 plasma passivation. The μ_{FE} is extracted from the linear region (V_d = 0.1 V) of transconductance (g_m). This curve reveals that μ_{FE} of PDMILC TFT was enhanced with a decrease of each channel width. (or the number of channels increases). The results suggest that during the MILC process, the poly-Si grain lateral length increases as the channel

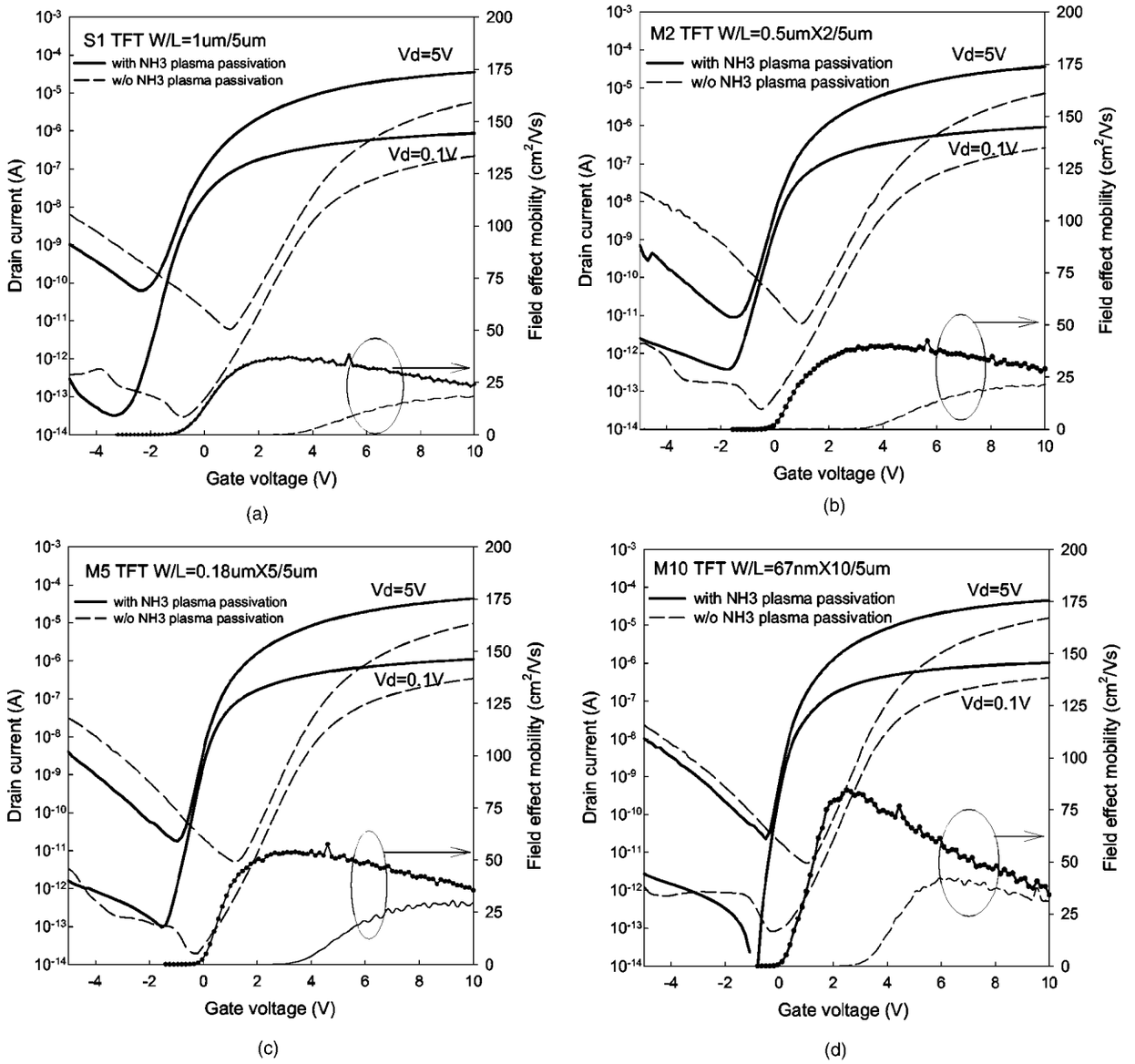

Figure 3. Device transfer characteristics I_d-V_g curve of (a) S1 (W/L = 1 μm/5 μm), (b) M2 (W/L = 0.5 μm × 2/5 μm), (c) M5 (W/L = 0.18 μm × 5/5 μm), and (d) M10 (W/L = 67 nm × 10/5 μm) PDMILC poly-Si TFT, with (solid line) and without (dash-line) NH_3 plasma passivation.

width declines. Therefore, the grain boundary defects of ploy-Si will be reduced to increase the mobility. Moreover, NH_3 plasma passivation further improves the μ_{FE} of a PDMILC TFT, suggesting that the NH_3 plasma effectively hydrogen passivated the dangling bonds at the grain boundary and the pile up of nitrogen at the SiO_2/poly-Si interface. In particular, the M10 PDMILC TFT has the most improved μ_{FE} at 84.63 cm^2/V s, because it has a split nanowire structure, which can greatly enhance poly-Si gain during the MILC process, and is exposed most effectively to an atmosphere of NH_3 plasma. Figure 5 plots the V_{th} of the PDMILC TFTs *vs.* the multichannel with different widths. The V_{th} is defined by constant current extraction, as the gate voltage required to yield normalized drain current of $I_d/(W/L) = 10^{-7}$ A at V_d = 5 V. After NH_3 plasma passivation, the V_{th} of each TFT device was approximately 4 V lower. Because of NH_3 plasma passivation reduced the barrier height (E_B) of the poly-Si grain boundary, the electrons can easily overcome E_B, producing a high current and allowing the TFT to be easily turned on. Also, the pileup of nitrogen at the SiO_2/poly-Si interface will

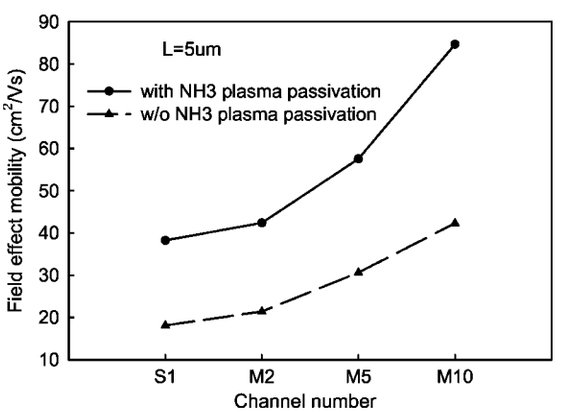

Figure 4. μ_{FE} of PDMILC poly-Si TFTs *vs.* multichannels with different widths, with and without NH_3 plasma passivation.

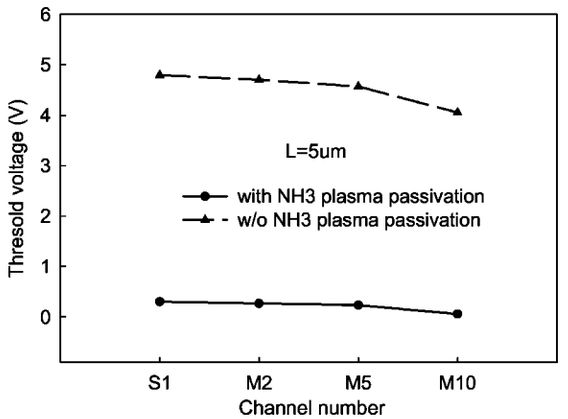

Figure 5. V_{th} of PDMILC poly-Si TFTs *vs.* multichannels with different widths, with and without NH_3 plasma passivation.

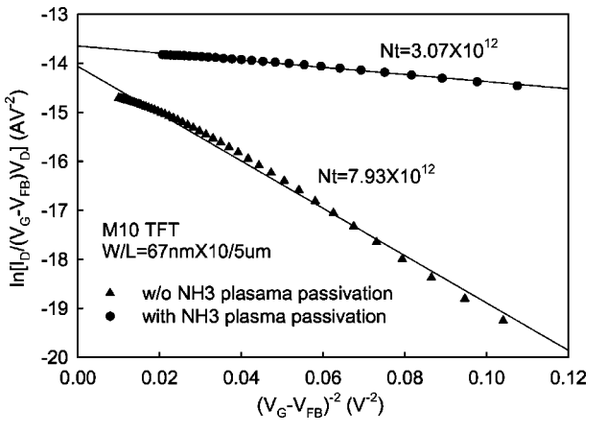

Figure 7. Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

reduce the interface trap density. Such a low value of V_{th} of the PDMILC TFT is appropriate in low-power AMLCD applications. Figure 6 plots the subthreshold swing (SS) of the PDMILC TFTs *vs.* the multichannels with different widths, with and without NH_3 plasma passivation. The parameter SS is directly related to the total trap states density (N_T) by[14]

$$SS = \left(\frac{kT}{q}\right)\ln 10\left(1 + \frac{q^2 t_{Si} N_T}{C_{ox}}\right)$$

where kT is thermal energy, C_{ox} is the gate oxide capacitance per unit area, and t_{Si} is the poly-Si layer thickness. Before NH_3 plasma passivation, the results reveal the decline of SS as each channel width decreases from S1, M2, and M5 to M10 TFT, and suggests that increasing the lateral size of the poly-Si grain reduces N_T. Moreover, NH_3 plasma passivation further reduces SS, because of the pileup of nitrogen at the SiO_2/poly-Si interface and the hydrogen passivation of the dangling bonds at the grain boundary. The amount of effects of NH_3 plasma passivation on PDMILC TFTs poly-Si grain boundaries can be evaluated from the grain boundary defects density (N_t).[15] Figure 7 plots extraction curves of N_t of M10 PDMILC TFTs, with and without NH_3 plasma passivation. Figure 8 plots N_t of PDMILC TFT *vs.* the multichannels with different widths, with and without NH_3 plasma passivation. The N_t decreases gradually from S1, M2, and M5 to the M10 PDMILC TFT with each channel width of the TFTs decreasing. Moreover, NH_3 plasma passivation substantially reduces N_t, providing high electrical performance. In addition, the M10 TFT has the lowest N_t (3.07×10^{12} cm^{-2}) and this value is consistent with its best performance.

Conclusion

Experimental results indicate that the performance of devices improves as each channel width decreases from the S1, M2, and M5 to the M10 PDMILC TFT. Moreover, the performance of devices further improves with NH_3 plasma passivation. The defect density (N_t) in the grain boundary reveals a strong consistency between theory and experimental results. Notably, M10 TFT has the best electrical performance. Because the M10 TFT has a split nanowire structure, which can greatly enhance poly-Si gain during the MILC process, and is exposed most effectively to an atmosphere of NH_3 plasma than other dimension TFTs. Both effects can reduce the number of defects at poly-Si grain boundaries in the active channel. In summary, we successfully demonstrate a practicable method to fabricate the high performance TFTs by structure modulation MILC process (PDMILC). Meanwhile, using NH_3 plasma passivation, the PDMILC TFTs can further improve the performance. These high performance NH_3 plasma passivation PDMILC TFTs are compatible with complementary metal-oxide-semiconductor technology, thus highly suitable for use in future SOP applications.

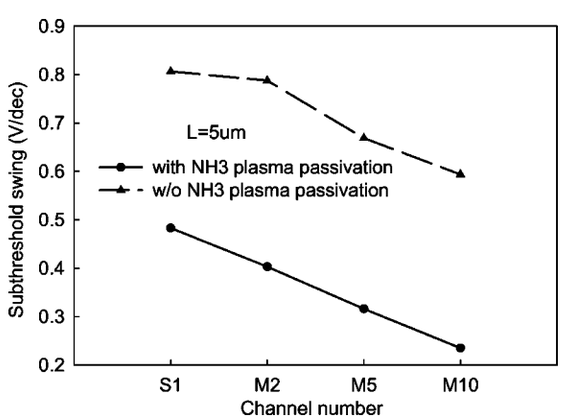

Figure 6. SS of PDMILC poly-Si TFTs *vs.* multichannels with different widths, with and without NH_3 plasma passivation.

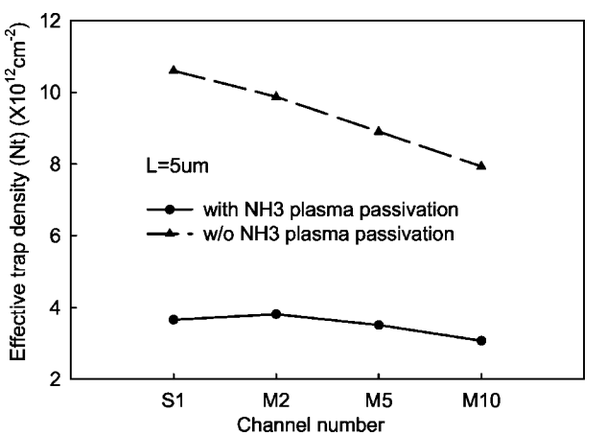

Figure 8. N_t of PDMILC poly-Si TFTs *vs.* multichannels with different widths, with and without NH_3 plasma passivation.

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