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Basic Characteristics of $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ Structure Using Layer-By-Layer Crystallization

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Layer-by-layer-crystallized $SrBi_2Ta_2O_9$ (SBT) films were deposited by metallorganic decomposition on a 14-nm-thick HfO_2 buffer layer. Experimental results indicate that the metal-ferroelectric-insulator-semiconductor (MFIS) stack with a layer-by-layer-crystallized SBT film exhibits ferroelectric hysteresis and a memory window of around 0.34 V at an operating voltage of 6.0 V. When postdeposition annealing was performed at 850°C, the layer-by-layer-crystallized MFIS structure exhibited favorable switching characteristics with negligible degradations of the memory window and capacitance retention time. The retention time of this structure exceeded 10^4 s and the extrapolated time was about 10^5 s.
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Recently, metal-ferroelectric-insulator-semiconductor (MFIS) structures have attracted much attention as promising candidates for field effect transistor (FET)-type ferroelectric nonvolatile memories (FeMFETs). FeMFETs provide many benefits, including smaller cells, simpler process flows, and the nondestructive readout operation feature. However, problems of interdiffusion between the ferroelectric layer and the silicon substrate may arise from a poor-quality interface layer, reducing the retention time, when the ferroelectric layer is directly deposited on the Si substrate.[1] To solve this problem, a good insulator layer that acts as a diffusion barrier must be found; it must have properties such as low leakage current and high dielectric constant. Insulating materials in the MFIS structure have been reported elsewhere; they include Si_3N_4, CeO_2, Ta_2O_5, ZrO_2, $LaAlO_3$, HfO_2, and Pr_2O_3.[2-9] However, a trapless ferroelectric layer and high-quality metal-ferroelectric interface are also required to ensure favorable retention characteristics.[10-13]

In this work, layer-by-layer-crystallized $SrBi_2Ta_2O_9$ ferroelectric films[14-16] were deposited by metallorganic decomposition (MOD) on a low-leakage HfO_2/Si substrate to fabricate an MFIS capacitor with a $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ structure. MFIS structures with conventionally crystallized $SrBi_2Ta_2O_9$ (SBT) films were used as control samples for comparison with layer-by-layer-crystallized and conventionally crystallized $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ structures. Layer-by-layer-crystallized and conventionally crystallized $Pt/SrBi_2Ta_2O_9/Pt/Ta/SiO_2/Si$ metal-ferroelectric-metal (MFM) capacitors were also fabricated and characterized. Retention characteristics of the MFIS structure can be improved by the layer-by-layer crystallization process. Additionally, the process promotes resistance to switching degradation at up to 10^9 cycles.

Experimental

MFIS capacitors with ferroelectric SBT and HfO_2 buffer layers were fabricated on 4-in. p-type (100) silicon wafers. The HfO_2 film was deposited by dc sputtering in Ar/O_2(24/3 sccm) ambient at room temperature using a 4-in. hafnium target. The deposited films were then annealed at 900°C for 3 min in oxygen atmosphere to yield a low-leakage HfO_2 film. The thickness of the annealed film was about 14 nm, as measured using a multiple-wavelength ellipsometer. The SBT films for the layer-by-layer-crystallized MFIS structures were prepared on the HfO_2/Si substrates by a layer-by-layer crystallization process. The wet films underwent a baking sequence at 120, 250, and 400°C each for 10 min in air. Then the deposited films were treated in an oxygen atmosphere at 750°C for 10 s by rapid thermal annealing (RTA). The heating rate was maintained at 10°C/s in the RTA process. For comparison, the conventionally crystallized MFIS structures that underwent the aforementioned baking sequence were adopted as control samples herein. After this process had been repeated four times to yield the desired film thickness of about 320 nm, all films were crystallized by postdeposition annealing (PDA) in an O_2 atmosphere at temperatures from 750 to 850°C for 3 min. Finally, 100-nm-thick Pt film was deposited by electron-beam evaporation through a shadow mask with an area of 3.5×10^{-4} cm^2 to serve as the top electrode.

The surface morphology and crystallinity of the $SBT/HfO_2/Si$ stack were analyzed by atomic force microscopy (AFM) and X-ray diffraction (XRD), respectively. The current density-electric field curves were measured using a Keithley 4200 semiconductor characterization system. The capacitance-voltage (C-V) characteristics and capacitance retention properties were evaluated using an HP4284A precision LCR meter at a frequency of 100 kHz. The program/erase endurance tests were performed by a system comprised of an HP8110A 150 MHz pulse generator, an HPE5250A low-leakage switch matrix, and an HP 4284A precision LCR meter. For MFM capacitors, the polarization-voltage characteristics were measured by a standardized ferroelectric test system RT66A.

Results and Discussion

Characteristics of Al/HfO_2/Si/Al MIS structure.—Normally, HfO_2 film crystallizes at high PDA temperatures, leading to high leakage current density. However, interfacial layers are form at such high temperatures of ~900°C, even when HfO_2 films are annealed in nitrogen ambient. When HfO_2 film is annealed in oxygen ambient, the thickness of interfacial layer increases, resulting in an increased equivalent oxide thickness (EOT) and lower leakage current. The leakage currents of the HfO_2 films annealed at various temperatures in the oxygen ambient (not shown) indicate that the leakage property can be improved as the annealing temperature increased, perhaps because of the increase of interfacial layer thickness. Additionally, the results concerning the frequency dependence of accumulation capacitance of those films (not shown) reveal that the capacitance of the HfO_2 films decreased with increasing annealing temperature, which is consistent with the results concerning the increase of the interfacial layer thickness. However, for the application of MFIS stack, formation of the interfacial layer is helpful to reduce the current through the I-S interface, resulting in an improvement of data retention.

Figure 1 shows the surface morphology of the HfO_2 films, including the as-deposited film and the film annealed at 900°C for 180 s in oxygen ambient. The roughness of the as-deposited film and the annealed film (PDA ≈ 900°C) were around 0.29 and 0.46 nm, respectively. From the surface morphology of the annealed film, it is difficult to judge the crystallinity of the film; therefore, XRD analysis of the HfO_2 films was also performed. The relevant results are shown in Fig. 2. As can be seen from the result of the annealed film (PDA ≈ 900°C), a weak signal concerning the crystallinity of HfO_2 film was found. The signal level is smaller and close to the value of background noise. From those results, we speculate that the HfO_2 film annealed at 900°C is partial crystallized.

Figure 3a presents the high-frequency C-V characteristics of the

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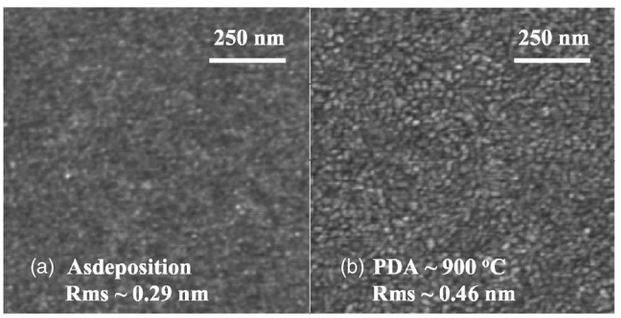

Figure 1. AFM images of HfO_2/Si structure: (a) as-deposited film and (b) the film annealed at PDA temperature of 900°C for 180 s in oxygen ambient.

Al/HfO_2/Si structure with 14-nm-thick HfO_2 film annealed at 900°C for 180 s in oxygen ambient, which has negligible trap-induced hysteresis and an EOT of about 6.5 nm, calculated from the accumulation capacitance. Additionally, Fig. 3b presents the current density-voltage (J-V) characteristics for the same MIS sample. The J-V curve reveals that the leakage current density was about 1.0×10^{-8} A/cm^2 at ±3 V. These small values may be conducive to increasing the capacitance retention time of the MFIS structure by reducing the current through the insulator-silicon interface.[10] The inset in Fig. 3b presents the frequency-dependence of the capacitance characteristics of the MIS structure. The data were measured at a dc voltage of −3 V with a small signal of 50 mV. The capacitance-frequency (C-F) curve exhibits negligible frequency dispersion. These electrical characteristics indicate that the HfO_2 film can serve as a buffer layer in the MFIS structure.

Crystallinity and surface morphology of $SrBi_2Ta_2O_9$/HfO_2/Si structure.—Figure 4 presents the XRD patterns of layer-by-layer-crystallized and conventionally crystallized Pt/SBT/HfO_2/Si structures. For the layer-by-layer-crystallized MFIS structure, the XRD spectra of the as-deposited SBT/HfO_2/Si structure included obvious

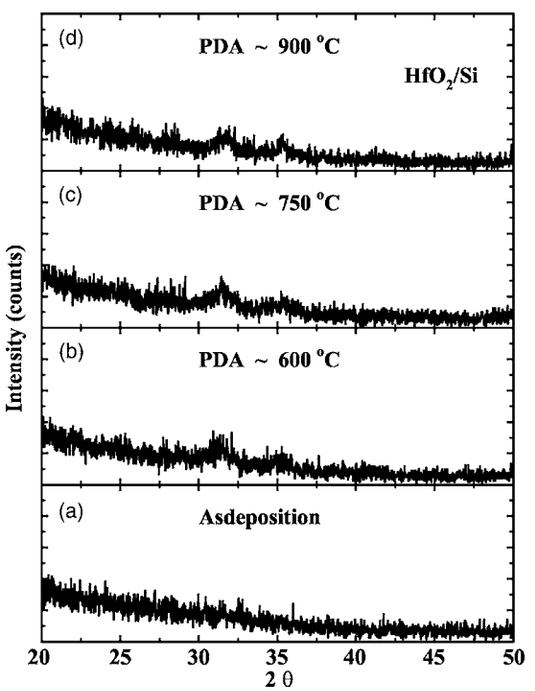

Figure 2. XRD patterns of HfO_2/Si structure with 14-nm-thick HfO_2 films as a function of the PDA temperature.

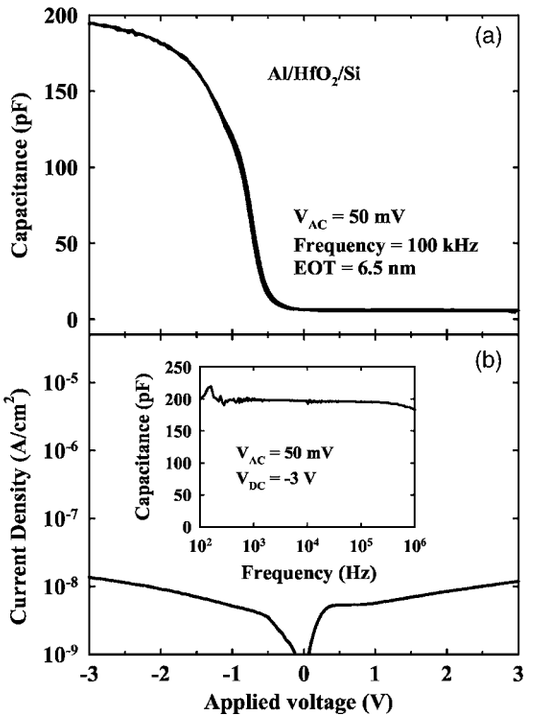

Figure 3. (a) C-V and (b) J-V characteristics of Al/HfO_2/Si capacitor. The inset shows the capacitance-frequency characteristic of this capacitor. The HfO_2 film was annealed at 900°C for 180 s in oxygen ambient.

(115) and (200) orientations. Additionally, the crystallinity of all the annealed SBT films improved when PDA was conducted in an O_2 atmosphere at temperatures of 750 and 850°C. These strong peaks associated with the predominant orientations in the XRD spectra verify that the SBT films with superior crystallinity can be obtained on top of the HfO_2 insulating layer.

Figure 5a-c presents the AFM surface morphology of layer-by-layer-crystallized SBT films on HfO_2/Si obtained at various PDA temperatures. As can be seen from Fig. 5a, a partially crystallized microstructure was exhibited in the as-deposited film of layer-by-layer-crystallized SBT/HfO_2/Si stack and the roughness was around 4.84 nm. When the PDA temperature increased, the improved crystallinity of the layer-by-layer-crystallized SBT/HfO_2/Si stack was found, resulting in the increase of both grain size and surface roughness. Besides, the same trend was also found in the conventionally crystallized SBT/HfO_2/Si stacks. The relevant results concerning the surface roughnesses of both stacks are also shown in Fig. 5d. The roughness of the layer-by-layer-crystallized SBT/HfO_2/Si structures exceeds that of the conventionally crystallized SBT/HfO_2/Si structures, and that of the layer-by-layer-crystallized MFIS structure saturated when the PDA temperature exceeded 750°C. However, the as-deposited film of conventionally crystallized SBT/HfO_2/Si stack exhibits an amorphous microstructure (not shown) with a roughness of around 0.72 nm. In contrast to the as-deposited film of conventionally crystallized MFIS stack, both a good crystallinity and a larger grain size present in the as-deposited film of the layer-by-layer-crystallized MFIS stack, which may lead to a larger roughness of layer-by-layer-crystallized MFIS stacks as PDA was performed.

Electrical properties of Pt/$SrBi_2Ta_2O_9$/Pt/Ta/SiO_2/Si MFM and Pt/$SrBi_2Ta_2O_9$/HfO_2/Si/Al MFIS structure.—Figure 6 plots the C-V characteristics of layer-by-layer-crystallized and conventionally crystallized Pt/SBT/HfO_2/Si structures. It was found that ferroelectric memory windows became narrow when the layer-by-layer-crystallized process was performed, a phenomenon similar to reported results for Pt/SBT/SiON/Si structure under high-temperature

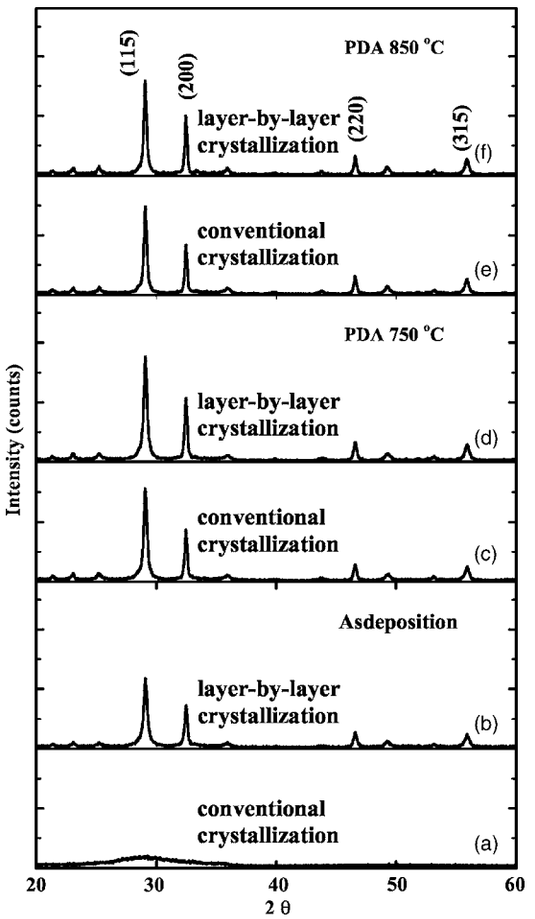

Figure 4. XRD patterns of SBT/HfO_2/Si structure with conventionally crystallized and layer-by-layer-crystallized SBT films as a function of PDA temperature.

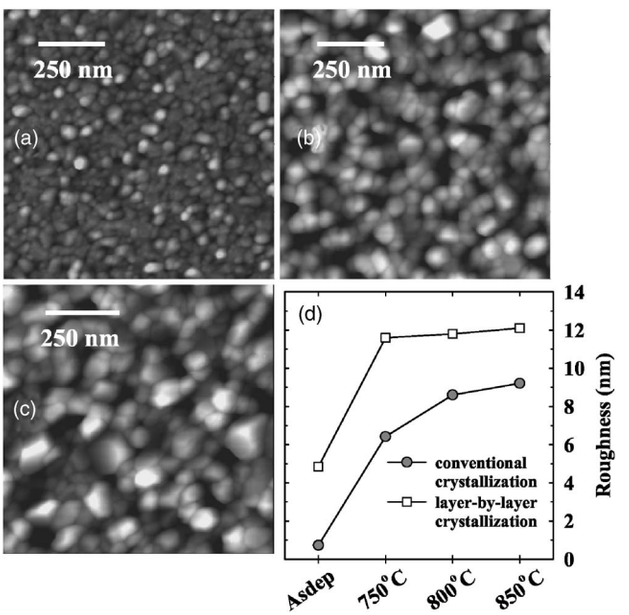

Figure 5. AFM images of layer-by-layer-crystallized SBT/HfO_2/Si structure: (a) as-deposited, (b) PDA temperature of 750°C, and (c) PDA temperature of 850°C. (d) Surface roughness of (●) conventionally crystallized and (□) layer-by-layer-crystallized SBT/HfO_2/Si structures as a function of PDA temperature.

RTA at 1000°C.[12] The memory windows of the layer-by-layer-crystallized and the conventionally crystallized MFIS structures were about 0.34 and 0.67 V at an operating voltage of ±6.0 V. Compared to the C-V curve of the conventionally crystallized MFIS structure annealed at 750°C, the results for the layer-by-layer-crystallized MFIS structure exhibited a negative voltage shift. The results for the conventionally crystallized MFIS structure obtained when high-temperature PDA was conducted at 850°C indicated similar behavior. These voltage shifts are probably caused by the reduction in the density of electron traps or ferroelectric oxide traps in the SBT/HfO_2/Si structure. The mechanism is complex and its details are presently being investigated.

Figure 7 plots the J-V characteristics of layer-by-layer-crystallized and conventionally crystallized MFIS structures. The J-V curves reveal that the leakage current density of the layer-by-layer-crystallized MFIS structure is on the order of 10^{-10}-3.0 $\times$ 10^{-9} A/cm^2 at an applied voltage of under 5.0 V. This leakage current density is lower than that of the conventionally crystallized MFIS structure. This lower leakage characteristic probably is caused by the suppression of current through the M-F interface or the improvement of the insulative property of the I-S junction.

To study further, the J-V characteristics of layer-by-layer-crystallized and conventionally crystallized Pt/SBT/Pt/Ta/SiO_2/Si MFM capacitors annealed in an atmosphere of O_2 at PDA temperature of 750°C were investigated and plotted in Fig. 8. Like the leakage properties of layer-by-layer-crystallized and conventionally crystallized MFIS structure, the layer-by-layer-crystallized MFM capacitor exhibits lower leakage than that of the conventionally crystallized MFM capacitor. However, this trend is different from the

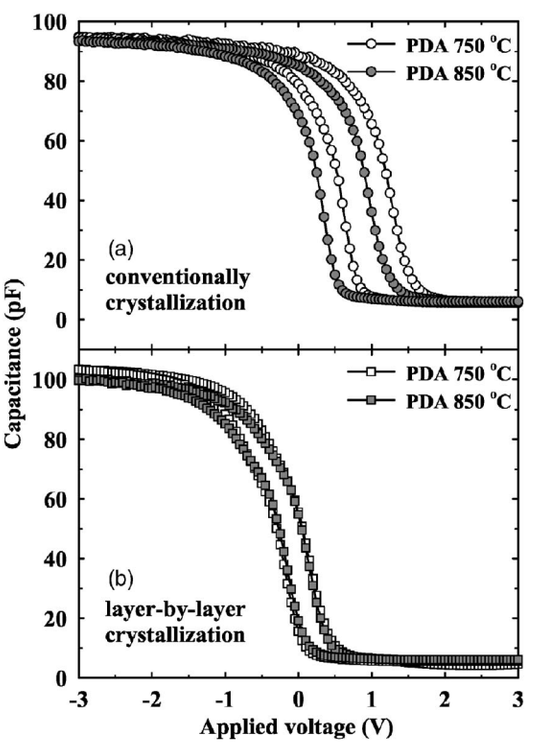

Figure 6. C-V characteristics of (a) conventionally crystallized (○, ●) and (b) layer-by-layer-crystallized (□, ■) Pt/SBT/HfO_2/Si structures. The open and full symbols represent the results of MFIS structure annealed at PDA temperatures of 750 and 850°C, respectively.

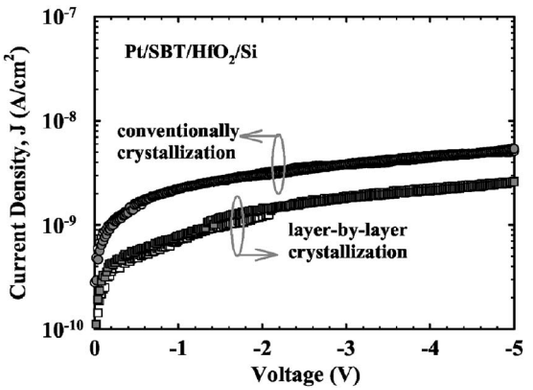

Figure 7. J-V characteristics of (○, ●) conventionally crystallized and (□, ■) layer-by-layer-crystallized Pt/SBT/HfO_2/Si structures. The open and full symbols represent the results of MFIS structure annealed at PDA temperatures of 750 and 850°C, respectively.

result of the surface roughness of MFIS stack (Fig. 5d). We speculate that layer-by-layer crystallization may result in a denser microstructure of SBT film and provide a more complete oxidation of the atoms (including Sr, Bi, and Ta). Therefore, by reducing the metallic ion in the bulk of the SBT film, the leakage current of SBT films may be suppressed.

To elucidate the conduction mechanism, Fig. 9a shows the ln(J/V)-$V^{1/2}$ and ln(J)-$V^{1/2}$ plots of the conventionally crystallized MFM capacitor. Both plots exhibit a positive gradient. From the slope of ln(J/V)-$V^{1/2}$ and ln(J)-$V^{1/2}$ plots, the optical dielectric constant of the conventionally crystallized SBT film can be determined. The optical dielectric constant obtained from the ln(J/V)-$V^{1/2}$ plot was estimated to be 15.26 and that obtained from the ln(J)-$V^{1/2}$ plot was around 1.19. However, the value obtained from the ln(J)-$V^{1/2}$ plot is too small and the order of this value is inconsistent with the reported result.[17] Therefore, we speculate that the dominant conduction mechanism of conventionally crystallized SBT film may be the Frenkel-Poole emission, and the optical dielectric constant of the conventionally crystallized SBT film was about 15.26. Additionally, the plots for layer-by-layer-crystallized MFM capacitors were also shown in Fig. 9b. As can be seen, the slope of the ln(J)-$V^{1/2}$ plot shows a positive value and the ln(J/V)-$V^{1/2}$ plot of layer-by-layer-crystallized SBT film exhibits a negative gradient. This indicates that the Schottky emission is the dominant conduction mechanism of the layer-by-layer-crystallized MFM capacitors.[18] The optical dielectric constant of the layer-by-layer-crystallized SBT film was about 11.50. These dielectric constants are close to the reported

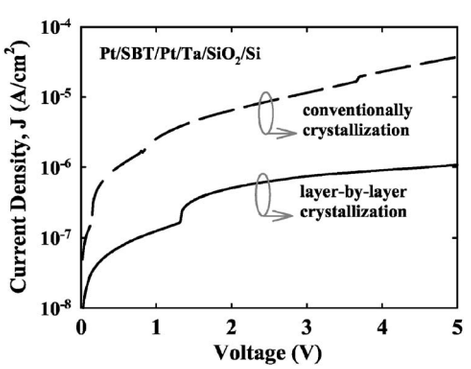

Figure 8. J-V characteristics of (- - -) conventionally crystallized and (—) layer-by-layer-crystallized Pt/SBT/Pt/Ta/SiO_2/Si MFM capacitors annealed at PDA temperature of 750°C.

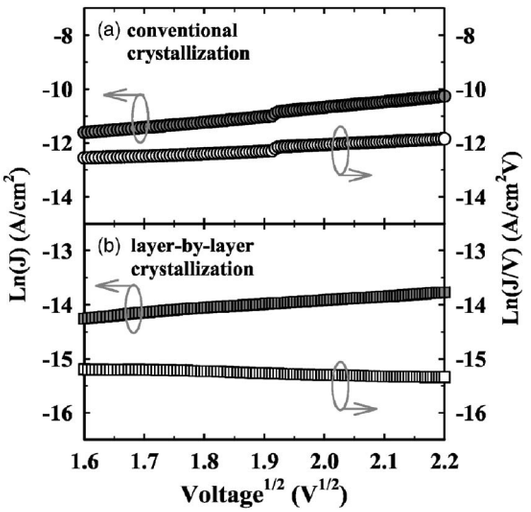

Figure 9. ln(J)-$V^{1/2}$ (full symbol) and ln(J/V)-$V^{1/2}$ (open symbol) plots of (a) conventionally crystallized (○, ●) and (b) layer-by-layer-crystallized (□, ■) Pt/SBT/Pt/Ta/SiO_2/Si MFM capacitors annealed at PDA temperature of 750°C.

values.[17] The above discussions imply that the layer-by-layer crystallization can effectively suppress the leakage current through the M-F interface and reduce the trap density of the SBT films. The retention time of MFIS structures is therefore longer because the currents through the M-F and I-S interface are suppressed.[10]

Figure 10 shows the capacitance retention characteristics of the layer-by-layer-crystallized Pt/SBT/HfO_2/Si structures. It was found that the layer-by-layer crystallization process can improve retention properties. The retention times of the layer-by-layer-crystallized MFIS structures exceeded 10^4 s when PDA was performed at temperatures between 750 and 850°C. This result reveals that the retention properties are improved probably because of the suppression of the leakage current of the MFIS structure and the reduction in the trap density of the SBT films.[10,13] This finding is also consistent with the results of the leakage properties of the MFM capacitors.

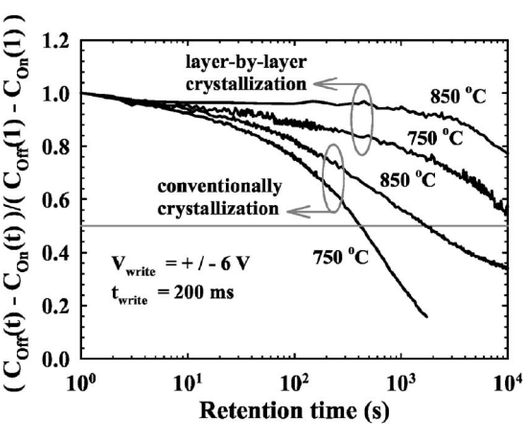

Figure 10. Capacitance retention characteristics of conventionally crystallized and layer-by-layer-crystallized Pt/SBT/HfO_2/Si structure annealed at PDA temperatures of 750 and 850°C. $C_{Off}(t)$ and $C_{On}(t)$ represent the time-dependent capacitance as negative and positive write pulses were applied, respectively. The retention properties were measured at 0.0 V for layer-by-layer-crystallized MFIS structures, and at 0.7 and 0.5 V for conventionally crystallized MFIS structures annealed at PDA temperatures of 750 and 850°C, respectively.

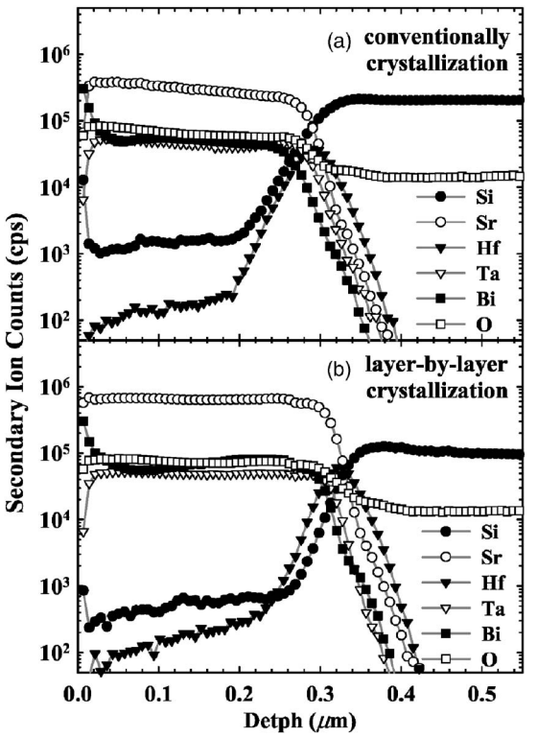

Figure 11. SIMS depth profiles of (a) conventionally crystallized and (b) layer-by-layer-crystallized SBT/HfO_2/Si stacks annealed at PDA temperature of 850°C.

Interdiffusion phenomena of the $SrBi_2Ta_2O_9$/HfO_2/Si stack.—Figure 11 shows the depth profile of a layer-by-layer-crystallized and a conventionally crystallized SBT/HfO_2/Si stack annealed at a PDA temperature of 850°C, obtained using secondary ion mass spectroscopy (SIMS). At such a high PDA temperature, the layer-by-layer-crystallized SBT/HfO_2/Si stack exhibits better interdiffusion resistance than that of the conventionally crystallized one. For the layer-by-layer-crystallized SBT/HfO_2/Si stack, the wet films first underwent a baking sequence in air and those were then treated in an oxygen atmosphere at 750°C for 10 s. Under this lower thermal budget, we speculate that the atoms (including Si, Hf, Sr, Bi, and Ta) may not diffuse seriously, because the depth profile of the conventionally crystallized SBT/HfO_2/Si stack (not shown) indicates that the stack also exhibits an adapted interdiffusion resistance as the PDA was performed at 750°C for 180 s. During the layer-by-layer crystallization process (annealing in oxygen ambient at 750°C for 10 s), the atoms (including Sr, Bi, Ta) are oxidized, leading to a crystalline phase of SBT film. Besides, the Si atom in both the back of the HfO_2 film and HfO_2/Si interface may be partially oxidized, which may suppress the diffusion of Si atom and result in an additional interfacial layer at HfO_2/Si interface. This may be a possible explanation for the improvement of interdiffusion resistance of the layer-by-layer-crystallized SBT/HfO_2/Si stack. However, the diffusion of silicon atoms into the SBT film may result in a certain amount of traps in the ferroelectric films, thereby degrading the leakage current and the capacitance retention characteristics for the MFIS stack. All these findings are consistent with the above discussion in Fig. 7 and 10.

Endurance characteristics of Pt/$SrBi_2Ta_2O_9$/HfO_2/Si/Al MFIS structures.—Figure 12 shows the endurance characteristics of the layer-by-layer-crystallized Pt/SBT/HfO_2/Si stack annealed at a PDA temperature of 850°C. A bipolar pulse train with an amplitude of 6 V and a pulse width of 2 μs was employed for testing the switching characteristics to study the endurance properties of this

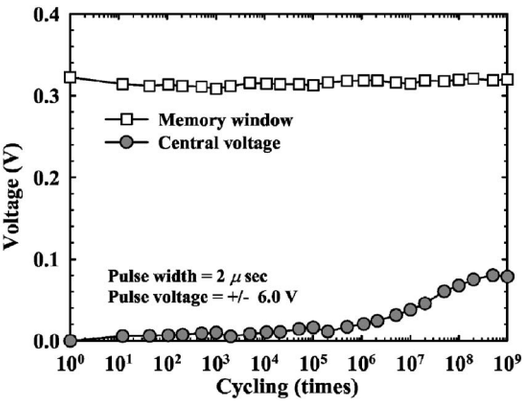

Figure 12. Memory window (□) and central voltage (●) as a function of switching cycles for layer-by-layer-crystallized Pt/SBT/HfO_2/Si structure annealed at PDA temperature of 850°C.

structure. The layer-by-layer-crystallized MFIS stack exhibits a favorable endurance characteristic with a negligible degradation of the memory window when the number of switching cycles exceeded 10^9. A positive shift in the central voltage was also found until the number of program/erase switching cycles exceeded 10^6. When the number of switching cycles was about 10^9, the shift of the central voltage of C-V curve was approximately 0.07 V, probably because election traps were generated during the switching stress. The C-V characteristics and capacitance retention characteristics of this layer-by-layer-crystallized Pt/SBT/HfO_2/Si structure before and after cycling are investigated to study further the degradation after stress, as shown in Fig. 13 and 14. It was found that up to 10^9 program/erase switching cycles negligibly degrade the retention properties. The retention time of this structure following stress exceeded 10^4 s, and the retention time extrapolated from the data was approximately 10^5 s.

Conclusion

A 320-nm-thick $SrBi_2Ta_2O_9$ film was prepared on Si(100) substrate using a 14-nm-thick HfO_2 buffer layer, which has low-leakage properties and a high dielectric constant. The C-V characteristics of the layer-by-layer-crystallized and the conventionally crystallized Pt/SBT/HfO_2/Si MFIS structures showed ferroelectric hysteresis. The memory windows of the layer-by-layer-crystallized and the conventionally crystallized MFIS structures were about 0.34 and 0.67 V

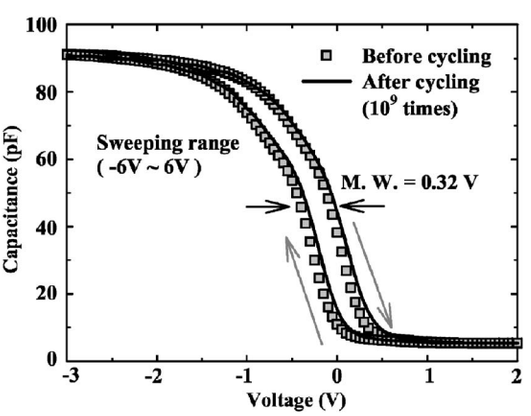

Figure 13. C-V characteristics (■) before and (—) after 10^9 switching cycles for layer-by-layer-crystallized Pt/SBT/HfO_2/Si structure annealed at PDA temperature of 850°C. The memory window of both curves was around 0.32 V.

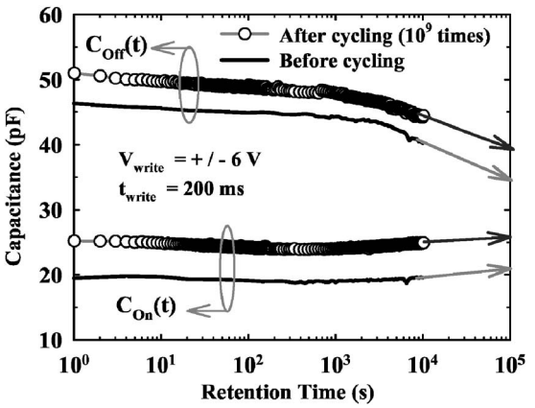

Figure 14. Capacitance retention characteristics (—) before and (○) after 10^9 switching cycles for layer-by-layer-crystallized Pt/SBT/HfO_2/Si structure annealed at PDA temperature of 850°C. The retention time exceeded 10^4 s and the extrapolated retention time was approximately 10^5 s.

at an operating voltage of ±6.0 V. The experimental results of MFM capacitors indicate that layer-by-layer crystallization can suppress the current through the metal-ferroelectric interface and reduce the trap density in the SBT films. Additionally, the MFIS structure with the layer-by-layer-crystallized SBT film exhibits favorable capacitance retention characteristics. When the PDA temperature was as high as 850°C, the retention time of the layer-by-layer-crystallized MFIS structure exceeded 10^4 s and the extrapolated retention time was approximately 10^5 s. Moreover, the structure exhibits good switching characteristics with negligible degradations of the memory window and retention time when the number of switching cycles was about 10^9.

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