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Reducing AC Power Consumption by Three-Dimensional Integration of Ge-On-Insulator CMOS on 1-Poly-6-Metal 0.18 μm Si MOSFETs

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We have used three-dimensional (3D) integration to reduce the ac power consumption in interconnects, which is the most severe issue beyond the dc power arising from the gate dielectric leakage current. From a direct calculation of the ac power consumption using an electromagnetic method, we show that both the ac power consumption and maximum operation frequency can be improved by integrating an additional integrated circuit layer. The 3D integration was realized by Ge-on-insulator (GOI) complementary metal oxide semiconductor field effect transistors (CMOSFETs) on 1-poly-6-metal (1P6M) 0.18 μm Si devices, where little performance degradation was measured in the lower layer 0.18 μm Si MOSFETs, due to the inherent low thermal budget (500°C rapid thermal anneal) of the GOI processing. The drive current of the 3D GOI n- and p-MOSFETs was more than double that of the control Si devices, providing another advantage of the approach.
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The relentless scaling down of transistor dimensions, leading to increasing circuit densities, results in the power consumption becoming the major limitation for integrated circuits (ICs). The gate leakage current in the ultrathin gate dielectric of individual transistors is the major source of the dc power consumption. However, by using high-κ oxynitride and metal oxides this issue can be addressed.[1-9] The ac power in the back-end interconnects ($CV^2f/2$) then becomes an important power consumption issue, particularly when both the operation frequency and interconnect density increases. For example, operation frequencies can be as high as 10.6 GHz (for ultrawide band access circuits) when using the high integration density and 9-metal interconnect layers available in the 90 nm technology node. Although this ac power consumption has been extensively discussed (e.g., panel session of *IEDM 2003*) no clear solution or approach is evident. Here, we suggest that three-dimensional (3D) integration can resolve this ac power consumption issue. Electromagnetic (EM) simulations, using IE3D software, suggest that both the ac power consumption and maximum operation frequency can be improved by integrating an additional IC layer. However, the key issue for 3D integration is how to create a high-performance upper layer on the complementary metal oxide semiconductor field effect transistors (CMOSFETs) without degrading lower-layer devices and interconnects.[10-12] This challenge also involves the high thermal budget [>1000°C rapid thermal anneal (RTA)] requirement for ion implant activation in the Si CMOSFETs, the low thermal budget required for the lower-layer shallow junction, silicide,[4] and the back-end interconnect stability. Here we demonstrate a new 3D solution using low thermal budget (500°C RTA) Ge-on-insulator (GOI) CMOSFETs. Little performance degradation was measured in lower-layer 0.18 μm 1-poly-Si-6-metal (1P6M) Si CMOSFETs.[13-15] In addition, the drive currents for 3D GOI n- and p-MOSFETs were more than double those of the Si control, due to higher electron and hole mobilities. The ac power consumption was reduced with little degradation of the lower-layer 0.18 μm MOSFETs. This, together with the improved current drive for the GOI CMOSFETs, should find application in future high-frequency, large-integration-density ICs.

Experimental

To calculate the ac power consumption in multiple layered interconnects, we used the 3D EM method reported previously[16-20] rather than analyzing the complicated parasitic circuits. The parasitic elements causing ac power consumption were treated using the 3D EM software, IE3D, which was calibrated through well-matched measured and modeled data for the radio frequency (rf) signal loss and power loss.[16-20] The reason for using the 3D EM simulator is to include the rf loss effect in low-resistivity (10 Ωcm) Si substrate.[16-20] An isolation thickness >100 μm into high-loss Si substrate is required to reduce the loss,[16-20] which makes the 3D calculation more accurate than the 2D case. The 3D GOI integration[5-7] was created using H^+ implantation of the Ge wafer, at a 5×10^{16} cm^{-2} dose and 200 keV energy, and depositing 100 nm PECVD SiO_2 on both the Ge and 1P6M 0.18 μm CMOS wafers, O_2 plasma-enhanced bonding, a "smart cut"[21,22] at 300°C, an extended 400°C annealing for 0.5 h, and slight polishing.[5-7,21-24] The p- and n-GOI MOSFETs were then formed using a high-κ$LaAlO_3$ gate dielectric deposited on the GOI,[21,22] followed by physical vapor deposited (PVD) IrO_2 and IrO_2/Hf dual metal gates,[5,6] self-aligned B^+ and P^+ ion implantation, and a 500°C RTA. A schematic diagram (Fig. 1a) shows the 3D integration and the features described above. As shown in Fig. 1b, the 3D integration can increase the circuit density and also reduce the interconnect distance by 1/2 by folding the 2D IC into 3D. For the multilevel parallel interconnect lines, the ac power is $Cv^2f/2$, $Li^2f/2$, and $i^2Rf/2$ for the parasitic C, L, and R circuits.

Results and Discussion

Figure 2a shows the equivalent circuit of the parasitic interconnect lines as a distributed circuit with 3D parasitic C, R, and L components. It is noticed that although the active MOSFETs consume ac power, the dominant dynamic power consumption is from the back-end interconnects.[25] The large parasitic effect in interconnect also dominates the circuit delay rather than the active MOSFETs. In addition, the ac power in MOSFETs can further be reduced by using the Si-on-insulator (SOI) wafer. Therefore, we focus the ac power consumption by back-end interconnect only. Because of the distributed nature of the circuit and the complicated parasitic effects, it is difficult to extract exact values for the parasitic R, L, and C components and to solve the ac power consumption correctly. Because circuit theory relies on Kirchhoff principles derived from the Maxwell's equations, we have calculated the ac power consumption directly using an EM wave approach. The EM software has the added capability of giving a 3D solution of the complicated structure depicted in Fig. 1a. Figure 2b shows the calculated *S* parameters of 1-mm-long parallel lines having a separation of 0.5 μm (close to the metal-to-metal separation of the 0.18 μm technology). The EM calculation is based on the interconnect struc-

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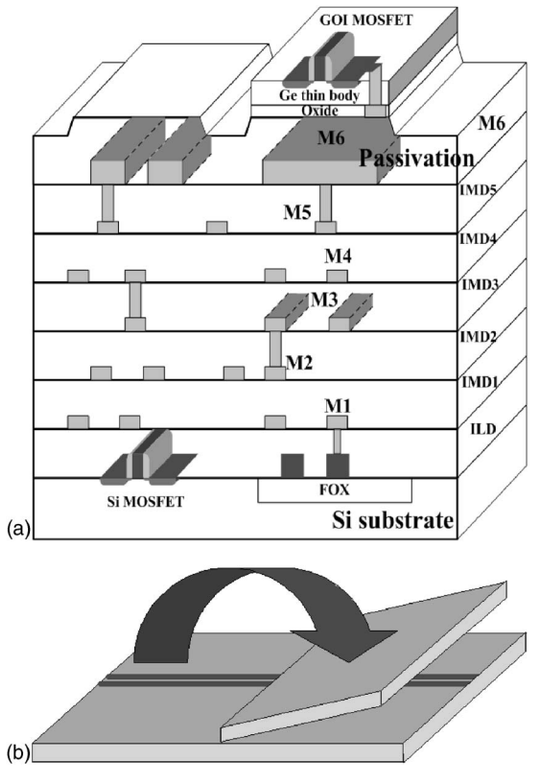

Figure 1. (a) Schematic of the 3D VLSI showing the lower-layer Si MOSFETs, multilevel (1P6M) parallel interconnect lines and top-layer GOI CMOS. Due to the thinness, the GOI devices can be connected to the bottom Si MOSFETs by VLSI back-end scheme. (b) The equivalent folding 2D IC to form the 3D IC. Both the integration density and interconnect distance can be improved by two or four times if folding once or twice.

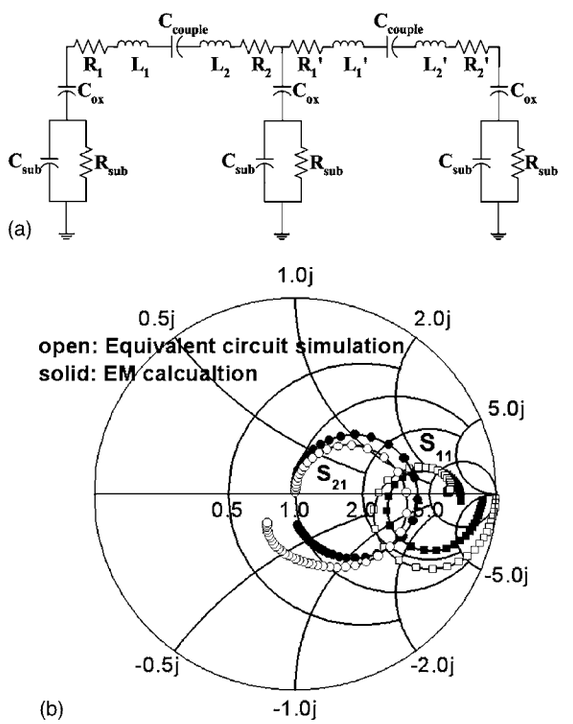

Figure 2. (a) The equivalent circuit of the interconnect lines of the 0.18 μm MOSFETs. (b) The simulated and IE3D EM calculated S_{21} and S_{11} for 1 mm long, 0.5 μm spaced, parallel lines.

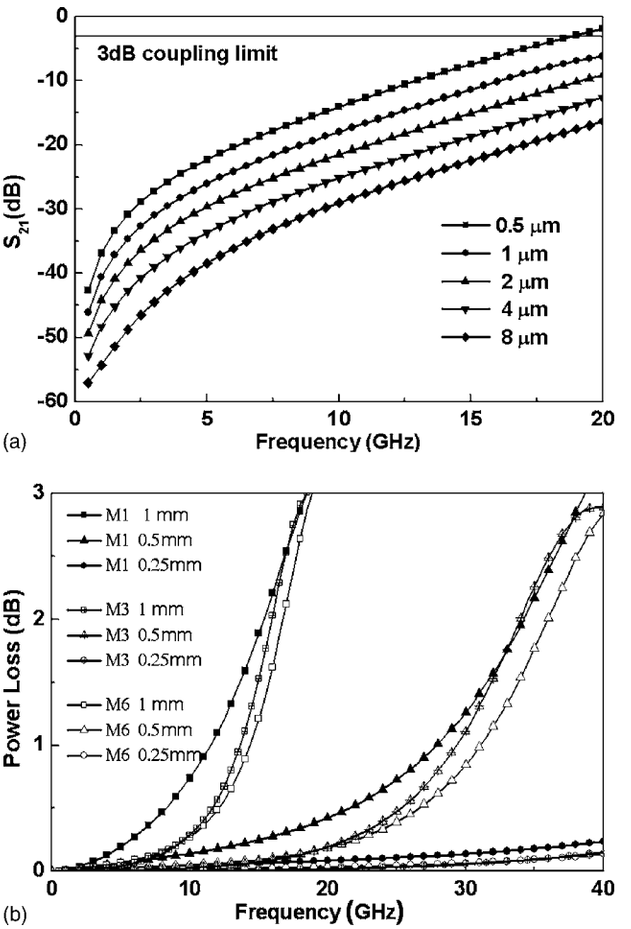

Figure 3. (a) Measured S_{21} coupling of two 1-mm-long parallel lines with various spacings from 0.5 to 8 μm using M6, and (b) calculated power loss of 0.5-μm-spaced, parallel lines of different lengths. The 3D integration can reduce the distance to half and 1/4 using single-layer GOI and double-layer GOI, respectively, above the bottom Si MOSFETs.

ture in Fig. 1a, where the thicknesses of back-end interconnect for field-oxide (FOX), interlayer dielectric (ILD), and Intermetal dielectric (IMD, from IMD1 to IMD5) are 0.35, 0.7, and 1.4 μm, respectively. The metal thickness for respective M1-M5 and M6 are 0.5 and 1.0 μm. The equivalent circuit simulation is also shown for comparison. The reasonably good match between the EM calculation and the equivalent circuit simulation justifies using the EM method to calculate the ac power consumption of the 3D parallel lines. The slight mismatch between is most probably due to the distributed nature of parallel lines. This is difficult to simulate using a simple lumped-circuit model. The ac power consumption can be calculated by $1 - |S_{21}|^2 - |S_{11}|^2$ rather than solving the complicated circuit, and adding the power consumption of $Cv^2f/2$, $Li^2f/2$, and $i^2Rf/2$ in each parasitic C, L, and R.

The signal coupling loss is severe for parallel lines at high frequency. Figure 3a shows the measured S_{21} signal coupling loss of 1-mm-long parallel lines, with various spacings from 0.5 to 8 μm using M6. The maximum allowed 3 dB coupling (50% signal loss to the second line) limits the highest IC operation frequency using high-density parallel lines. The operation frequency increases with increasing line separation and thus limits the interconnect line separation and density. For the 1 mm long line with a 0.5 μm separation, a maximum operating frequency of <20 GHz was obtained, according to the technology data provided by the foundry. From this result, further reducing the interconnect metal distance in the

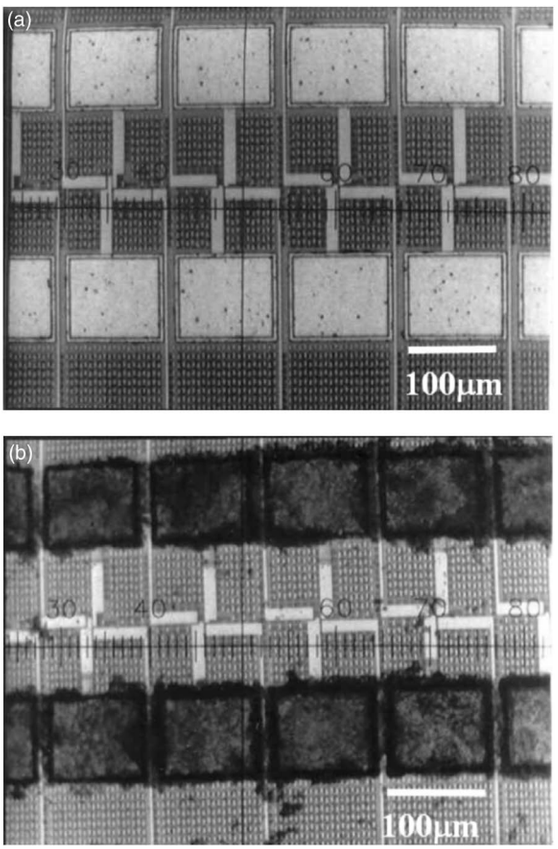

Figure 4. Images of 0.18 μm MOSFETs with probing pads (M6 and 2 μm thickness) (a) before and (b) after the GOI bonding. The "dark" area on the pad after bonding is due to the selectively bonded Ge by "smart cut".

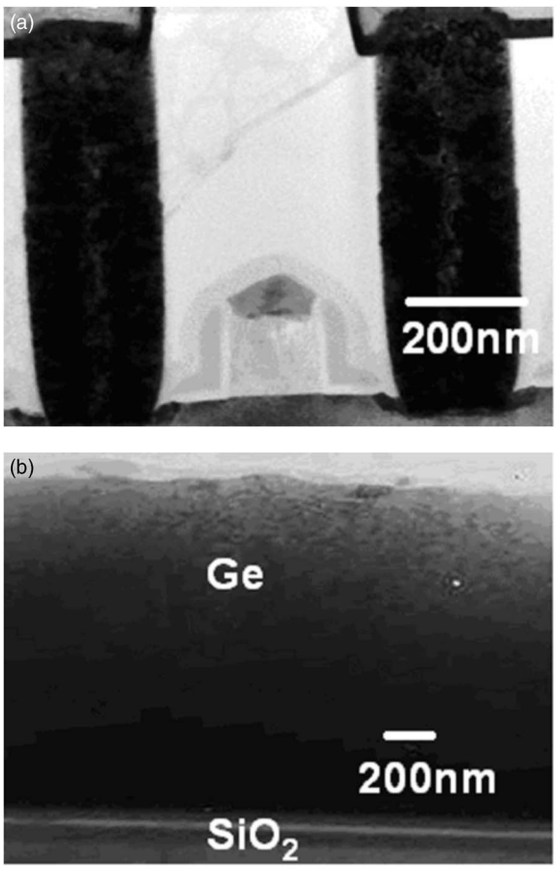

Figure 5. Cross-sectional TEMs of (a) the lower 0.18 μm MOSFET and (b) the selectively bonded and smart-cut GOI on a pad. The Ge/SiO_2 interface appears to be dislocation-free and smooth.

90 nm node is not useful for high-frequency circuits. The power loss of the 1-mm-long, 0.5 – μm-spaced parallel lines is also shown in Fig. 3b. The power loss is more severe than the coupling loss of parallel lines shown in Fig. 3a. For 1-mm-long parallel lines with the 0.5-μm gap, the maximum frequency allowed for 3 dB ac power consumption is 20 GHz and can be increased to 40 GHz if two layers are used in the 3D integration. A much larger improvement can be achieved using three layers (two layers in GOI plus a single one from the Si CMOSFETs). This reduces the ac power consumption to ⩽0.25 dB at 40 GHz, because it is related to parasitic effects as well as being nonlinear with the line length.

The results above indicate that the 3D integration is effective in reducing the ac power consumption. However, the main challenge is how to realize such 3D integration with little performance degradation of the Si devices in the lower layer. Figure 4a and b shows a plan-view image of the 1P6M 0.18 μm MOSFETs before and after the 3D GOI formation, respectively, where the GOI was formed on the 0.18 μm Si devices by using the "smart-cut" techniques[21,22] described above. The dark area on the pad after bonding is due to the selectively bonded Ge. This was confirmed by surface profile measurements. This is related to the top M6 (2 μm thick) without planarization, where the Ge bonding can only be attached to these higher M6 metal pads. A Ge thickness of 1.6 μm was measured from the surface profile and is consistent with previous H^+ implantation and smart-cut GOI.[21,22] Although void-free bonding was achieved previously[6,7] and selective bonding was formed in this work, further large-size void and defect-free bonding need to be demonstrated. However, such large-scale bonding has been used for 12-in. SOI wafer manufacture, which may not cause the problem for large-size GOI bonding on Si IC.

Figure 5a and b shows cross-sectional transmission electron microscopy (TEM) views of the bottom 1P6M 0.18 μm Si MOSFETs and the top GOI, respectively. After the 500°C RTA thermal cycle for GOI CMOSFET fabrication, no observable degradation can be seen in the cross-sectional TEM of the lower layer 0.18 μm Si

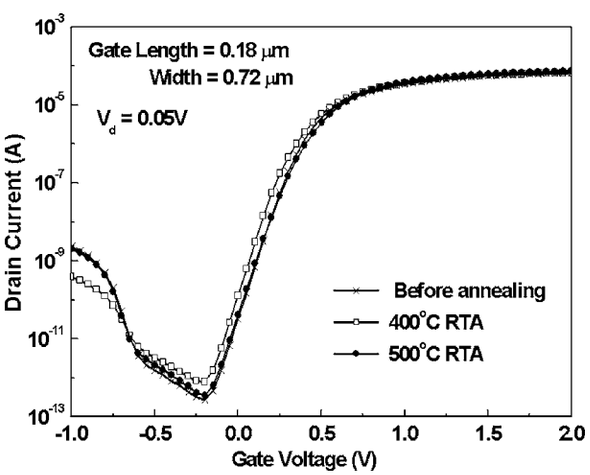

Figure 6. The I_d-V_g characteristics of the 0.18 μm MOSFETs, which, after the bonding process, are beneath the 3D GOI. Little drain current degradation occurred after the thermal processing cycle.

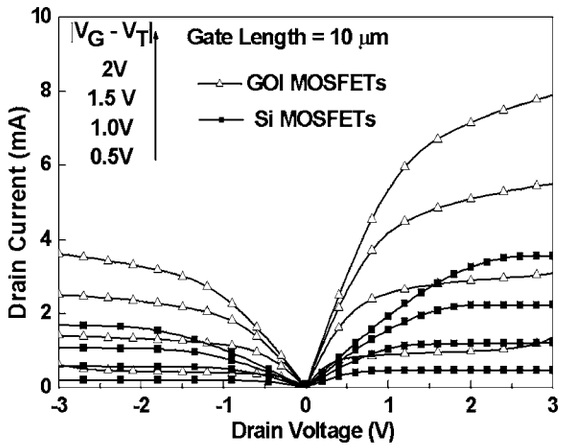

Figure 7. The I_d-V_d characteristics, at various V_g-V_t values, for $IrO_2/LaAlO_3$ p-MOSFETs and IrO/Hf/LaAlO3 n-MOSFETs from the top-layer GOI and the control 2D Si. An EOT of 1.4 nm was determined for both the GOI and Si devices from cyclic voltammetric measurements.

MOSFETs. This is due to the low RTA process temperature of 500°C for the GOI CMOSFETs. The cross-sectional TEM shows a dislocation-free, smooth Ge/SiO_2 interface, similar to our previous GOI results.[5-7] The top Ge layer thickness of 1.6 μm is the same as that measured from the surface profile.

We measured the characteristics for the lower layer 1P6M 0.18 μm Si MOSFETs, before and after the thermal cycle for 3D GOI fabrication, to determine if there was any degradation. Figure 6 shows the I_d-V_g characteristics of the bottom layer 0.18 μm Si MOSFETs, where a comparable subthreshold swing and off-state current were measured. Little degradation was observed even after the 500°C RTA required for activating the source and drain ion implantation of the top GOI CMOSFETs.

Figure 7 displays the I_d-V_d characteristics, for a family of V_g-V_t values, for the top-layer $IrO_2/LaAlO_3$ p-MOSFETs and $IrO_2/Hf/LaAlO_3$ n-MOSFETs on GOI. For comparison, data for similar dual-metal-gates/high-κ CMOSFETs[5,6,21-24] on Si are also plotted. These devices were processed at a higher 950°C RTA, because of the higher ion implant annealing required for the Si MOSFETs. Good transistor characteristics were observed for both p- and n- devices. The drive currents are 2.1 and 2.2 times higher for the metal-gated/high-κ n- and p-MOSFETs on GOI than for the Si devices. This is an advantage of the GOI devices and is consistent with previous reports.[5-7] Such improvement is due to the smaller effective mass of Ge than Si. Similar better device performance is also obtained in small effective mass III-V FETs than Si MOSFETs, which also gives better high-frequency performance at rf regime.[26] Therefore, the smaller effective mass is the key factor for both dc drive current and rf performance improvements.[26] A further advantage of the 3D integration would be the high circuit density and also that a 3D memory with a record high density can be realized by 3D integration.[12] Although there are other approaches to realize the 3D integration, such as using chip-stacking from a packaging approach,[27] unique advantages of this work are the approximately two times higher drive current and potential high interconnect density using wafer-level process technology. The higher circuit density and better device drive current are equivalent to scaling down the very large scale integrated (VLSI) technology, which may provide another useful approach when quantum-mechanical scaling limits occur. Further challenge of this approach is the formation of ultrathin body Ge at the limited thermal budget, which is also useful to reduce the junction leakage of GOI CMOSFETs. The large leakage current is the biggest challenge of small-energy-bandgap materials such as Ge and InGaAs,[26] although they also give high mobility and transistor drive current.

Conclusion

From our EM calculations, calibrated by well-matched simulation and experimental data, we have shown that the ac power consumption in a circuit can be significantly reduced using 3D integration. The 3D integration was realized by low-temperature GOI process technology, which produced little degradation of the lower-level Si 0.18 μm devices. The self-aligned process is fully compatible with current VLSI technology. The 2.1-2.2 times higher current drive capability of the GOI CMOSFETs are another desirable feature of this approach.

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