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CF_4 Plasma Treatment for Fabricating High-Performance and Reliable Solid-Phase-Crystallized Poly-Si TFTs

Shen-De Wang,[z] Wei-Hsiang Lo, and Tan-Fu Lei

Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan

A CF_4 plasma treatment on solid-phase-crystallized (SPC) poly-Si thin-film transistors (TFTs) has been demonstrated. Using this technique, fluorine atoms can be introduced into the poly-Si film to passivate the defects, and hence, the device performance of the SPC poly-Si TFTs can be significantly improved. The fluorinated SPC poly-Si TFTs exhibit a good subthreshold slope, low threshold voltage, and high field effect mobility. Moreover, the fluorinated SPC poly-Si TFTs also exhibit an improved hot-carrier-stress immunity, which is due to the strong Si-F bonds formed in the poly-Si channel region.
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Polycrystalline silicon thin-film transistors (Poly-Si TFTs) have attracted much attention due to the possibility to realize the integration of switching pixels and their peripheral driver circuits on a single glass substrate of active matrix liquid crystal displays (AMLCDs).[1-3] Compared with conventional amorphous-Si TFTs, poly-Si TFTs have many advantages including higher driving current and greater carrier mobility. However, the trap states in the poly-Si grains and grain boundaries degrade the carrier's transport and increase the off-stated leakage current.[4-6] To eliminate these trap states becomes the main topic for future production of high-performance poly-Si TFTs. Hydrogen-based plasma passivation is the most popular method utilized in the current production.[7-9] Although hydrogenation can passivate the intragrain and grain boundary trap states in the poly-Si film, the hydrogenated poly-Si TFTs suffer from a serious reliability issue, which is attributed to the weak Si-H bonding. Recently, several studies have demonstrated the use of fluorine (F) atoms to fluorinate poly-Si films, which can improve performance and reliability of poly-Si TFTs, particularly under long-term electrical stress.[10-15] This is because fluorine atoms can terminate dangling bonds and replace weak bonds in the grain boundaries and SiO_2/poly-Si interface, and thus reduce the trap states in the poly-Si channel. In addition, strong Si-F bonds, more stable than Si-H bonds, can greatly improve device reliability under long-term electrical stress.

Fluorine ion implantation (FII), the most adoptive fluorinating technique, has been investigated.[10-13] It is worth pointing out that the ion implantation method is no longer suitable for large-sized glass substrate application. Moreover, to activate the fluorine atoms and recover the defects created by FII, a subsequent high-temperature annealing is required. However, the high-temperature process is not compatible with current production. Kim et al. demonstrated the use of fluorinated oxide (SiO_xF_y) to replace FII, which can serve as a diffusion source.[14,15] This technique increases manufacturing processes because extra film deposition and etching processes are necessary. To date, although the effects of fluorination have been investigated and clarified, there is still a lack of a process-compatible technique to introduce fluorine atoms effectively into poly-Si films for the poly-Si TFT fabrication. In this work, we proposed a novel fluorinating technique by employing CF_4 plasma treatment, which is a simple and efficient process. To avoid an unwanted etching effect, we controlled the radio frequency (rf) to apply a low power (5 W) to dissociate fluorine atoms, which were used to fluorinate the poly-Si film. The fluorinated poly-Si TFTs have been fabricated using this technique and their device characteristics and reliability have been investigated.

Experimental

The schematic diagram of the fabrication process is illustrated in Fig. 1. First, a 100-nm-thick amorphous silicon layer was deposited on a thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 h in N_2 ambient for the phase transformation from amorphous to polycrystalline silicon. Individual active regions were then patterned and defined. After standard RCA cleaning, samples were subjected to the CF_4 plasma treatment conducted in a plasma-enhanced chemical vapor deposition (PECVD) system at 350°C for 15 s, under a pressure of 200 mTorr and a power of 5 W. A 50-nm-thick tetraethyl orthosilicate (TEOS) oxide was deposited to serve as the gate insulator and a 200-nm-thick poly-Si film was deposited and patterned for the gate electrode. A self-aligned phosphorous ion implantation was preformed with the dosage and energy of 5×10^{15} cm^{-2} and 40 keV, respectively. The dopant activation was performed at 600°C furnace annealing at N_2 ambient for 24 h, followed by a deposition of the passivation layer and a definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. The control samples were prepared without the fluorinating process. To concentrate on revealing the fluorine passivation effects of the CF_4 plasma treatment, none of the additional hydrogenation process was performed on the control samples. The electrical and reliability characteristics were performed using an HP 4156B.

Results and Discussion

Figure 2 shows the transfer characteristics ($I_D - V_{GS}$) for the control and fluorinated poly-Si TFTs. The measurements were performed at two different drain voltages of $V_{DS} = 0.1$ and 5 V. The parameters of the devices, including the threshold voltage (V_{th}) and subthreshold swing (S.S.), maximum on-current (I_{on}) and the minimum off-current (I_{off}), were measured at $V_{DS} = 5$ V. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100$ nA. The extracted device parameters are listed in Table I.

Accordingly, the performance of the fluorinated poly-Si TFT is significantly improved. The threshold voltage and subthreshold swing of the fluorinated poly-Si TFT were found to be 8.3 and 1.73 V/dec, which are superior to that of the control one (12 and 2.06 V/dec, respectively). It is known that V_{th} and S.S. are strongly influenced by the deep trap states, associated with the dangling bonds, which have energy states near the middle of the silicon bandgap. Therefore, using CF_4 plasma treatment can effectively terminate the dangling bonds in the poly-Si and SiO_2/poly-Si interface. In addition, the maximum on-current (I_{on}) and on/off current ratio of the fluorinated TFT are also better than that of the control TFT.

The minimum off-current (I_{off}) of the fluorinated device was nearly unsuppressed, which is consistent with the previous reports by Chern et al.[11] and Kim et al.[15] However, while the applied gate voltage was toward more negative ($V_{GS} < -2$ V), the fluorinated poly-Si TFT showed a smaller leakage current compared with that of the control TFT. As is well known, under a high electric field, the

[z] E-mail: bryant519.ee90g@nctu.edu.tw

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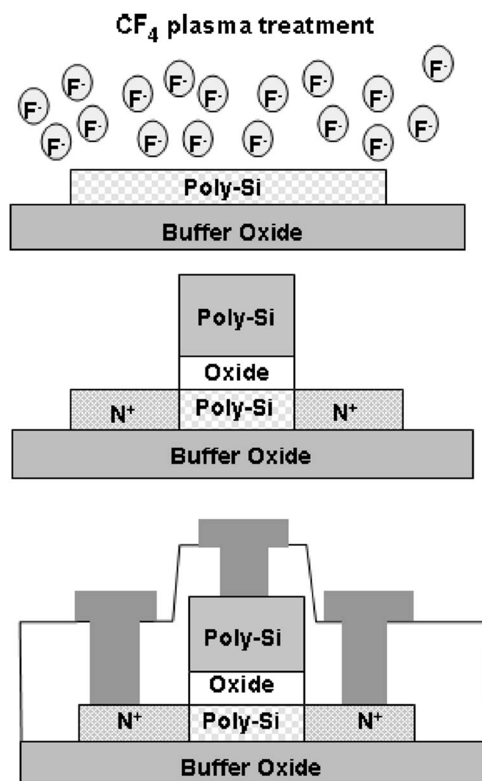

Figure 1. Schematic diagram of the poly-Si TFTs by using CF_4 plasma treatment.

leakage current in the poly-Si TFT mainly comes from the trap-assisted band-to-band tunneling near the drain edge. This observation suggests that there must be fewer trap states for the fluorinated poly-Si TFT, and thus the leakage current under a high electric field is reduced.

Figure 2 also shows field effect mobility vs the gate voltage of control and fluorinated poly-Si TFTs. The field effect mobility was calculated from the value of transconductance at $V_{DS} = 0.1$ V. As is seen, the maximum field effect mobility of the fluorinated poly-Si TFT is higher than that of the control TFT. The fluorinated poly-Si TFT shows approximately 28% enhancement in the maximum field

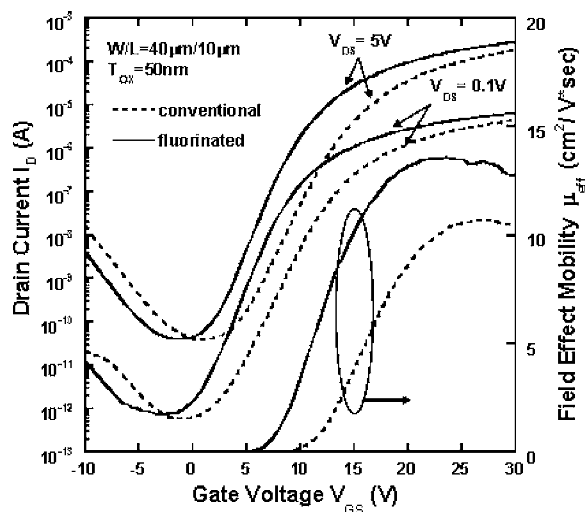

Figure 2. Transfer characteristics of the control and fluorinated poly-Si TFTs with $V_{DS} = 0.1$ and 5 V.

Table I. Comparison of device characteristics of the control and fluorinated poly-Si TFTs.

Device parameters	Conventional	Fluorinated
Threshold voltage Vth (V)	12	8.3
Subthreshold swing S.S. (V/dec)	2.06	1.73
Maximum on-current I_{on} (μA)	180	279
Minimum off-current I_{off} (pA)	38.7	40.7
On/off current ratio I_{on}/I_{off} (*10^6)	4.65	6.85

effect mobility. Note that the field effect mobility is significantly affected by the tail states near the bandedge, which resulted from the strain bonds in poly-Si and SiO_2/poly-Si interface.[4] This feature implies that the CF_4 plasma treatment cannot only terminate the dangling bonds, but also relieve the strain bonds. Based on these results, a schematic cross-sectional view of the SiO_2/poly-Si interface is illustrated in Fig. 3. It is suggested that strong Si-F bonds replace the dangling and strain bonds for the fluorinated poly-Si films, and thus the performance of the device is greatly improved.

The grain boundary trap state densities (Q_T) of the conventional and fluorinated poly-Si TFTs were estimated by the Levison and Proano method.[16,17] Figure 4 exhibits the $\ln[I_D/(V_{GS} - V_{FB})]$ vs $1/(V_{GS} - V_{FB})^2$ curves at low V_{DS} and high V_{GS}. Q_T was extracted from the slopes of these curves. Fluorinated poly-Si TFT exhibits a Q_T of 1.32×10^{13} cm^{-2}, whereas the control TFT has 1.67×10^{13} cm^{-2}. This result implies that the CF_4 plasma treatment can passivate the grain boundary trap states in the poly-Si film. To further study the fluorine passivation effect near the interface, the effective interface trap states densities (N_t) near the SiO_2/poly-Si interface were also calculated. From the S.S., by neglecting the depletion capacitance, N_t can be expressed as[18]

$$N_t = [(\text{S..S./ln } 10)(q/kT) - 1](C_{ox}/q) \quad [1]$$

where C_{ox} is the capacitance of the gate oxide. The N_t values of the control TFT and the fluorinated TFT are 1.45 and 1.21×10^{13} cm^{-2}, respectively. The N_t values reflect trap states near the SiO_2/poly-Si interface. Therefore, these results figure that trap states in both grain boundaries and the SiO_2/poly-Si interface were reduced by using CF_4 plasma treatment, which results in great improvement in device performance.

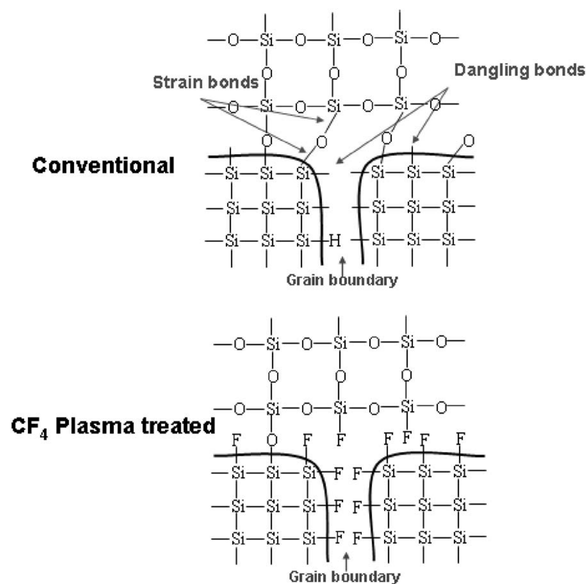

Figure 3. Schematic cross-sectional view of SiO_2/poly-Si interface with and without CF_4 plasma treatment.

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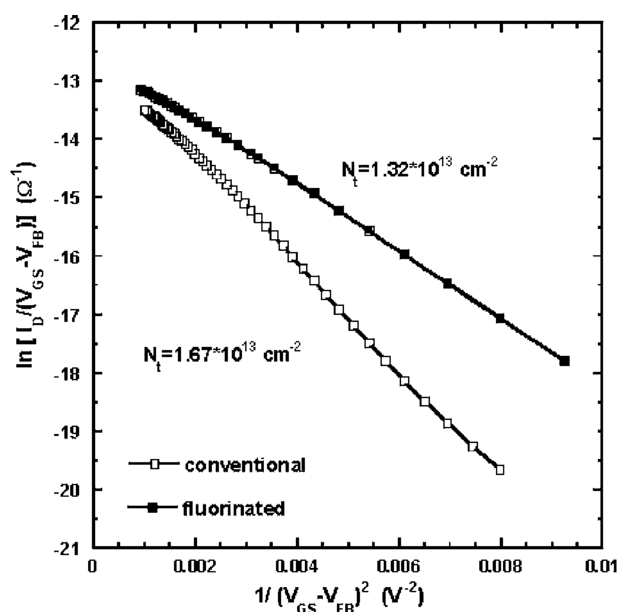

Figure 4. $\ln[I_D/(V_{GS} - V_{FB})]$ vs $1/(V_{GS} - V_{FB})^2$ curves at $V_{DS} = 0.1$ V and high V_{GS} for control and fluorinated poly-Si TFTs.

Figure 5 shows the output characteristics ($I_D - V_{DS}$) of the fluorinated and control poly-Si TFTs. As is seen, the driving current increases significantly for the fluorinated poly-Si TFT. This is due to the higher mobility and smaller threshold voltage of the fluorinated poly-Si TFT compared with the control TFT. The driving current increased 130, 84, and 55% at $V_{DS} = 20$ V with $V_{GS} = 10$, 15, and 25 V, respectively. Figure 6 shows the secondary ion mass spectroscopy (SIMS) profiles of the control and fluorinated poly-Si films. The SIMS profiles show that lots of fluorine atoms could be introduced into the poly-Si layer by using CF_4 plasma treatment, but not carbon atoms. The SIMS analysis also shows a notably high concentration of fluorine atoms piling up near the SiO_2/poly-Si interface, instead of in the deep poly-Si layer. These piled-up fluorine atoms can provide a more effective passivation of trap states, because the quality of the SiO_2/poly-Si interface is the main issue for carrier transport.

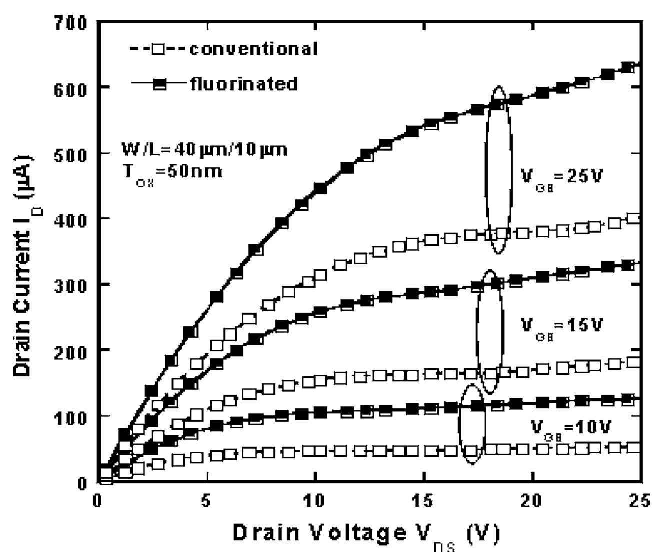

Figure 5. Output characteristics of the control and fluorinated poly-Si TFTs with $V_{GS} = 10$, 15, and 25 V.

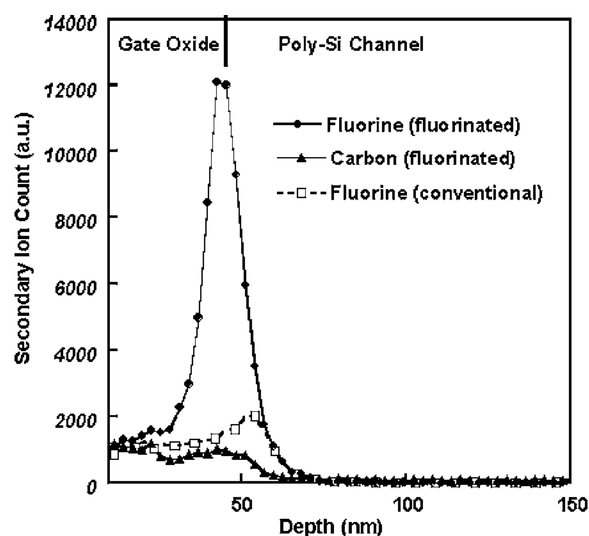

Figure 6. SIMS analyses of the control and fluorinated poly-Si films.

Figure 7 exhibits activation energy (E_a) vs gate voltage for the control and fluorinated poly-Si TFTs at $V_{DS} = 1$ V. In the off-region (low V_{GS}), the value of E_a reflects the required energy for carriers to leak by means of trap states, whereas in the on-region (high V_{GS}), the value of E_a reflects the carrier transport barrier caused by the trap states within the poly-Si channel.[19] Compared with the control TFT, the extracted E_a of the fluorinated poly-Si TFT decreases in the on-region and increases in the off-region. That is to say, for fluorinated poly-Si TFT, fluorine atoms can passivate the trap states and hence reduce the barrier height for the carrier's transport when the device is turned on. Fewer trap states resulted in the increase of E_a in the off-region and thus, trap-assisted leakage current is suppressed after the fluorinating process. Moreover, in the subthreshold region, a steeper profile can be found for the fluorinated TFT, which proves that the interface quality of the fluorinated TFT was better than that of the control TFT.

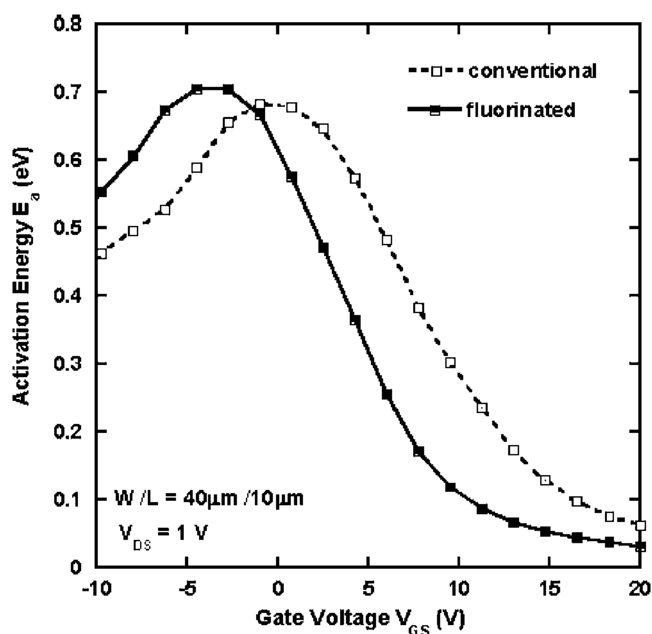

Figure 7. Activation energy vs gate voltage of the control and fluorinated poly-Si TFTs.

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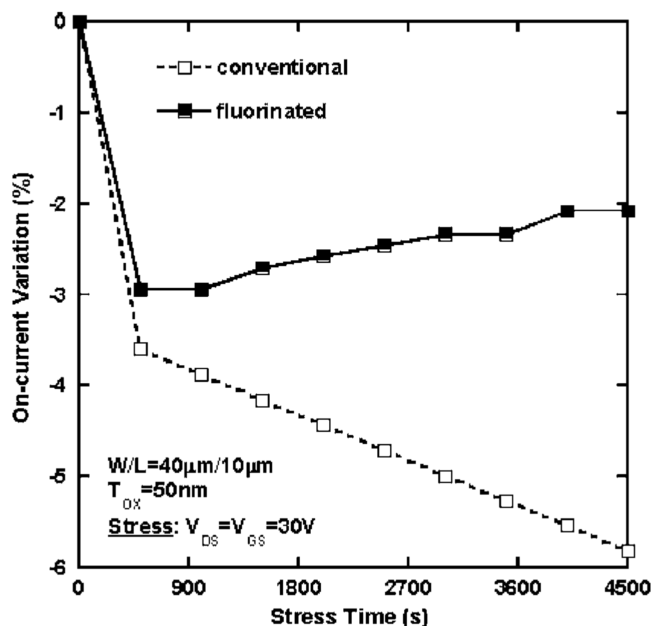

Figure 8. On-current variation as a function of stress time under a hot-carrier stress of the control and fluorinated poly-Si TFTs.

Additionally, the hot carrier stress was carried out to examine the reliability of the device. Figure 8 shows the variation of on-current under a hot carrier stress. The stress conditions were performed at $V_{DS} = 30$ V and $V_{GS} = 30$ V for 4500 s. The variation of on-current was defined as $(I_{on,stressed} - I_{on,initial})/I_{on,initial} \times 100\%$, where the $I_{on,initial}$ and $I_{on,stressed}$ are the measured I_{on} prior to and after the electrical stress. The on-current degradation can be attributed to two mechanisms: oxide trap charges and the creation of trap states in the poly-Si. They can be attributed to channel-hot-electron (CHE) and self-heating (SH) phenomenon. For CHE, electrons were injected and trapped in the gate oxide; then, the carrier flow is disturbed, reducing the ion. The SH-induced damage is due to the large Joule heat, resulting from a high drain current.[20,21] Because TFTs are fabricated on a poor thermal-conducting substrate, devices reach a very high temperature during operation. Such high temperature enhances bonds breaking to generate trap states in the poly-Si, and thus degrades the TFT performance. As can be seen, the fluorination process can greatly alleviate the on-current degradation under a hot carrier stress. We deduce that by using CF_4 plasma treatment, due to the fluorine incorporation at the SiO_2/poly-Si interface, the quality of the interface was greatly improved. The improved interface can result in great enhancement of gate oxide integrity.[22] Moreover, with Si-F bonds formed to replace weak bonds in the poly-Si, the bonds breaking can be eliminated. Hence, damage caused by CHE and SH was suppressed for the fluorinated sample. As a result, device reliability was greatly improved for the fluorinated poly-Si TFT.

Conclusion

We reported a novel fluorinating technique of poly-Si TFTs by employing CF_4 plasma treatment. Using this technique, significant improvements in the performance of fluorinated poly-Si TFTs have been demonstrated. A steeper subthreshold slope, smaller threshold voltage, higher carrier mobility, and better on/off current ratio can be obtained due to the reduction of trap states in the poly-Si and the SiO_2/poly-Si interface. Moreover, the CF_4 fluorinating process also improves hot-carrier immunity. It is concluded that the CF_4 fluorination technique can provide a simple, effective, and process-compatible method to introduce fluorine atoms into poly-Si film to fabricate high-performance as well as high-reliability poly-Si TFTs.

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