Theoretical Analysis of Low Phase Noise Design of CMOS VCO

Yao-Huang Kao and Meng-Ting Hsu

***Abstract*—A theoretical analysis on low phase noise of voltage-controlled oscillators (VCOs) based on complementary cross-coupled LC VCO by 0.35-μm complementary metal oxide semiconductor technology is demonstrated. From the procedure of optimization steps, the excess noise factor of the amplifier coming from the active device has been determined. The proposed VCO operates at 2 GHz with phase noise of −116 dBc/Hz at offset frequency 600 kHz. The power consumption is 22.62 mW under 3 V bias with 9.1% frequency tuning. The achievement of low phase noise is also matched with prediction by formula in the frequency domain.**

***Index Terms*—Complementary metal oxide semiconductor (CMOS), excess noise factor, phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

PREDICTION of phase noise for integrated complementary metal oxide semiconductor (CMOS) voltage-controlled oscillators (VCO) is an essential topic of research. The CMOS technology is viewed as a promising solution for the wireless transceiver on a single chip. As a local oscillator in the transceiver, the phase noise of the VCO is one of the most critical parameters for the quality and reliability. Phase noise in oscillator has been studied extensively [1]–[7]. The feasible design procedure and structure to obtain the low phase noise is still in progress [8]. It has been indicated that the single-sideband power spectral density of phase noise is given by the following [4]

$$L(\Delta\omega) = \frac{KT \cdot R_{\text{eff}} \cdot [1+A] \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2}{P_{signal}}$$

$$G_M = R_{\text{eff}} \cdot (\omega_0 C)^2 = \frac{R_{\text{eff}}}{(\omega_0 L)^2} \tag{1}$$

where R_{eff} is the effective resistance of the LC-tank, which approximately equals the series resistance of the inductor, A is the excess noise factor of the amplifier, ω_0 is the oscillation frequency, $\Delta\omega$ is the frequency offset from the carrier, and P_{signal} is the carrier's power level. This model described well the shape of the spectrum, but the excess noise factor A is another empirical fitting parameter and rarely discussed [3], [4]. Here, in this study, the phase noise of cross-coupled LC VCO is investigated. Based on (1), we optimize the power P_{signal}, factor A, and factor Q to achieve the low phase noise performance. From the procedure of optimization steps, the excess noise factor A of the amplifier coming from the active device has been determined. The achievement of low phase noise is also matched with prediction by formula in the frequency domain.

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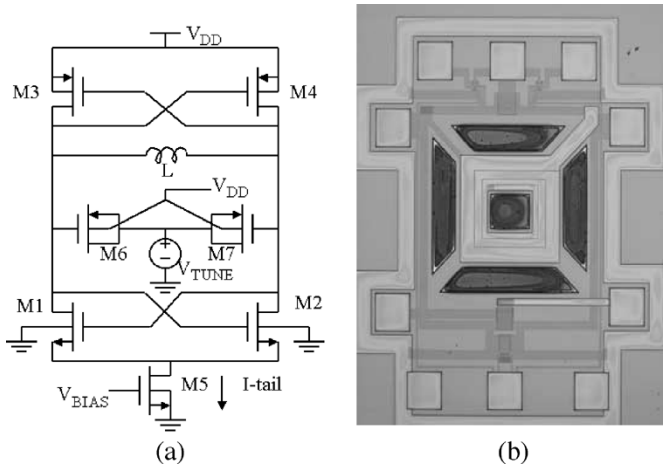

Fig. 1. (a) Core circuit of complementary cross-coupled pair VCO. (b) Die photograph of VCO (dimension 880×1110 μm^2).

TABLE I
SOME PARAMETERS OF VCO

MOSFET Size ($L \times W \times M$)	**0.35μm process**
M1,M2	**0.35μm x 5μm x 60**
M3,M4	**0.35μm x 5μm x 120**
M5	**0.35μm x 5μm x 40**
M6,M7	**0.35μm x 5μm x 80**
Power consumption	**22.62mw**
Phase noise	**-116dBc/Hz at 600KHz offset**
Tuning range	**9.1%**
Figure of merit (FOM)	**-173dBc/Hz at 600KHz offset**

II. Phase Noise in Cross-Coupled LC VCO

The block diagram of a typical cross-coupled VCO and its die photograph are shown in Fig. 1(a)and (b). The cross-coupled pair NMOS transistors M1 and M2 in accompany with the PMOS transistors M3 and M4 has the ability to generate the negative resistance to compensate the LC tank loss. M5 is the current tail. The normally used varactor is inversion-mode MOS varactor (M6 and M7). The details of design parameters for a 2-GHz operation are listed in Table I. The chip size of VCO including pads is 880×1110 μm^2.

The first step in improving the phase noise is to maximize the quality factor of the tank circuit, basically the inductor.

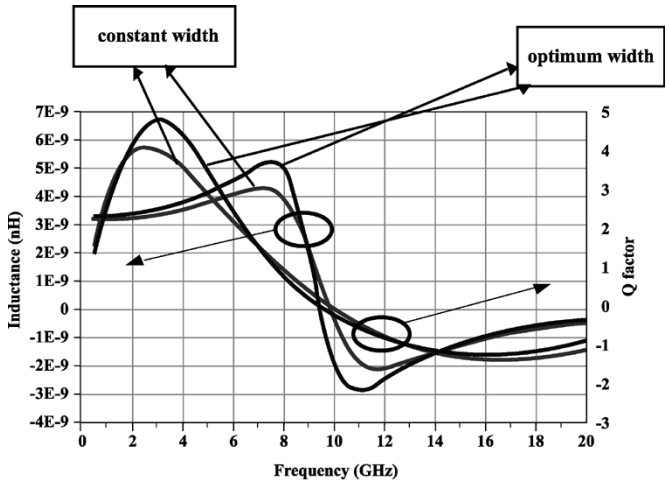

Fig. 2. Measured inductance and Q factor between constant width and optimum width under the same inductance 3.3 nH.

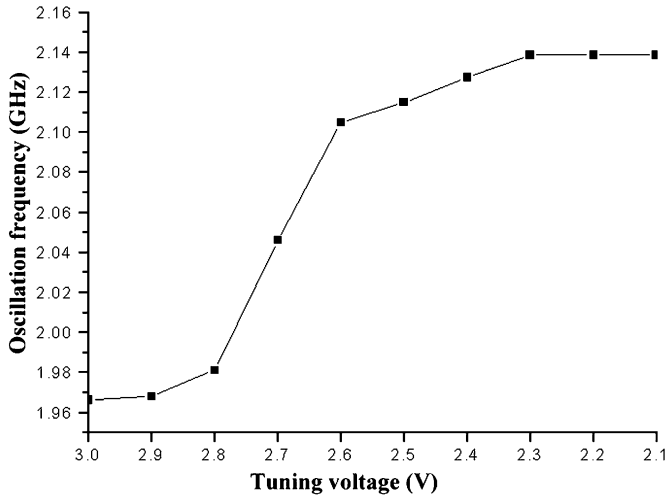

Fig. 3. Measured VCO transfer function.

This work is mainly on the layout optimization of the planar inductor, three general guidelines are adopted to construct a width-varying spiral inductor [4], [5]. The measured inductance and quality factor Q between constant width and optimum width under the same inductance 3.3 nH is shown in Fig. 2. The measured inductance Q factor is about five. The die size of the optimized inductor is 564×564 μm^2. As for varactor, the PMOS is used because of the wide tuning capability and low phase noise. They have good quality values of about 40 at 2 GHz. But the quality factor of the tank is still limited mainly by the performance of the inductor. Fig. 3 shows the tuning range transfer function of the oscillator, and its tuning range is about 9.1%.

The second step is to maximize the signal power in the tank circuit. The circuit is conceptually divided into the passive tank and active circuit as shown in Fig. 4(a). The active part includes the PMOS and NMOS. The negative resistance is inversely proportional to oscillation amplitude as shown in the Fig. 4(b). The dotted line indicates the simulated results and the solid line is the average value by linearization. The trace seems to quite linear at large amplitude, although a slight bending at small amplitude. The behavior around the steady state can be approximated by a

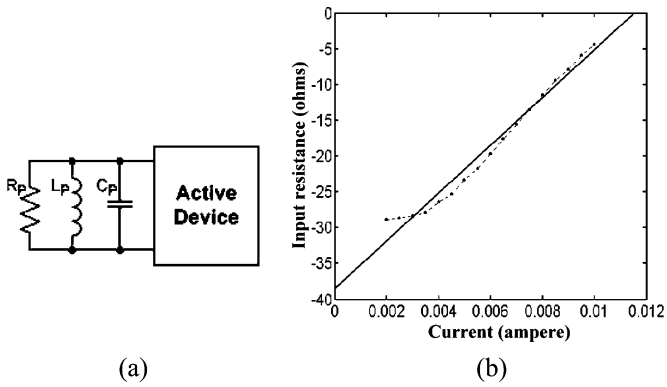

Fig. 4. (a) Conceptual block diagram of oscillator. (b) Dependence of negative resistance of oscillation current at 2 GHz. The dotted line indicates the simulated results and the solid line is the average value by linearization.

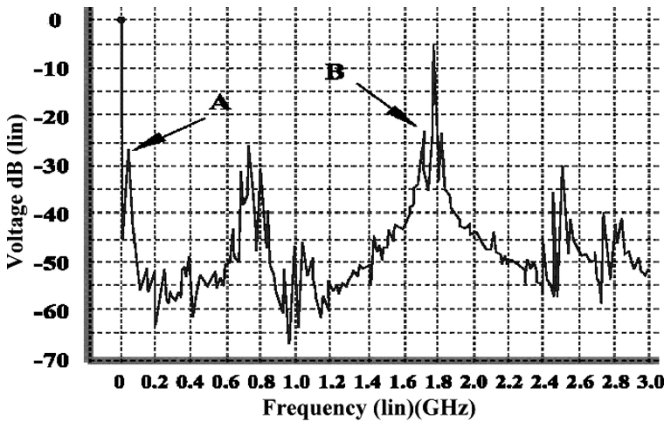

Fig. 5. Oscillator frequency spectrum with current injection at $f_{\rm m} = 50$ MHz.

linear relationship as $R_{\rm in} = -R_0(1 - I/I_{\rm m})$, where $R_{\rm o}$ is the initial value of linear fitting resistance, $I_{\rm m}$ is the maximum value of current with zero negative resistance. The power delivered to the external load $R_{\rm p}$ (oscillator) is maximized as oscillation current amplitude $I_{\rm max} = 2/3I_{\rm m}$ [9]. In our case, $I_{\rm m} = 11.31$ mA and $I_{\rm max} = 7.54$ mA with 3-V supply voltage.

The third step is to trim the ratio of $W_{\rm p}/W_{\rm n}$ to have equal rise and fall time in the waveform. A symmetric waveform is helpful to get the lower $1/f^3$ corner in phase noise. The final step is to minimize the excess noise factor A in (1). Actually, the total noise of VCO is attributed from two parts, one is the total noise source in all active devices, and the other is coming from the nonlinear mixing mechanism in oscillation under large-signal operation [6]. Here, our target is to minimize the excess noise factor coming from nonlinear mixing mechanism. It can be found by the following procedure. It is well known that all the noise source of device can be transformed to one of the output drain node. A small-signal sinusoidal current simulating the low frequency noise at $f_{\rm m} = 50$ MHz is injected into this output node. Then a sideband peak at $f_0 \pm f_{\rm m}$ emerges in the spectrum with simulation results as shown in Fig. 5. The larger difference between sidebands and center carrier is, the more sinusoidal the waveform is [3], [6]. These results indicate in smaller the excess noise factor. It implies that the effect of nonlinear mixing is the minimum. The optimization is a trade off among the drain current, size, and $V_{\rm GS} - V_{\rm T}$ of tail

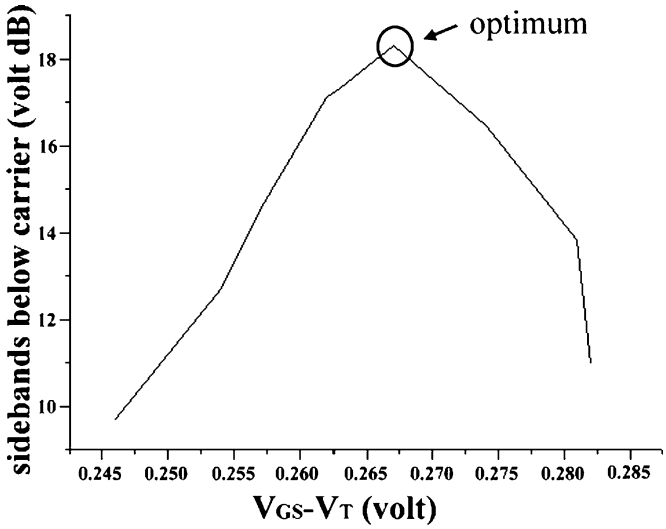

Fig. 6. Level dependence on effective gate voltage.

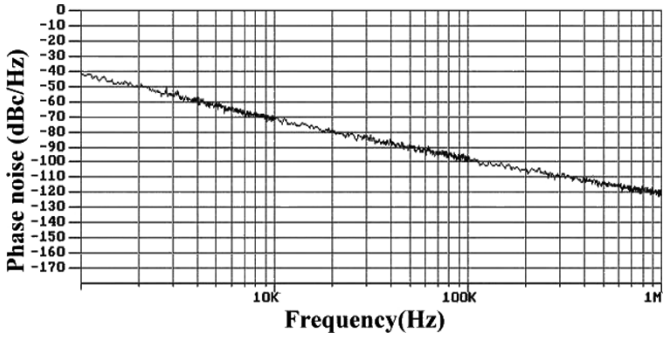

Fig. 7. Measured phase noise at 2 GHz.

MOS with $g_{\rm m}$ of cross-coupled pair keeping constant. Fig. 6 shows the relation between $V_{\rm GS}-V_{\rm T}$ and level difference. The optimum situation is with the largest difference. According to our observation between mark A and mark B in Fig. 5, the excess noise factor A can be reduced to 4 dB [6].

III. Measurement and Discussion

The measured result of phase noise is demonstrated with -116 dBc/Hz at 600 kHz offset as shown in Fig. 7, and the corner frequency of $1/f^3$ is equal to 15 kHz. In our work, the $R_{\rm eff} = 8.84\ \Omega$ at 2 GHz, A =2.51 is deduced from excess noise factor (4 dB) by nonlinear mixing mechanism, and $V_{\rm peak} = 0.92$ V. The calculation of phase noise at 600 kHz offset from (1) is given as $L(600\ {\rm kHz}) = -114.83$ dBc/Hz. The prediction is quite agreement with the measured one.

The VCO performance by means of a figure of merit is defined as [2]

$$\mathrm{FOM(dBc)} = S_{SSB} \cdot \left(\frac{f_{\rm offset}}{f_C}\right)^2 \cdot P_{\rm diss}({\rm mW}) \qquad (2)$$

where $S_{\rm SSB}$ is the signal sideband noise at offset frequency $f_{\rm offset}$. The value of FOM from (2) is -173.2 dBc/Hz. The comparison with some reported papers basing on the same structure and related technology is also listed in Table II. The performance of our work can be compatible with some reported papers. Though a less value of FOM, our VCO has large output power of signal than others.

TABLE II
Comparison With Some Reported Papers Basing on the Same Structure and Related Technology

Reference	This Work	[2]	[7]	[8]
Technology	CMOS 0.35μm	CMOS 0.35μm	CMOS 0.25μm	CMOS 0.18μm
f_o(GHz)	2.06	2.03	2.45	12
Vdd(V)	3	2.5	2.5	1
Power Diss. (mw)	22.62	10	10.6	7.7
Phase Noise (dBc/Hz)	-116@ 0.6MHz	-117@ 0.6MHz	-115@ 0.6MHz	-102@ 0.6MHz
FOM(dBc)	-173.2	-177.6	-176.8	-179.4
Tuning range	9.1%	26%	17.9%	3.33%
Output power(dBm)	2.33	0	NA	NA

IV. Conclusion

The theoretical analysis of a low phase noise VCO with complementary cross-couple pair is presented. From the procedure of optimization steps, the excess noise factor of the amplifier coming from the active device has been determined. The oscillator is implemented by the standard 0.35-μm CMOS technology with phase noise -116 dBc/Hz at 600 kHz offset.

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