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Fabricating Thin-Film Transistors on Plastic Substrates Using Spin Etching and Device Transfer

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This work presents a novel method for transferring thin-film transistors (TFTs) from a Si wafer to another flexible plastic substrate. First, high-performance poly-Si TFTs were fabricated on a 1.5 μm thick SiO_2 on a Si wafer and then attached to a flexible plastic substrate by optical adhesive. Next, spin-etching was utilized to remove the backside Si, using SiO_2 as a stopping layer. A qualitative model was established to explain the relationship between the chemical flow rate/rotation speed to the etching rate and the uniformity of Si removal. The Si etching rate exceeded 200 μm/min while the Si to SiO_2 selectivity of 250 was maintained given optimized spin-etching parameters. Substrate bonding and Si spin-etching steps caused no degradation or yield loss as compared to the electrical characteristics before transference. Additionally, extrinsic stress only weakly affected the properties of poly-Si resistors and TFTs on a flexible plastic substrate.
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Thin-film transistors (TFTs) on flexible plastic substrates are of considerable interest because of several advantages including light weight, thinness, flexibility, shock resistance, and low cost. TFT devices are widely applied to large area electronics such as flat-panel display, "smart" labels on consumer items, smart cards, and sensors, while the small active matrix liquid-crystal display (AMLCD) with extremely high resolution is also in great demand for digital cameras and cellular phones.[1-5] However, the fabrication of high-performance TFTs on plastics is extremely challenging for the following reasons: first, the maximum process temperature must be lower than the glass transition temperature T_g of plastic backplanes so that many conventional high-temperature processes such as oxidation, recrystallization, or activation must be modified. Second, because the thermal expansion coefficient of plastic substrate ($6.2 \times 10^{-5}/°C$) is much larger than that of Si ($2.4 \times 10^{-6}/°C$), film cracking or delaminating may occur. Dimensional instability of substrates also causes difficulties for fine pattering of the devices during photolithography process. Finally, issues of reproducibility and manufacturability on flexible substrates should also be addressed.

Two types of approaches have been considered to overcome these obstacles. One utilizes various low-temperature processes including excimer laser annealing, metal-induced lateral crystallization, plasma-enchanced chemical vapor deposition (PECVD), and sputtering, etc. to fabricate TFTs directly on plastic substrates.[1,5] The other method, indirectly, fabricates TFTs first on a glass or quartz substrate and then transferred the devices to the plastic substrate by etching or laser ablation.[6,7] The authors of this study have also proposed a novel technique of device transfer by backside etching (DTBE) which combines chemical-mechanical polishing (CMP) with wet chemical etching processes to fabricate TFTs on a rigid glass or plastic substrate.[8] Unlike the other methods, the DTBE technique relies on no expensive excimer laser equipment. Furthermore, because the starting material of the DTBE technique is a silicon wafer, its processes are fully compatible with mature complementary metal oxide semiconductor (CMOS) industry where maximum process temperature can be up to 1100°C. Although high-temperature poly-Si TFTs have been fabricated on quartz substrate for years, the extremely high cost of quartz (at least ten times higher than a Si wafer with the same size) limits its application and popularity.[9,10] Contrarily, utilizing DTBE technique, both high-performance integrated circuits and TFT arrays can be easily fabricated by conventional CMOS processes and then transferred from the Si wafer to the other low-melting-temperature substrates.

In this work, the CMP step in the previous DTBE method was replaced by the spin-etching process. In contrast to CMP, the spin-etching process exerts little mechanical stress or thermal stress on the sample, enabling the device to be transferred to a thin flexible backplane. Besides, spin etching consumes fewer chemicals than conventional wet etching; the fresh chemicals keep supplying to the sample during spin etching, so the etching rate is high and the throughput is comparable to conventional wet etching. This investigation examines the spin-etching properties, the mechanism of silicon etching and the electrical characteristics of transferred thin-film devices.

Experimental

Spin-etching process.—Before the backside silicon are removed and the thin-film devices are transferred to a plastic substrate, the properties of the spin-etching process, including the etching rate, the uniformity and the selectivity, etc. should be clarified. Figure 1 schematically depicts the spin-etching equipment; the etching chemicals were dropped into the spinner through a manual valve in a funnel at an adjustable flow rate. The spinner was made of Teflon and was manufactured by Laurell Technologies Corp. A mixture of hydrofluoric acid (HF), nitric acid (HNO_3), and some acetic acid (CH_3COOH) was used as the main etchant for silicon. The spin speed of the samples varied from 1000 to 4000 rpm, while the flow rate of the etchant ranged from 100 to 333 mL/min.

The etching rate of silicon was calculated from the difference between the sheet resistance R_S of a 4 in. wafer before and after spin-etching process, *i.e.*, the change in wafer thickness can be expressed as

$$\Delta \text{ thickness } (T) = \rho/R_{S\text{-before}} - \rho/R_{S\text{-after}}$$

where ρ is the resistivity of a Si wafer.

To test the etching selectivity of Si to silicon nitride or silicon dioxide, a layer of 2300 Å Si_3N_4 or a 6000 Å thick SiO_2 was formed on a Si substrate by LPCVD and wet oxidation, respectively. Both the etching selectivity and the etching uniformity were accurately measured using an ellipsometer.

Fabrication of thin-film devices.—In the DTBE process, both poly-Si resistors and TFTs were fabricated on the 4 in. wafers. First, a 1.5 μm thermal oxide layer was grown on a Si substrate as an etching-stop layer against poly etchant. Then, a 1000 Å amorphous Si layer was deposited by LPCVD at 550°C and patterned to form an active region.[11-13] A 1000 Å thick TEOS-SiO_2 layer by PECVD and a 250 nm thick poly-Si layer by LPCVD at 620°C were then deposited as gate insulator and gate electrodes, respectively. Self-aligned phosphorous implantation at a dosage of 5×10^{15} cm^{-2} with an energy of 60 keV was carried out to generate the source/drain areas.

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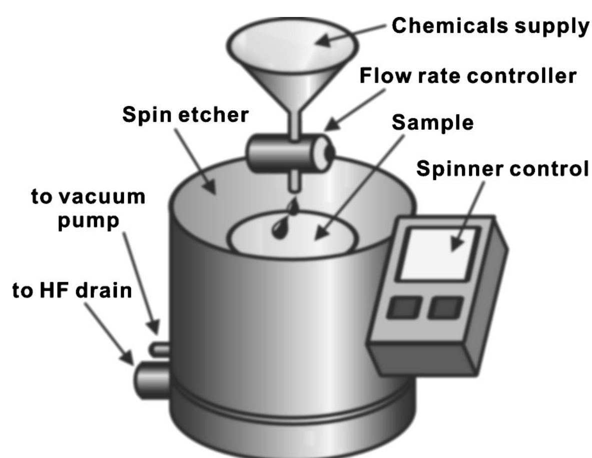


Figure 1. The schematic diagram of spin-etching equipment.

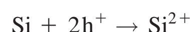
After the passivation oxide was deposited by PECVD and the contact holes were opened, a 5 nm Ni layer was evaporated onto the contact windows and then the samples were annealed at 550°C in a furnace for 48 h to recrystallize the channel region. Next, to further increase the grain size and active the dopants simultaneously, the samples were annealed in an N_2 ambient at 900°C for 1 h, resulting in the so-called "secondary crystallization" effect.[13] Afterward, the samples underwent a standard backend process to form the source/drain and gate metallization. Finally, a passivation process using NH_3 plasma was performed for 1 h.[14] The cross-sectional view of the finished TFT was shown in Fig. 2a. Before the thin-film devices were transferred to the plastic substrate, the electrical characteristics of the TFTs and poly-resistors were measured using Agilent 4156 semiconductor-parameter analyzer.

Device transfer process.—After the device characteristics were measured, a 3000 Å TEOS-oxide was deposited on the surface to protect the TFTs from damage by the organic adhesive. Next, as shown in Fig. 2b, the wafer (with devices on it) was bonded to a flexible plastic substrate with a thickness of 110 μm by the optical adhesive and then cured at 80°C for 3 h on a hot plate. Afterward, spin-etching process with Si etchant was applied to remove the backside Si. As the thickness of the backside Si was reduced, the flexible plastic substrate tended to deform because it had a low Young's modulus. Accordingly, a supporting glass substrate had to be attached below the plastic substrate to prevent the samples from cracking during the etching process of backside silicon.

The spin etching step automatically stopped because the Si etchant has a high etching selectivity of 250 to the etching-stop layer, SiO_2. Finally, a photolithography process was performed to open the contact pads, as indicated in Fig. 2c. Again the electrical characteristics of TFTs or poly resistors were measured to examine the influence of DTBE.

Results and Discussion

Spin etching process.—The etchants most commonly used in the isotropic etching of silicon are mixtures of hydrofluoric acid (HF), nitric acid (HNO_3), and acetic acid (CH_3COOH), the so-called HNA system[15] or poly etcher. The reaction is initiated by promoting Si from its initial state to a higher oxidation state



$$Si + 2h^+ \rightarrow Si^{2+}$$

The holes are produced by the following autocatalytic process

$$HNO_3 + HNO_2 \rightarrow 2NO_2^- + 2h^+ + H_2O$$

$$2NO_2^- + 2H^+ \rightarrow 2\ \ HNO_2$$

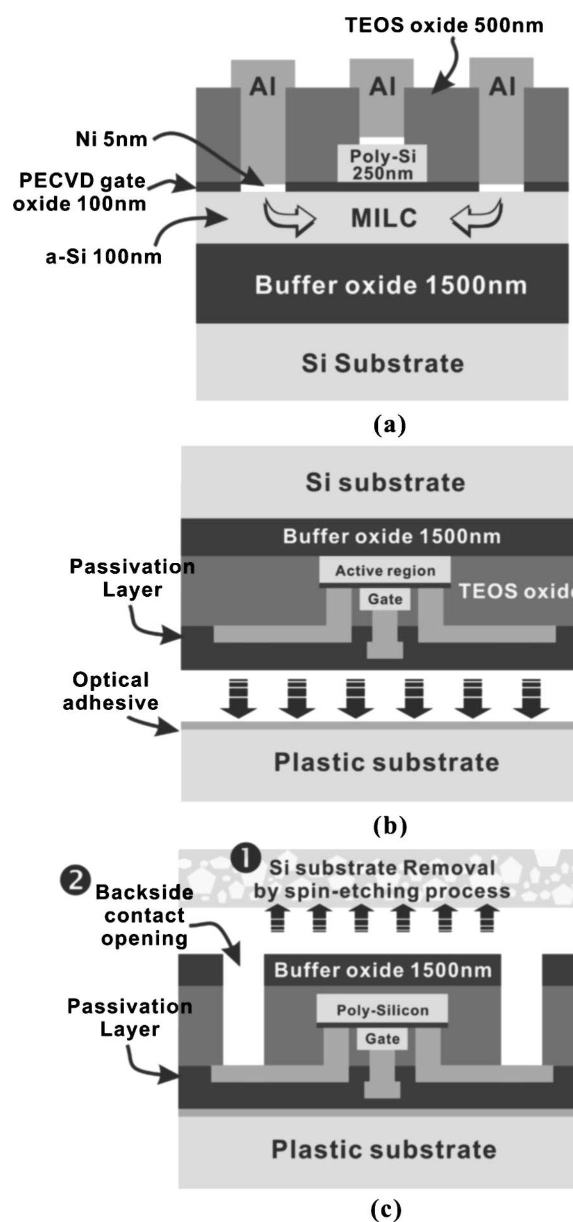
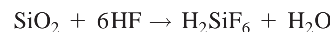


Figure 2. The process flow of device transfer by backside etching (DTBE) technique.

Si^{2+} combines with OH^- (from the dissociation of H_2O) to yield $Si(OH)_2$, which subsequently liberates H_2 to form SiO_2. SiO_2 then dissolves in HF



$$SiO_2 + 6HF \rightarrow H_2SiF_6 + H_2O$$

The overall reaction can be written as

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2$$

Here, the acetic acid acts as a buffer agent, which controls the dissociation of the nitric acid and preserves the oxidizing power of HNO_3 over a wide range of dilutions during etching.

The most serious problem encountered during backside etching concerns the process temperature. Because the thermal expansion coefficients of Si and the polymeric materials are significant, the plastic substrate easily rolls up and cause the Si to peel away from the plastic during the exothermic reaction of backside etching process. Moreover, several plastic substrates and adhesives are eroded

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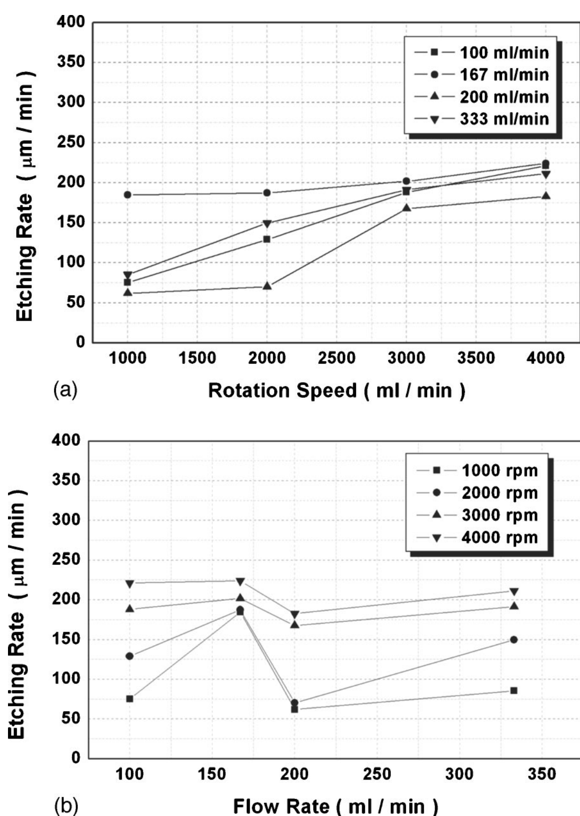

Figure 3. Etching rate *vs.* (a) rotation speed and (b) chemical flow rate.

by hydrofluoric or nitric acid, so the conventional wet etching cannot be applied to them. In spin etching, however, the sample is spun at a high speed, while the fresh cooling chemicals are supplied continuously to the wafer surface; accordingly, the influence of temperature is almost eliminated and the plastic substrate or adhesives are not damaged.

Figures 3a and b plots the curves of etching rate versus flow rate and rotation speed, respectively. Figure 3a reveals that the etching rate increases with the rotation speed, and that the maximum etching rate exceeds 200 μm/min at the highest spin speed of 4000 rpm and a chemical flow rate of 167 mL/min. Consequently, spin etching is a very efficient process compared to conventional wet etching ($\sim$2 μm/min at 25°C). Given a 4 in. wafer with a thickness of 550 μm, the DTBE process can be completed in 3-5 min. Nevertheless, Fig. 3b shows no apparent relationship between the etching rate and the flow rate at a fixed spin speed. Specifically, the etching rate reaches a maximum at the flow rate of 167 mL/min and considerably declines above a flow rate of 200 mL/min.

A simple mechanism of spin-etching process depicted in Fig. 4 is proposed to further explain the observed phenomenon. The etching procedure involves three steps: (*i*) First, a boundary layer is formed near the silicon surface where the etching species are rapidly consumed. All of the reactants diffuse through this boundary layer to support the reaction (mass transport control), (*ii*) then, reaction species at the surface, *e.g.*, HNO_3 and HF, will react with Si, in a process that depends strongly on the temperature (surface reaction control), and finally (*iii*) the reaction products diffuse through the boundary layer and return to the bulk of the liquid (product diffusion control).

In spin-etching, the spin speed mainly affects steps (*i*) and (*iii*), because a higher rotation speed yields a thinner boundary layer and thus a faster diffusion rate of both reactants and products. Accordingly, as shown in Fig. 3a, the etching rate keeps increasing with spin speed at every flow rate and gradually saturates when the rotation speed larger than 3000 rpm, implying that the system is then in the surface reaction control regime. In this regime, increasing the flow rate of etching chemicals may cool the surface of the sample and slightly change the reaction rate.

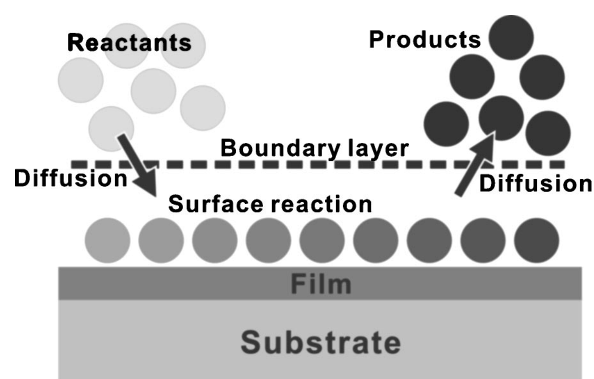

Figure 4. The proposed mechanism of spin-etching process.

At a low rotation speed (<2000 rpm), however, the total process is more like a conventional wet etching rather than a spin etching. Without help from the centrifugal force, the reaction products near the silicon surface would now be repelled by the supplied chemicals so that the etching rate increases with the flow rate from 100 to 167 mL/min, as shown in Fig. 3b, indicating that the system is in the diffusion control regime. Moreover, the system leaves the diffusion control regime and enters the surface reaction control regime as the flow rate increases. The etching speed then decreases significantly owing to the cooling effect of chemicals.

Figure 5 shows the etching rate with respect to the etching uniformity for Si_3N_4. A 4 in. wafer with a Si_3N_4 layer of 2300 Å was spun and etched by the poly etchant for 360 s; every 120 s, the etching process was terminated and the film thickness of Si_3N_4 was measured using an ellipsometer. The rotation speed was 4000 rpm and the flow rate was 100 mL/min. From Fig. 5, we find that not only was the etching rate from the wafer center to the edge very uniform, but the etching repeatability was also satisfactory. (Data on the thickness of the film near the wafer edge could not be obtained using our equipment.) The etching selectivity of Si to Si_3N_4 is larger than 10^4, indicating that the silicon nitride formed by LPCVD is an ideal etching stop layer against poly etchant.

The etching characteristics of poly etchant for SiO_2 were also investigated. As shown in Fig. 6, the etching rate increases with the flow rate, and gradually saturates at a flow rate above 200 mL/min.

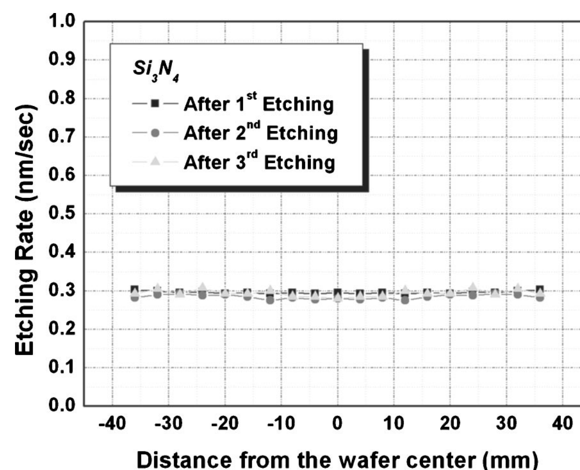

Figure 5. The spin-etching uniformity of the silicon nitride film obtained by poly etchant.

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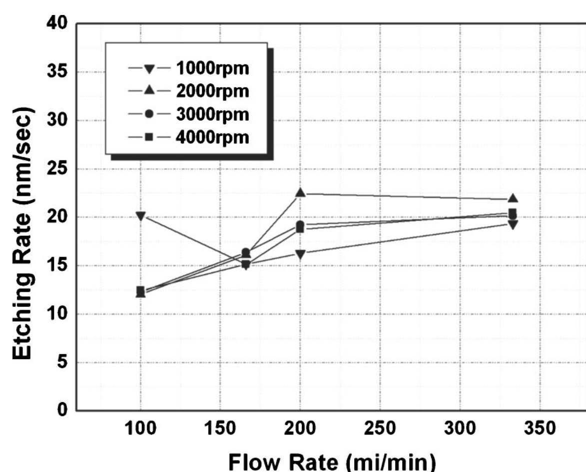


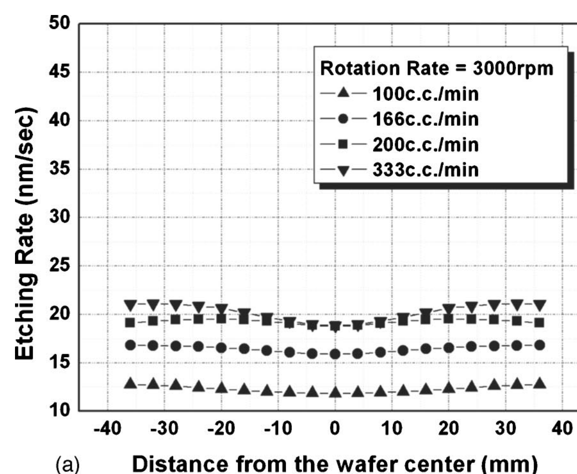
Figure 6. The spin-etching rate of silicon dioxide versus chemical flow rates under different spin speed.

Because the relative concentration of hydrofluoric acid was low in our poly etchant and the hydrofluoric acid was consumed very quickly during etching, the etching mechanism is diffusion-controlled and this mechanism depends on the chemical refresh rate. Additionally, the rotation speed negligibly influences to etching rate, except at 1000 rpm. It is notable that the etching rate greatly increases at the lowest flow rate (100 mL/min) and rotation speed. We presumed that the temperature at the surface had arisen, resulting in the increment of surface reaction rates. The etching selectivity of Si to SiO_2 is larger than 150. Although this value is inferior to that of silicon nitride, a thick SiO_2 stop layer with lower stress than Si_3N_4 can be formed through wet oxidation and patterned easily with HF. Consequently, we chose SiO_2 rather than Si_3N_4 as an etching stop layer in DTBE process.

Figures 7a and b compare the etching uniformity for SiO_2 with different rotation speeds. From Fig. 7a, we can observe a U-shaped curve of etching uniformity, but the etching uniformity can be improved by increasing the rotation speed, as indicated in Fig. 7b. A similar phenomenon can also be found during backside Si etching. Figure 8 shows a photograph of devices after they were transferred to another plastic substrate by DTBE technique at a spin speed of 4000 rpm and a flow rate of 167 mL/min. The TFT arrays were originally fabricated on a 4 in. (10 cm diam) wafer. During spin-etching, the etching rates near the wafer edge and that at the wafer center were higher than that in other areas, so the patterns that had been in these areas were destroyed by poly etchant even when a protecting oxide stop layer was present. Finally, the transferred devices formed a ring-shaped pattern with a diameter of 5 cm. To solve this problem of nonuniformity, the nozzle structure should be modified to spray the etchant more evenly to make the etching rates equal all over the wafer. Efforts to transfer larger samples using the DTBE technique are under way. In this work, we transferred TFTs or poly resistors from a 4 × 4 cm chip of a Si wafer for a better yield of experiments.

Fabricating of thin-film devices by DTBE.—Because the devices were not directly fabricated on the plastic substrate using DTBE method, the characteristics of the plastic substrates were not strictly constrained. Nevertheless, the following properties for an optimal polymeric backplane are still required

1. The glass transition temperature T_g of a plastic substrate should exceed 130°C, because the samples after being transferred would undergo a photolithography process with a hard baking temperature of 120°C for the photoresist.



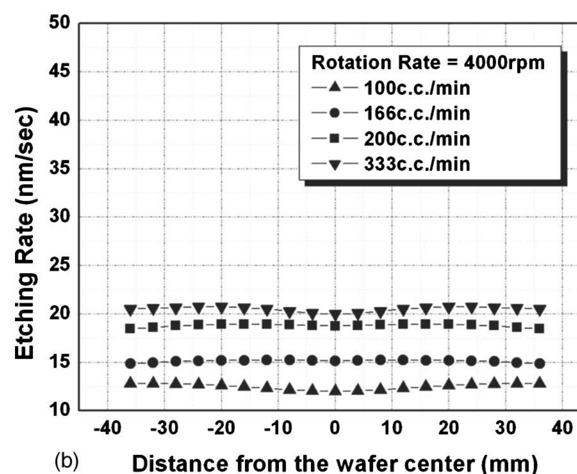


Figure 7. The spin-etching uniformity of silicon dioxide obtained at a spin speed of (a) 3000 rpm and (b) 4000 rpm.

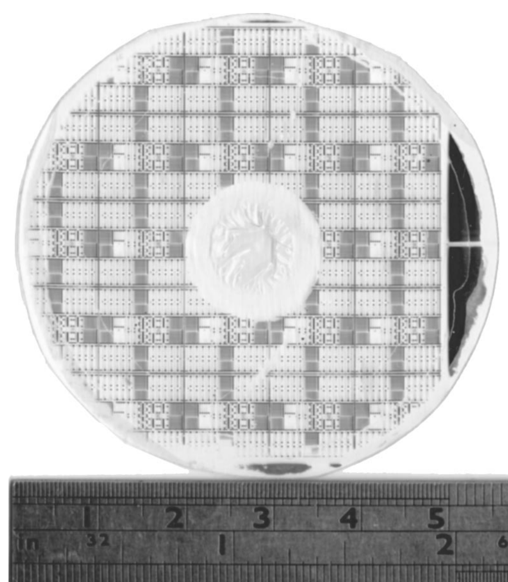


Figure 8. A ring-shaped pattern with a diameter of 5 cm formed by DTBE.

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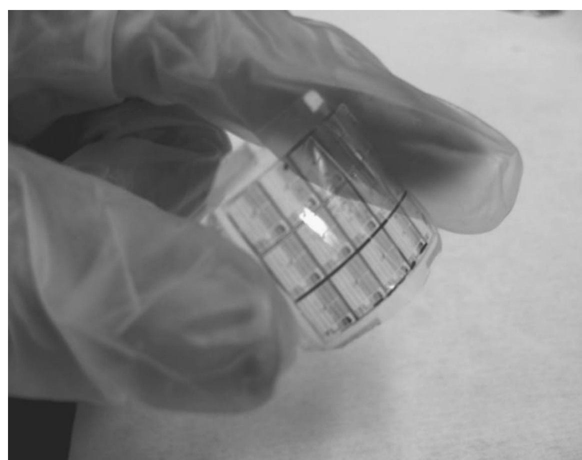
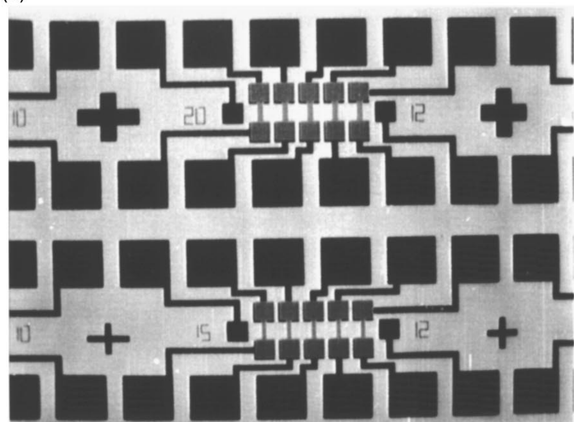

(a)



(b)

Figure 9. (a) Photograph of several TFT arrays transferred to a flexible plastic substrate, and (b) photograph of optical microscopy observed with back light source.

2. The optimal polymeric backplane should have good chemical resistance, especially to HF, HNO_3, development (TMAH) and acetone (ACE).

3. It should have a low thermal expansion coefficient to ensure the accuracy of alignment during lithography process.

4. The substrate should have a high transparency and low reflectance for a transmission-type image display.

5. The substrate should have a low moisture absorption.

Many conventional plastic substrates including polyethersulfone (PES), polyarylate (PAR), polycarbonate (PC), and polyethylene terephthalate (PET) meet the above criteria, but we utilized a new kind of cyclic olefin polymers (COP) named ARTONfilm in this work.[16] ARTONfilm, purchased from JSR corp., possesses several advantages such as good light transmittance above 93%, high T_g of 170°C, low water absorption and good adhesion to hard coatings, etc. Besides, the requirements for optical adhesives are similar to that for plastic substrate.

Figure 9a presents a flexible ARTON substrate on which the thin-film devices had been transferred successfully. The finished die size was 3 × 3 cm. The optical microscope image of these devices observed with back light source is shown in Fig. 9b. The dark regions represent aluminum pads, poly-Si gates, and S/D electrodes, which are all opaque, while the white area is the transparent plastic substrate, adhesive, and SiO_2. The backside Si had been thoroughly removed during spin-etching process and no physical damage was observed.

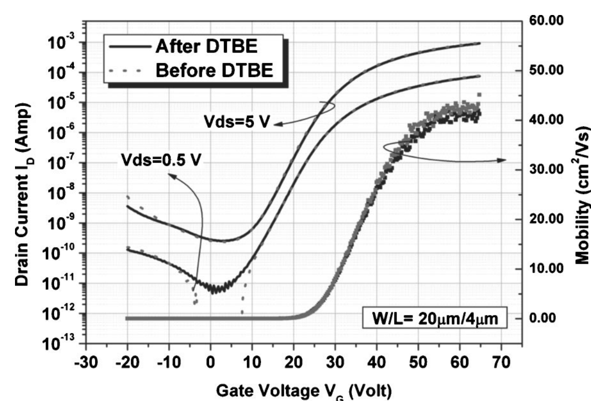


Figure 10. I_D-V_G curves and mobility curves of TFTs before and after DTBE process.

Electrical characteristics of thin-film devices after DTBE.—Figure 10 illustrates the I_D-V_{GS} and field-effect mobility curves of a TFT before and after DTBE. Notably, the DTBE process does not degrade the electrical characteristics of TFTs, such as threshold voltage, mobility, ON/OFF current ratio and subthreshold swing. The field-effect mobility is 43 cm^2/V s, as determined by[17]

$$\mu_{FE} = \frac{L}{C_{ox} \cdot W \cdot 0.1} \times g_m \quad [1]$$

where L is the channel length, W is the channel width, C_{ox} is the gate oxide capacitance, and g_m is transconductance. The ON/OFF current ratio is larger than 10^6 when the threshold voltage is around 10 V. The variation of electrical properties was not observed, especially the anomalous improvement of field-effect mobility and subthreshold swing found in the author's previous work.[8] Here, the samples were all passivated by NH_3 plasma and the trap states in the grain boundary were not affected when the capping oxide layer was deposited.

The electrical characteristics of devices on a bending substrate in a flexible display should not be degraded. Statistically, Fig. 11 summarized several key electrical properties of TFTs with different gate length (while gate width = 20 μm) before and after transfer. Each data point was averaged by at least three devices and then normalized to the value of the gate length equal to 8 μm. For example

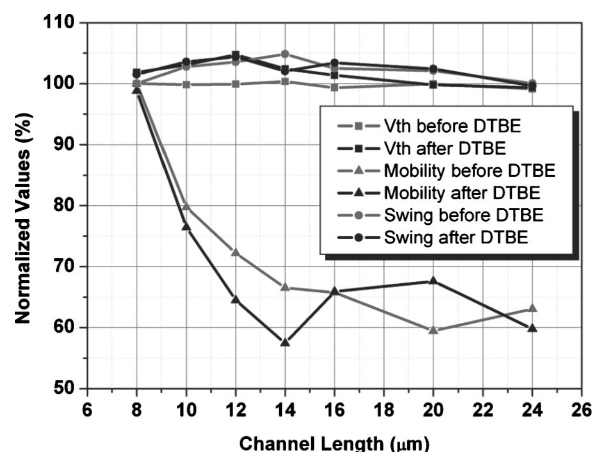


Figure 11. Normalized electrical characteristics of TFTs after DTBE process versus channel length.

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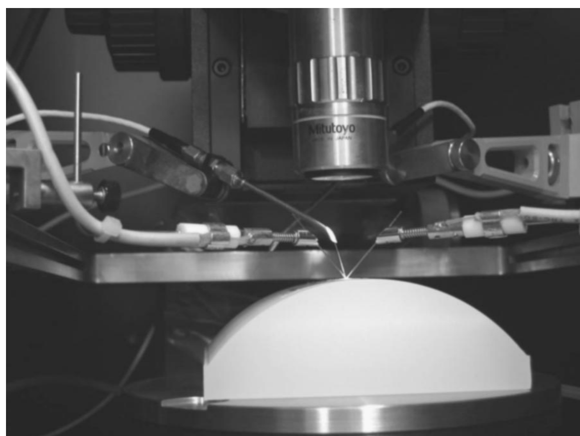

Figure 12. The testing base and probes for bending measurements.

$$\text{Normalized mobility } \mu_{W/L=20/10}^{norm} = \frac{\mu_{W/L=20/10}}{\mu_{W/L=20/8}} \times 100\% \quad [2]$$

It can be found that both the threshold voltage and subthreshold swing exhibit no dependence on the channel length while the field-effect mobility decreases with increasing the gate length, because the efficiency of Ni-induced lateral recrystallization initiated at the source/drain contacts becomes poorer for a longer distance of silicide diffusion. The TFTs with short gate length thus occupy fewer defective grain boundaries and contribute to high field-effect mobility. Besides, for DTBE technique, the devices on a wafer underwent several bonding (annealing of the optical adhesive), etching and photolithography processes; accordingly, the electrical characteristics of TFTs would be influenced slightly by heat, organic contaminants, or moisture generated in these steps, resulting in a larger deviation of electrical characteristics than those before the transfer processes.

To examine the influence of mechanical stress on the device performance, several testing bases with various radii of curvature were made; the poly resistors or TFTs after transfer were fixed to the testing base and the electrical characteristics were measured, as shown in Fig. 12. Figure 13 plots the confidence interval (CI) of poly resistance in different bending cases. The average resistance dose not change after DTBE even at the smallest bending curvature of 2 cm, but the distribution of resistance is wider than those before transfer. Additionally, Fig. 14 illustrates the electrical properties of TFTs with W/L = 20 μm/8 μm under various radii of bending curvature, where parallel bending means that the direction of strain is

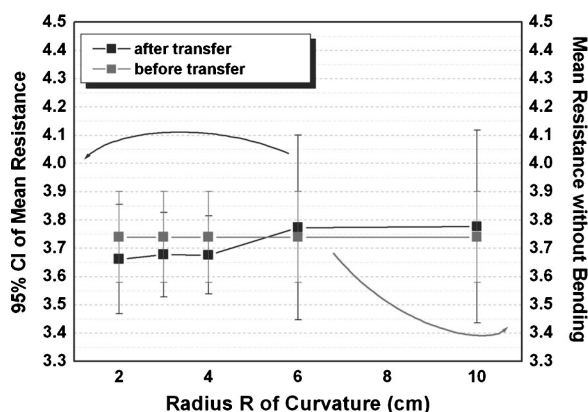

Figure 13. Resistance of poly resistors measured under different bending curvatures.

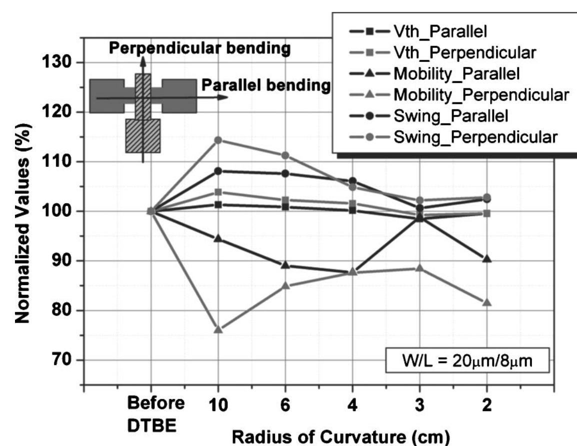

Figure 14. Comparison of electrical properties of TFTs before DTBE and that measured at various bending curvatures after DTBE.

parallel to the current path. And the devices under bending tests all suffer compressive stress since the TFTs after DTBE were upside-down attached to the testing base. The experimental data are normalized to the value before DTBE. According to the research of Wagner *et al.*, the mobility of amorphous Si TFTs would slightly decrease with increasing the compressive strain because of possible variation of optical bandgap of a-Si:H under compression.[18] Nevertheless, no significant correlation between the electrical properties of TFTs and different bending curvatures can be found in Fig. 14. We speculate that the elastic optical adhesive as well as thick etching stop/capping oxide layers may absorb the extrinsic stress during bending tests, and therefore the thin-film devices sandwiched between these layers suffer lower stress. Actually, when low modulus, small thickness substrate, and encapsulation are used, the thin-film approximation breaks down and the whole structure can be bent to extremely small radii, even being folded like a map.[19,20]

Conclusions

Fabricating high-performance thin-film transistors on plastics is extremely challenging. This work proposed an indirect process for transferring thin-film devices on a silicon wafer to another polymeric backplane. Spin-etching process was applied to overcome the issues about heat and mechanical stress resulted from CMP or conventional wet chemical etching. Moreover, the electrical characteristics of poly-Si resistors or TFTs are not changed after transfer process or the bending measurement, confirming that the device transfer technique with backside spin-etching process a practical means of fabricating thin-film devices on a flexible plastic substrate or fragile glass substrate. The DTBE technique is highly compatible with the conventional high-temperature CMOS process. If it could be combined with modern Ni-mediated crystallization or continuous grain silicon technology, the integration of a display and complex logic circuits on a plastic substrate can be expected in the near future.[13,21]

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