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Effects of Low-temperature NH_3 Treatment on the Characteristics of HfO_2/SiO_2 Gate Stack

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The effects of postdeposition low-temperature (~400°C) NH_3 treatment (LTN treatment) on the characteristics of the HfO_2/SiO_2 gate stack with the TiN gate electrode were studied in this work. After the HfO_2 films were deposited using an AIXTRON Tricent atomic vapor deposition system, the LTN treatment was performed prior to the postdeposition annealing (PDA) step to prevent the growth of an additional interfacial layer, which is known to accompany the traditional high-temperature nitridation technique. The effective electrical oxide thickness for the devices annealed at 700°C PDA, either with or without LTN treatment, was estimated to be about 2.2 and 2.3 nm, respectively, without considering quantum effects. It was found that the LTN treatment effectively improves the characteristics of the HfO_2/SiO_2 stack gates, such as capacitance-voltage (*C-V*) characteristics, frequency dispersion, trap generation rate, and dielectric breakdown voltage even at the high PDA temperature of 700°C.
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For aggressively scaling devices into a nanometer regime, the concomitant thinning of SiO_2 gate dielectric has been approaching its physical and electrical limits. The main hurdle encountered is the intolerably huge leakage current caused by the direct quantum tunneling of carriers through these ultrathin oxides. Recently, high-*k* materials have been extensively studied to take advantage of their capability of maintaining the drive current while substantially suppressing the leakage current due to the increased physical thickness at the same equivalent oxide thickness (EOT). Among them, HfO_2 is highly attractive owing to its relatively high dielectric constant (~25), sufficiently large bandgap (~5.9 eV), suitable tunneling barrier height for both electrons and holes (>1 eV), and thermal compatibility with contemporary complementary metal oxide semiconductor (CMOS) processes.

Nitridation of the Si surface by high-temperature (600-700°C) NH_3 treatment prior to the deposition of the high-*k* gate dielectrics has been shown to be effective in not only suppressing the undesirable interfacial layer formation, which is helpful in minimizing the EOT value, but also preventing the boron penetration.[1,2] However, nitrogen can readily diffuse through the high-*k* films and pile up at the interface at such high temperatures, resulting in higher densities of the interface states and near-interface bulk traps, which in turn lead to a larger hysteresis and channel mobility degradation.[2-5] In this study, therefore, we used the low-temperature NH_3 (LTN) process immediately after the deposition of HfO_2 thin films to suppress the diffusion of nitrogen in order to achieve high-quality gate dielectrics with low defect densities both at the interface and in the bulk without causing a significant increase in EOT. We found that the incorporation of LTN treatment does not cause additional growth of the preexisting interfacial layer during a subsequent high-temperature annealing step. Further, the LTN treatment also improves the electrical properties of the HfO_2/SiO_2 gate stack, including lower interface defect density and less frequency dispersion. Moreover, the LTN treatment can remarkably reduce the trap generation in the HfO_2/SiO_2 gate stacks when subjected to high stressing conditions and the increase of the gate leakage with subsequent higher-temperature PDA.

Experimental

Metal-oxide-semiconductor (MOS) capacitors were fabricated on p-type (100)-oriented silicon wafers with a resistivity of 8–10 Ω cm utilizing conventional local oxidation of silicon (LOCOS) isolation. After HF-last dipping, a thin oxide layer of approximately 15 Å was grown in an O_2 ambient at 800°C, at a ramping rate of 200°C/s, by rapid thermal annealing (RTA). Next, an HfO_2 film of approximately 4 nm was deposited at a substrate temperature of 500°C by atomic vapor deposition (AVD) in an AIXTRON Tricent system. Prior to the PDA treatment, some samples were subjected to the LTN treatment in a pure NH_3 ambient at a substrate temperature of 400°C for 5 min in 30 mbar ambient. Then all wafers were subjected to the PDA treatment, either at 600 or 700°C, in an N_2 ambient for 60 s. A 2000 Å TiN electrode was subsequently sputtered and patterned to form the gate electrodes. Afterward, aluminum was sputtered on the wafer back side to form a back side electrode. In order to clearly study the effects of LTN, no other anneal treatments were performed after back side electrode formation. High-resolution transmission electron microscopy (HRTEM) was used to monitor the physical thickness of the gate stacks. For electrical analysis, an Agilent 4284, a precision impedance meter, was used for capacitance-voltage (*C-V*) measurement, and a semiconductor parameter analyzer, Agilent 4156A, was used for current-voltage (*I-V*) measurements and constant voltage stress (CVS). The EOT values of the gate stacks were estimated from 100 kHz *C-V* measurements, using the North Carolina State University CVC method without considering quantum effects.[6] The CVS estimation was performed at constant voltage stress $V_g = -3.75$ V and trap generation rate was evaluated at $V_g = -1$ V.

Results and Discussion

Figure 1a-d shows HRTEM images for the 500°C-deposited HfO_2/SiO_2 gate stacks after various post-deposition treatments. Specifically, Fig. 1a shows the as-deposited film, Fig. 1b shows the film subjected to a 600°C PDA, Fig. 1c shows the film subjected to a 700°C PDA, and Fig. 1d shows the film with LTN treatment and 700°C PDA. We can clearly see that the physical thickness of the interfacial oxide layer does not change significantly even after the high-temperature 700°C PDA. This indicates that the interfacial thermal oxide is rather stable and is not affected by the LTN. It is observed that the extent of crystallization in the HfO_2 film becomes more apparent with increasing PDA temperature. In contrast, the film undergoing the LTN treatment prior to the high-temperature PDA of 700°C, as shown in Fig. 1d, does not show any evidence of crystallization.

Figure 2a shows the high-frequency (100 kHz) *C-V* characteristics of all samples subject to various post-deposition conditions. It is observed that the distortion that occurs in the *C-V* curves can be significantly suppressed with increasing PDA temperature. The origin of the hump near 0 V in the *C-V* curves is believed to be closely related to the presence of fast interface states, since their positions

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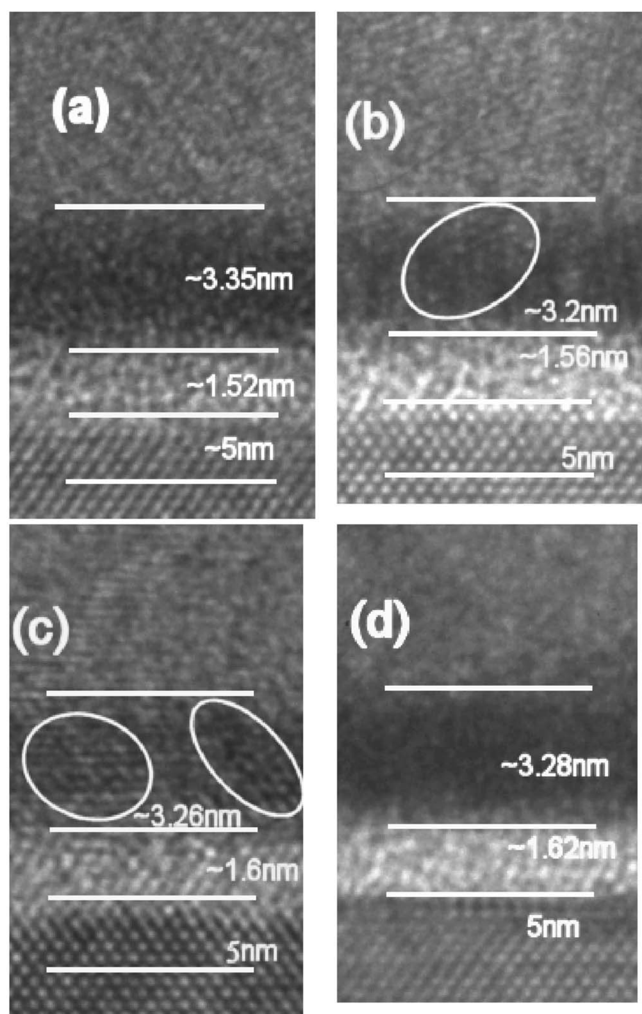

Figure 1. Cross-sectional HRTEM images of the HfO_2/SiO_2 gate stacks (a) for as-deposited film; (b) annealed at 600°C; (c) annealed at 700°C; and (d) annealed at 700°C and subjected to LTN treatment.

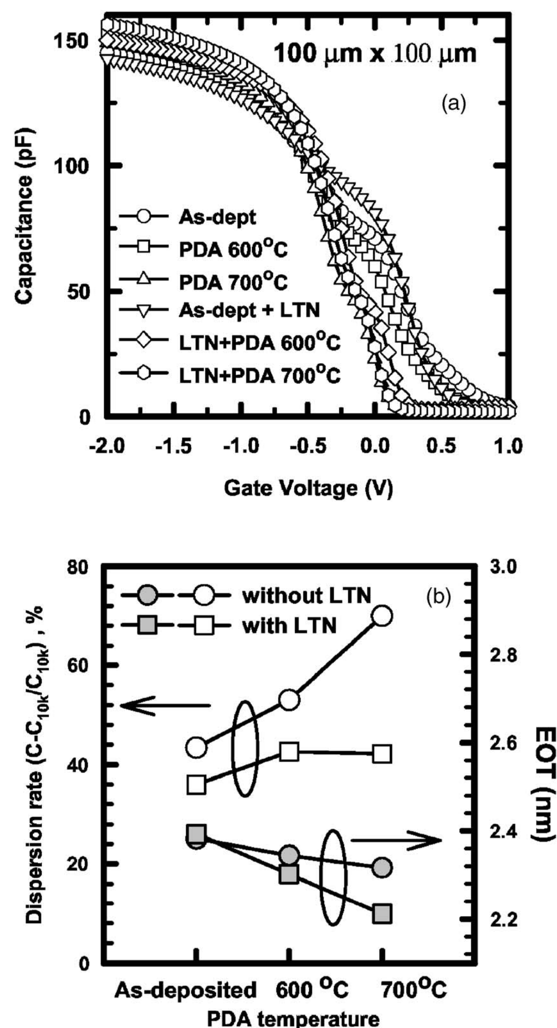

Figure 2. (a) *C-V* characteristics and (b) frequency dispersion rates and EOT values of the HfO_2/SiO_2 gate stacks with/without LTN for various temperatures PDA.

are located in the depletion region.[7] The incorporation of LTN treatment can substantially lower the PDA temperature needed to smoothen the distortion. Moreover, another benefit of the LTN treatment is its capability of suppressing the increase in EOT value even after undergoing high-temperature PDA. This is speculated to arise from an increase in the overall *k* value of the gate stack because extremely low thermal budget causes less low-*k* interfacial layer formation.[8] The frequency dispersion rate is displayed in Fig. 2b. For the samples without LTN, the frequency dispersion rate worsens upon increasing PDA temperature, while the samples with LTN only depict a slight increase with increasing PDA temperature. This trend suggests that there are more defects presented in the HfO_2/SiO_2 gate stack without LTN.[9]

The hysteresis widths for the annealed HfO_2/SiO_2 gate stacks with and without LTN are shown in Fig. 3. Obviously, the LTN treatment leads to smaller hysteresis. Due to the serious distortion in the *C-V* curves for the as-deposited samples with/without LTN, as well as the 600°C PDA-annealed sample without LTN, their hysteresis values cannot be precisely determined and are not shown.

Figure 4 displays the gate leakage current density as a function of gate voltage for the as-deposited and PDA-annealed HfO_2/SiO_2 gate stacks, both with and without LTN. The magnitude of leakage current density increases monotonically for the samples without LTN with increasing PDA temperatures. This trend is thought to be caused by the crystallization of HfO_2 thin films at higher PDA

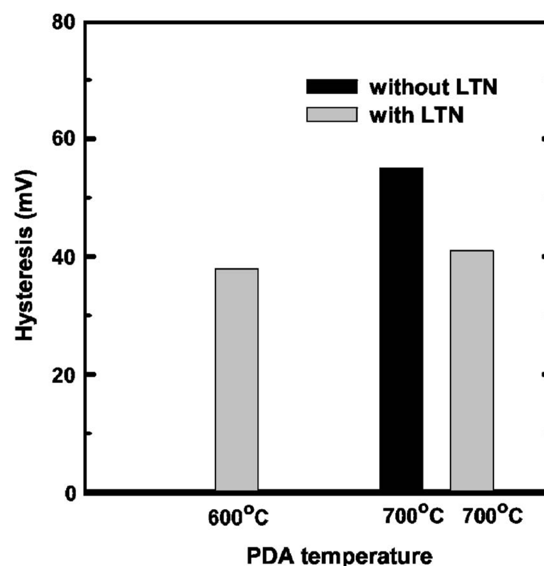

Figure 3. Plot of hysteresis as a function of the PDA temperature of the HfO_2/SiO_2 gate stacks with/without LTN.

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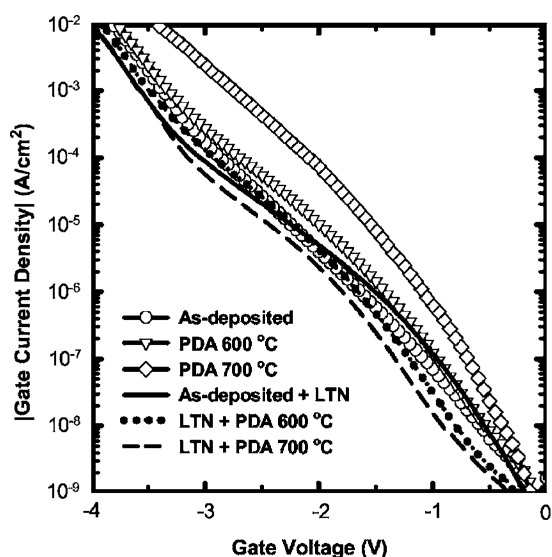

Figure 4. *J-V* characteristics of HfO_2/SiO_2 gate stack with/without LTN for various PDA temperature treatments.

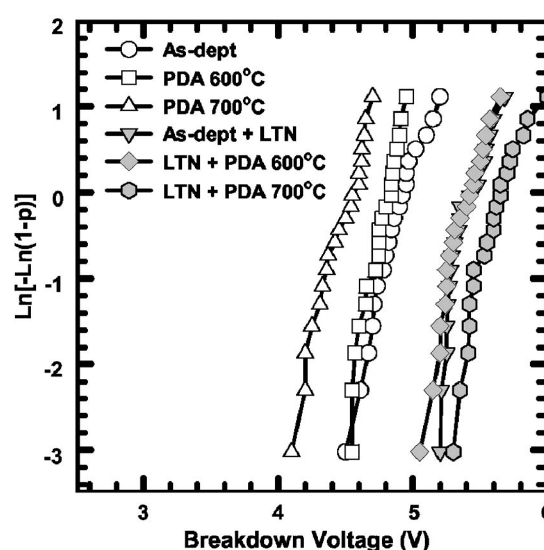

Figure 6. Weibull distributions of dielectric breakdown voltage for the HfO_2/SiO_2 gate stacks, with/without LTN, with various temperatures PDA treatments.

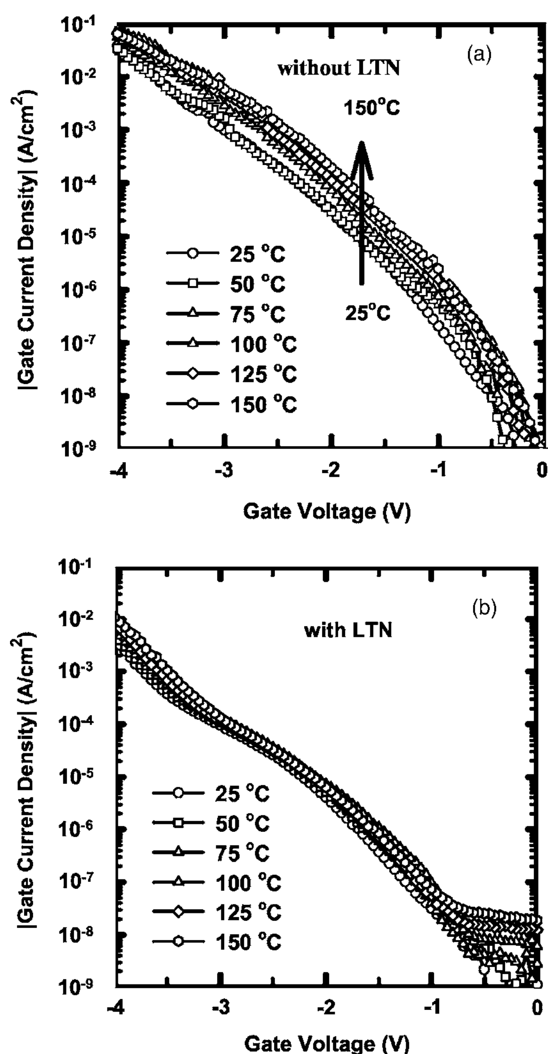

Figure 5. Dependences of gate leakage current density on temperature for the 700°C PDA-treated HfO_2/SiO_2 gate stacks with or without LTN.

temperatures.[10] Similar to the previous results, the LTN can effectively suppress the leakage current increase after high-temperature PDA, because nitrogen incorporation can help to improve the thermal stability of HfO_2 and increase the crystallization temperature.[1-4]

Figure 5 shows the dependence of gate leakage current density on the measuring temperature for the HfO_2/SiO_2 gate stacks annealed at 700°C PDA, without (Fig. 5) and with (Fig. 5b) LTN treatment. Without LTN treatment, the conduction mechanism in the resultant gate dielectrics is related to Frenkel-Poole emission or trap-assisted tunneling,[11,12] while the conduction mechanism with LTN treatment is more likely to be related to Fowler-Nordheim conduction, because the variation of the gate leakage with varying measuring temperature is significantly suppressed. This result strongly suggests that there are fewer defects in the LTN-treated sample, which might be due to fewer grain boundaries as a result of better thermal stability and/or the passivation of incomplete bonds in the bulk by the nitrogen atoms.[13]

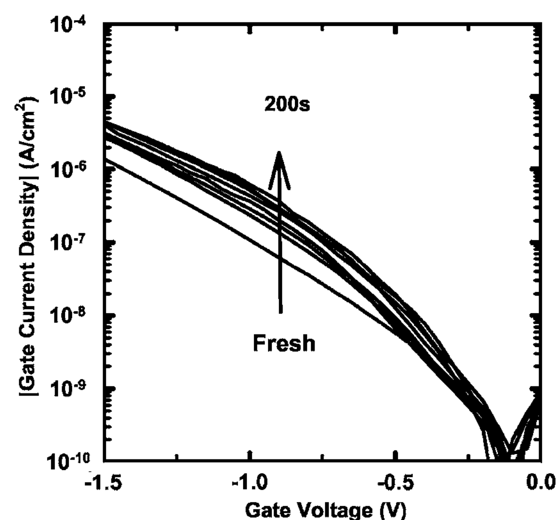

Figure 7. *J-V* characteristics as a function of stress time under constant voltage stress ($V_g = -3.75$ V) for the 700°C PDA-treated HfO_2/SiO_2 gate stacks without LTN.

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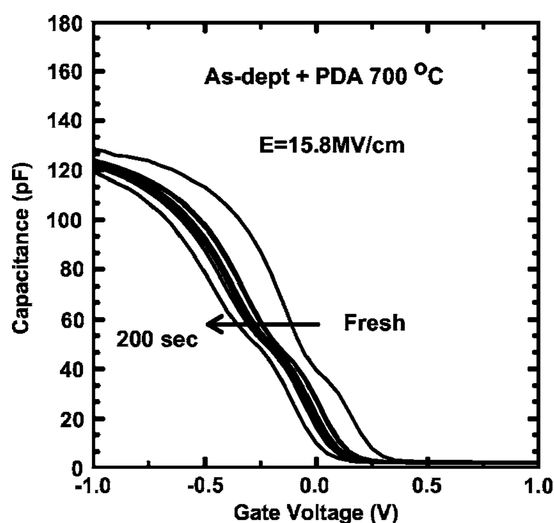

Figure 8. *C-V* curves measured at 100 kHz with stress time as a parameter under constant voltage stress ($V_g = -3.75$ V) for the 700°C PDA-treated HfO_2/SiO_2 gate stacks without LTN.

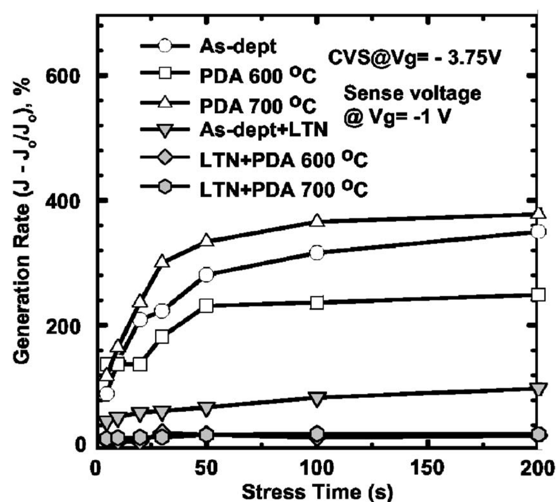

Figure 10. (a) Trap generation rate of the HfO_2/SiO_2 gate stacks with/without LTN under constant voltage stress ($V_g = -3.75$ V).

The Weibull distributions of the dielectric breakdown voltage for the HfO_2/SiO_2 gate stacks are shown in Fig. 6. It is evident that with nitrogen incorporation, the LTN samples exhibit higher breakdown voltages. More importantly, the samples subjected to the combination of LTN and 700°C PDA exhibit the highest breakdown voltage among all splits, while those without LTN display increasingly severe degradation in the breakdown voltage as the PDA temperature increases. Again, we hypothesize that the bond network of the HfO_2 film is strengthened by the nitrogen incorporation during the high-temperature PDA process, similar to the case in SiO_2. The weakness caused by the high-temperature annealing for the samples without LTN echoes the fact that the crystallization of HfO_2 will create more grain boundaries and those boundaries can be easily broken during high field stress.

Figure 7 shows the *J-V* characteristics for the samples subjected to 700°C PDA during constant voltage stress (CVS). The stress voltage was −3.75 V. It is clearly observed that the gate leakage current increases over stress time at the low voltage region. In order to clarify the mechanism responsible for the gate leakage increase after constant voltage stress, the *C-V* curves of a MOS capacitor were measured after different CVS times (Fig. 8). The CVS was periodically interrupted to measure the *J-V* and *C-V* characteristics. One observes that the *C-V* curve gradually shifts toward negative voltage as the stress time progresses. This tendency indicates that hole trapping occurs during constant voltage stress. Figure 9a illustrates the energy band diagram of the gate stack under $V_g = -3.75$ V stress, i.e., gate injection. The parameters, including physical thicknesses, band offsets, and the voltage drops across the individual insulators, were determined based on our TEM analyses and the work function of TiN (~4.8 eV) reported in previous research.[14,15] It can be seen that the probability of hole tunneling from the substrate is much higher than that of electron tunneling from the gate because of the shorter tunnel distance. Therefore, it is reasonable to assume that the leakage current is dominated by the hole injection. For the reason that the hole tunneling current will be impeded by the hole trapping inside the gate stack, the evolution of gate leakage current under CVS will decrease, not increase. Therefore, we conclude that the trap-assisted hole tunneling mechanism is responsible for the increase in gate leakage current, as shown in Fig. 9b. Certainly, it belongs to the stress-induced-leakage current (SILC) in the high-*k* gate stack. SILC is an important concern in the scaling of the gate oxide thickness because it can decrease DRAM refresh times, degrade EEPROM data retention, and deteriorate MOSFET off-state power dissipation. It is known that the trap generation rate is an index for SILC.[16] Figure 10 shows a comparison of the trap generation rate for different samples under CVS of $V_g = -3.75$ V. Clearly, the LTN can significantly reduce the trap generation rate and, especially, the sample with a higher-temperature PDA of 700°C still exhibits an extremely low trap generation rate.

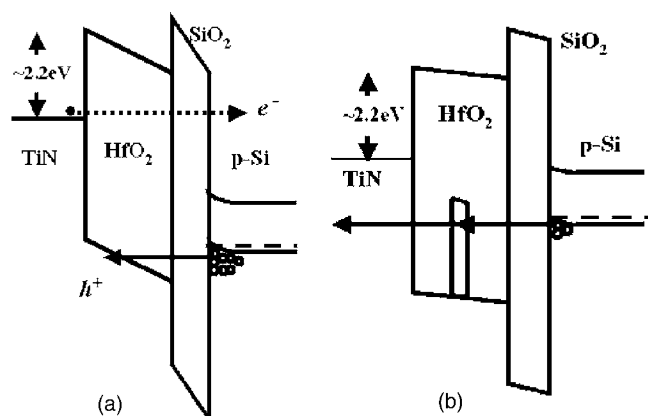

Figure 9. (a) Schematic energy band diagram of the gate stack under $V_g = -3.75$ V stress and (b) trap-assisted hole tunneling mechanism responsible for the increase in gate leakage current.

Conclusion

The effects of postdeposition low-temperature (~400°C) NH_3 treatment on the characteristics of the HfO_2/SiO_2 gate stacks with TiN gate electrode were investigated in this work. Our results indicate that samples subject to the LTN treatment exhibit superior *C-V* characteristics, less frequency dispersion, and lower gate leakage. In addition, the defect density in the bulk and the immunity against trap generations are significantly improved, especially for samples with subsequent 700°C PDA.

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