0.13-μm RF CMOS and Varactors Performance Optimization by Multiple Gate Layouts

Chien-Chih Ho, *Student Member, IEEE*, Chin-Wei Kuo, *Student Member, IEEE*, Yi-Jen Chan, *Senior Member, IEEE*, Wan-Yih Lien, and J.-C. Guo

***Abstract*—0.13-μm radio frequency (RF) CMOS devices with multifinger gate structure have been fabricated by the standard logic process, and the measured effective gate-length is 80 nm. Extensive RF characterization has been done to obtain cutoff frequency (f_T), associated power gain cutoff frequency ($f_{\max}$), minimum noise figure ($NF_{\min}$), output power ($P_{\rm out}$), and power added efficiency (PAE) for RF circuit design and to explore the optimized gate layout in terms of the extracted RF device parameters. Our important finding to be reported in this paper is that an optimized unit finger width (W_F) exists by trade-off among f_T, $f_{\max}$, $NF_{\min}$, $P_{\rm out}$, and PAE. Under fixed total width to achieve the same current drivability (I_{ds}), the smaller W_F and the larger finger number (N_F) leads to higher $f_{\max}$ but lower f_T due to trade-off between gate resistance (R_g) and parasitic gate capacitance. As for $NF_{\min}$ complicated by f_T and R_g, counter-balance between parasitic gate capacitance and R_g leads to nearly constant $NF_{\min}$ w.r.t. various splits of (W_F, N_F). Regarding $P_{\rm out}$ and PAE, W_F of 4 μm and N_F of 18 is the optimized layout parameter, which offers the maximum $P_{\rm out}$ of around 11 dBm and PAE of 30.5% at 5.8 GHz. The performances of accumulation-mode MOS varactors with different gate layout structures are also investigated in this report. Since the same area varactors with different gate layout may result in different parasitic resistance and fringing capacitance, which will affect the capacitance tuning range and the associated Q-factor. The maximum Q-factor is about 59 of the 120 μm^2 gate area varactor, and its tuning range is from 210 fF to 1.64 pF, where the maximum $C_{\max}/C_{\min}$ ratio is about 7.8.**

***Index Terms*—0.13-μm CMOS, $NF_{\min}$, RF power, varactor.**

I. Introduction

BY SCALING down the CMOS gate dimension, it results in an improvement in the radio-frequency (RF) performance in terms of the RF noise and power characteristics [1], [2]. Due to the low-cost and high-integration benefits, where the low-power performance advantage in the baseband is well established, the CMOS technology has recently been recognized as a good candidate to realize the RF front-end circuits in the wireless communications. Recent works concerning the RF performance of CMOS devices have been released [3]–[6]. The performances such as current gain cutoff frequency (f_T), associated power gain cutoff frequency ($f_{\max}$), minimum noise figure ($NF_{\min}$), and transconductance (g_m) have been improved greatly in parallel with a rapid technology evolution. However, by scaling down the CMOS device, the optimum layout of transistors for high frequency and low noise application becomes a critical issue, which is worthwhile for us to pay attention.

The total gate-width of the FET-type device is the key factor to guarantee the amount of delivering RF output power. A multifinger structure with a small gate finger width is the most popular approach to reduce the input gate resistance, which results in a performance improvement as well as RF noise figure reduction. However, by further shrinking the gate finger width (W_F), namely increasing the gate-finger number (N_F), the layouts become the stripe-shape rather than the square-shape. This nonoptimized layout will introduce the additional parasitics from the lossy Si substrates, especially the parasitic capacitances, which will degrade the device microwave performance. In this report, we investigated four different types of CMOS devices with a drawn length of 0.13 μm and varying W_F and N_F to keep the total gate-width constant, including 2 μm $\times$ 36 fingers, 4 μm $\times$ 18 fingers, 6 μm $\times$ 12 fingers and 8 μm $\times$ 9 fingers, respectively, by means of the device RF power and noise performance. By scaling down the CMOS gate dimension together with the advanced low-k and Cu metal technologies, recent published results in terms of RF performance demonstrated an f_T of 155 GHz and an $f_{\max}$ of 60 GHz [7]–[9]. In this work, the optimized gate layout MOSFET fabricated by 0.13-μm Copper logic process (w/o low-k dielectric) which considering the high frequency, power, and noise performance demonstrates the f_T of 104 GHz and $f_{\max}$ of 68 GHz.

Besides the optimum layout transistors of the Si-based RF components, high-quality on-chip voltage-controlled capacitors (varactors) also play an important role in the integrated RF passive devices. Varactors can be used in the LC-tank voltage-controlled oscillators for providing a large tuning range of capacitance. Recently, the accumulation-mode MOS varactors have been proven to be superior to the reverse-biased p–n junction varactors in terms of power consumption, phase noise and tuning range in the voltage-controlled oscillators (VCOs) design [10], [11]. As to the technology scaling down, the thinner used gate oxide results in the capacitance increase. The capacitance tuning range can therefore be enhanced from the MOS varactors. However, the optimum layout of MOS varactors for achieving quality-factor (Q) and capacitance tuning range is worthwhile to be investigated. This report characterizes the performance of four different types MOS varactors with

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TABLE I
MEASURED g_m, f_T, AND $f_{\max}$ OF THE TOTAL DEVICE WIDTH OF 72-μm DEVICES OF THESE FOUR DIFFERENT GATE CONFIGURATION

Width (W_F) × finger (N_F) (μm)	I_{ds} (mA/mm)@ V_{ds}=1.2 V, V_{gs}=1.1 V	g_m (mS/mm)	f_T (GHz)	f_{max} (GHz)
2 × 36	715	911	99	70
4 × 18	719	911	104	68
6 × 12	731	887	107	65
8 × 9	717	889	107	62

different gate finger length (L), width (W), branch numbers (B), and group numbers (G).

II. EXPERIMENTAL MEASUREMENT SETUP

Effective gate-length of 80-nm nMOS devices used in this work were fabricated by using the foundry 0.13-μm CMOS standard logic process with the Cu metal. The draw length for the typical devices on layout (not exactly equal to the mask size due to some pattern enhancement technique) is 0.13 μm, and the exactly physical gate length is 80 nm after through the whole process flow, which was examined by the scanning electron microscope (SEM). The fabricated transistors were first characterized by dc I–V measurements. The S-parameters measurements were carried out up to 40 GHz by using the CASCADE on-wafer probes, an HP8510C network analyzer, and the dummy devices for the open and short calibration to eliminate the probe pads parasitic effects in Si substrates [12]. The RF noise figure and associated gain were obtained by using the ATN-NP5B noise parameter extraction system up to 10 GHz, which covers the most important frequency band for the wireless communication. The device power performance was measured by using the Maury load-pull system. The C–V curves of the MOS varactor were measured by an HP4284, and the Q-factor was extracted from the S-parameters by an HP8510C network analyzer.

III. MOS DEVICE MICROWAVE CHARACTERISTICS

Dc and RF characteristics are listed in Table I for the 0.13-μm RF nMOS with multifinger gate structure of four (W_F, N_F) splits. The dc peak transconductances (g_ms) are in the range of 890–910 mS/mm. The f_T increases from 99 to 107 GHz by increasing the W_F from 2 μm to 8 μm with a corresponding decrease of N_F from 36 to 9, which makes the total gate area constant. However, the $f_{\max}$ demonstrates the opposite trend, namely decreasing from 70 to 62 GHz, corresponding to an increase of W_F and decrease of N_F. To investigate the mechanism responsible for the measured results, which may be related to the layout configurations, we analyzed the device measured S-parameters by extracting their small-signal equivalent circuit model. The parameters extraction method from [13] was adopted in this work. Fig. 1 shows the small-signal equivalent circuit model for the RF CMOS devices, and the extracted components from the S-parameters for the 0.13-μm nMOS with four splits of gate layout are listed in Table II. The initial values of these components were directly obtained from some specific biasing points, such as at gate zero or peak g_m bias. The polycide gate finger is directly connected to the metal one layer by

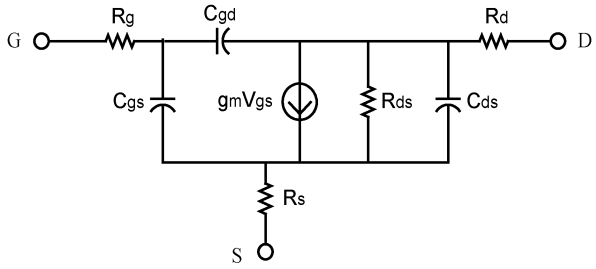

Fig. 1. Small-signal equivalent circuit model of the 0.13-μm gate-length MOSFET.

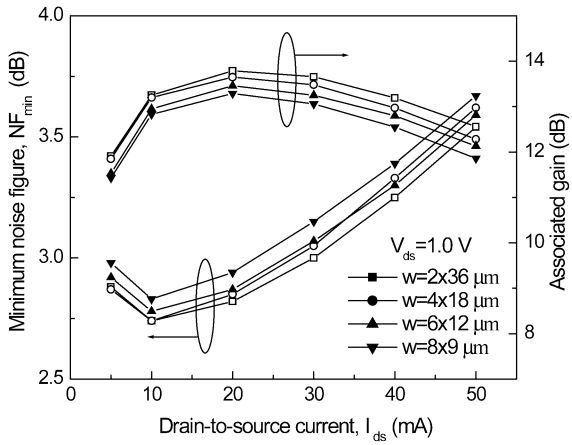

Fig. 2. Measured $NF_{\min}$ and associated gain versus the drain current for these four different gate layout configuration of 0.13-μm CMOS devices at 5.8 GHz.

the contacts on gate pads. Therefore, the extracted R_g from the measured S-parameters contains the resistance due to the gate fingers and pad contacts. However, our multifinger type gate design can significantly reduce the gate associated resistance. By decreasing W_F and increasing N_F, the total gate resistance (R_g) decreases systematically from 9.1 Ω for 8 μm × 9 fingers to 5.2 Ω for 2 μm × 36 fingers. However, in the meanwhile the gate associated parasitic capacitance (C_{gs}, C_{gd}) increases with N_F, which introduces more parasitic gate capacitance associated with a stripe-shaped gate configuration. Since the f_T is proportional to $g_m/2\pi(C_{gs}+C_{gd})$, the higher parasitic capacitance in the 2 μm × 36 gate configuration device results in a lower value of f_T. On the other hand, the $f_{\max}$ is strongly related to the input impedance, dominated by the R_g, and the lower R_g in the 2 μm × 36 device accounts for the higher $f_{\max}$.

Fig. 2 shows the $NF_{\min}$ and the associated gain at 5.8 GHz versus drain current (I_{ds}) for RF nMOS with the mentioned gate layout splits but without the intentional measurement

TABLE II
EXTRACTED SMALL-SIGNAL EQUIVALENT CIRCUIT COMPONENTS OF THESE FOUR DIFFERENT GATE CONFIGURATION DEVICES

Width (W_F) × finger (N_F) (μm)	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)
2 × 36	5.2	5.0	2.3	80	86	30	33
4 × 18	6.0	4.0	2.2	79	80	28	31
6 × 12	6.9	4.1	2.2	80	79	26	31
8 × 9	9.1	4.1	2.4	77	76	25	30

TABLE III
POWER PERFORMANCE OF THE TOTAL DEVICE WIDTH OF 72-μm DEVICES OF THESE FOUR DIFFERENT GATE CONFIGURATION AT 5.8-GHZ OPERATION

Width (W_F) × finger (N_F) (μm)	NF_{min} (dB) @ 10 mA	Gain (dB)	P_{out} (dBm)	Max. efficiency (%)
2 × 36	2.74	12.4	10.5	27
4 × 18	2.74	13.2	10.9	31
6 × 12	2.78	13.3	10.7	29
8 × 9	2.83	12.6	10.4	26

de-embedding. The $NF_{\min}$ can be characterized by the following equation [14]:

$$NF_{\min} = 1 + K \cdot \frac{f}{f_T}\sqrt{g_m\left(R_g + R_s\right)} \propto \sqrt{\frac{R_g + R_s}{g_m}} \quad (1)$$

where R_s is the source series resistance and K is the fitting parameter. The $NF_{\min}$ systematically decreases by reducing the I_{ds}, reaching a minimum value at 10 mA. From the other point of view, a higher channel current in the device causes a higher noise level due to the increase of carrier random fluctuations. The increase of $NF_{\min}$ below 10 mA is mainly associated with the gain reduction near the device threshold region. A slight gain reduction at high current level regime is consistent with the dc g_m gain profiles. As shown in Fig. 2, the device of 2 μm × 36 fingers achieves the lowest $NF_{\min}$ of 2.74 dB and highest associated gain of 13.79 dB, which is due to the lowest $(R_g + R_s)$ resistance.

In brief, by decreasing W_F and increasing N_F, the RF CMOS exhibits better $NF_{\min}$ performance. However, the device RF power performance does not demonstrate the same trend as that of $NF_{\min}$. Fig. 3 and Table III show the output power performance of the RF nMOS with total width of 72 μm at 5.8 GHz. The devices were matched to obtain the maximum output power by the source and load tuners. The power performance is dependent not only on the gate resistance (R_g), but also the parasitic capacitances quite significantly. As shown in Fig. 3, the 4 μm × 18 fingers device reveals the highest output power (P_{out}), power gain and power added efficiency (PAE). Although the 2 μm × 36 finger device achieves the lowest parasitic resistance contributing to the lowest $NF_{\min}$, the 4 μm× 18 finger device demonstrates the best power performance, where P_{out} is 10.9 dBm with a gain of 13.2 dB and PAE of 30.5% at 5.8 GHz. Again, gate associated parasitic capacitance is considered as the major factor to be traded off with R_g, and the gate layout of the multifinger structure is a tradeoff between RF noise and power performance. The stripe-shaped layout device achieves the best noise performance and the $f_{\max}$; however, it also introduces more parasitics which degrades the RF power characteristics. Therefore, for the RF CMOS with a total gate width of 72 μm in this study, the optimized gate layout in terms of f_T, $f_{\max}$, $NF_{\min}$, P_{out}, and PAE is 4 μm × 18 fingers.

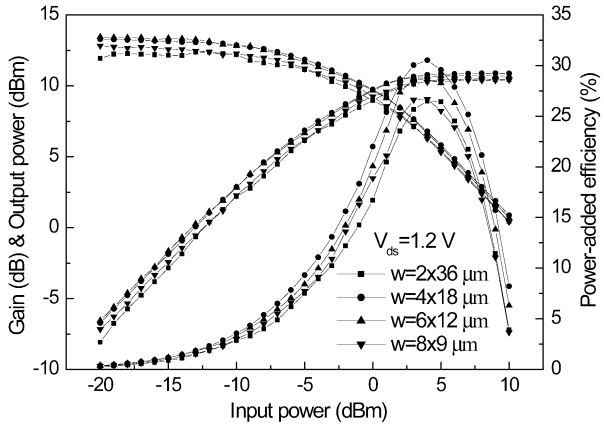

Fig. 3. Measured RF output power performance versus the input power for these four different gate layout configuration of 0.13-μm CMOS devices at 5.8 GHz.

IV. MOS VARACTOR MICROWAVE CHARACTERISTICS

Fig. 4 shows the layout of the feather type MOS varactor. The goal in our MOS varactor design is to enlarge the capacitance density within a limited area, i.e., enhancing the $C_{\max}$ value. Therefore, we use the feather type MOS varactor design instead of the traditional finger type MOS varactor design. The n^+/n-well MOS varactors with a multifinger and feather structure gate were fabricated by using the 0.13-μm CMOS technologies. The terminals of the source, drain, and bulk were shorted together. By biasing a positive voltage between the gate and the well, the device is accumulated, and the capacitance equals the gate oxide capacitance. By supplying a reversed bias, the device channel is depleted and the series capacitance decreased. The ratio of the $C_{\max}/C_{\min}$ defines the varactor tuning range. The $C_{\text{ox}}(C_{\max})$ increases as the oxide thickness scales down, where the scaled technology provides a wider tuning range. To achieve the optimum layout in terms of the Q-factor and capacitance ratio, we varied the gate finger length, width, group numbers and branch numbers to keep the total gate area constant of 120 μm^2, including 0.25 μm × 1 μm × 120 × 4 (type

TABLE IV
MEASURED CAPACITANCE, Q-FACTOR, AND PARASITIC SERIES RESISTANCE OF THE DIFFERENT GATE LAYOUT STRUCTURE MOS VARACTORS WITH A GATE BIAS AT -1.0 V

Area (L × W × B × G)	Capacitance tuning range (pF)	C_{max}/C_{min} ratio	Parasitic resistance (ohm) @ -1.0 V	Q-factor @ -1.0 V
Type A (0.25 × 1 × 120 × 4)	0.38~1.53	4.0	7.5	53
Type B (0.5 × 1 × 60 × 4)	0.28~1.57	5.6	6.8	54
Type C (0.5 × 2 × 60 × 2)	0.26~1.59	6.1	6.4	55
Type D (1 × 2 × 30 × 2)	0.21~1.64	7.8	5.7	59

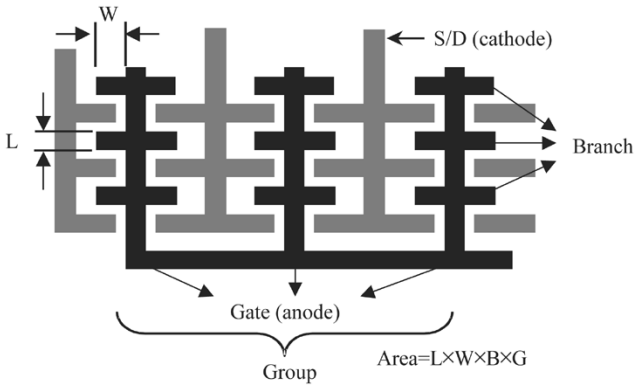

Fig. 4. Layout of the MOS varactor with the multifinger structure gate.

A), 0.5 μm × 1 μm × 60 × 4 (type B), 0.5 μm × 2 μm × 60 × 2 (type C) and 1 μm × 2 μm × 30 × 2 (type D), respectively. The range of gate bias voltage was from -1.0 V to 1.0 V. Since the same area varactors with different layout (L, W, G, B) have different fringing capacitance and parasitic resistance, the capacitance and Q-factor will be different for the same gate area varactors with different layout structures. Fig. 5 shows the measured capacitances and Q-factors of these four types of varactors at 2.4 GHz. As shown in Table IV, the capacitance tuning range of type A structure with higher group (G) and branch (B) numbers is the lowest among other types, and the maximum Q-factor is 53. From the parameter-extraction method in [15], the main series parasitic resistance and capacitance values of the varactor are shown in Table IV. The type A varactor, due to the $L = 0.25$ μm and the stripe-shaped layout configuration, introduces more parasitic series resistance and the fringing capacitance, respectively. It therefore results in a low Q-factor and a low capacitance tuning range. As to the type D varactor, where the L is 1 μm and the layout is more square-shaped, the Q-factor and the capacitance tuning range can be enhanced simultaneously. The maximum Q-factor of 59 with a tuning range ratio of 7.8 is achieved in the type-D varactor.

This 0.13-μm feather type MOS varactor, shown in Fig. 4, has a higher parasitic resistance, ranging between 5.7 to 7.5 Ω, which limits the Q-values even though using this advanced device technology. The Q-values in the $C_{\max}$ region are generally lower than the finger type varactors, which is due to the enhanced capacitance and a higher parasitic resistance, i.e., $Q \sim (RC)^{-1}$. The change of parasitic resistance between $C_{\max}$ and $C_{\min}$ is small. The layout consideration in varactor design is similar to the conclusions obtained from the nMOS investigation, i.e., stripe-shaped configuration introducing more parasitics.

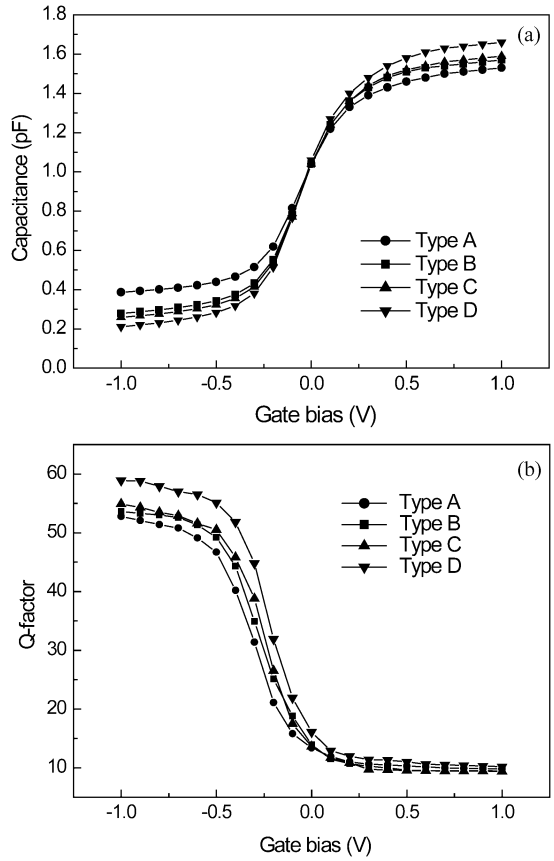

Fig. 5. (a) Measured capacitance of the MOS varactors with different gate layout structure. (b) Measured Q-factor of the MOS varactors with different gate layout structure at 2.4 GHz.

V. CONCLUSIONS

In this work, high-frequency power and noise characterization has been done on 0.13-μm nMOS to investigate the optimized gate layout in terms of the extracted RF performance parameters f_T, $f_{\max}$, $NF_{\min}$, P_{out}, and PAE. The tradeoff among all the parameters is strongly related with the associated parasitic gate resistance (R_g) and capacitances (C_{gs}, C_{gd}). For this study, the gate layout of 4 μm × 18 fingers is identified as the optimum design in terms of f_T, $f_{\max}$ and $NF_{\min}$, P_{out}, PAE at 5.8 GHz. In the varactor gate layout structure design, for the purpose of providing larger capacitance tuning range and Q-factor, the gate layout should consider more on the parasitic resistance and the capacitance, where the stripe-shaped layout is not suitable in this regard.

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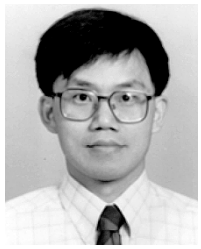

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