$CoTiO_3$ High-κ Dielectrics on HSG for DRAM Applications

Tien-Sheng Chao, *Senior Member, IEEE*, Wei-Ming Ku, Hong-Chin Lin, Dolf Landheer, Yu-Yang Wang, and Yukihiro Mori

***Abstract*—In this paper, a new high-κ dielectric $CoTiO_3$ has been investigated for the first time on hemispherical grained (HSG) poly-Si dynamic random access memories capacitors. Three types of HSG were prepared. We found that capacitors with maximum grain size and the highest density exhibit twice the capacitance of the others. The dielectric constant for $CoTiO_3$ was estimated to be larger than 50. Leakage current measurements performed at temperatures as high as 100 °C show that this dielectric is stable. The polarity dependence is found to be due to the different barrier heights with the nitride barrier. A leakage mechanism is proposed for this polarity dependence.**

***Index Terms*—Dynamic random access memories (DRAM), high-κ, nitride.**

I. Introduction

DYNAMIC random access memories (DRAM) are the most widely manufactured and used semiconductor memories. To achieve high density, the DRAM memory cell structure is changing from a planar cell to a stack or trench type cell. The challenges for cell scaling are how to minimize feature size to obtain high density and how to reduce the equivalent oxide thickness (EOT) to maintain the minimum charge in the capacitor [1]. To scale the EOT, dielectric materials that have a high dielectric constant (k) are needed. Metal insulator semiconductor (MIS) capacitors using Al_2O_3 or $Ta_2O_5 (k \sim 10–25)$ have been adopted for the 130-nm node and below [2]–[4]. To maintain sufficient storage capacitance, a higher κ dielectric is required. In addition to the transition to higher κ materials and reduction of dielectric thickness, another technique used to increase the storage capacitance is to roughen or texture the poly-Si to increase the electrode surface area [5]–[8]. The hemispherical grains (HSGs) selectively deposited on the poly-Si electrode can result in a factor of 1.8 times or larger capacitance [9], [10]. In this paper, a new high-κ dielectric, $CoTiO_3$, is deposited for the first time on the HSG for DRAM cell capacitors.

Manuscript received May 5, 2004; revised October 26, 2004. This work was supported by the National Science Council, Taiwan, R.O.C., under Contract NSC-92-2215-E009-070. The review of this paper was arranged by Editor V. R. Rao.

T.-S. Chao is with the Department of Electrophysics, National Nano Device Laboratories, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: tschao@mail.nctu.edu.tw).

W.-M. Ku and H.-C. Lin are with the Department of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan, R.O.C.

D. Landheer is with the Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, ON K1A 0R6, Canada.

Y.-Y. Wang is with the ASM Taiwan, Hsinchu 300, Taiwan, R.O.C.

Y. Mori is with the ASM Process Laboratory, Nagaoka, Japan.

Digital Object Identifier 10.1109/TED.2004.839880

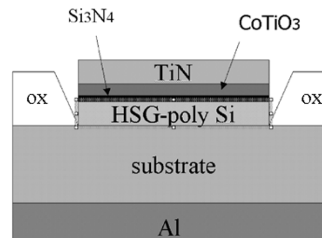

Fig. 1. Cross section of the $TiN–CoTiO_3/Si_3N_4$-Si structure.

We found that by using high density with the optimal grain condition, the capacitance can be doubled and the estimated κ value could be larger than 50, very promising for the 90-nm node and beyond.

II. Experiments

Fig. 1 shows the cross section of the capacitor. Capacitors were fabricated on a n-type 150 mm wafer. After the growth of a 500-nm thick field oxide, the active region was defined and etched. Wafers underwent cleaning and then a 100-nm poly-Si film was deposited. The HSGs were deposited by ASM. The first step in this process involved transforming a-Si films into HSG for the bottom electrodes. A-Si films were deposited by a low-pressure chemical vapor deposition (LPCVD) process at 525 °C. Doped a-Si films were deposited from silane and phosphine source gases at 510 °C. The HSG transformation of the a-Si layer was formed in an ASM A600 UHVCVD reactor. The seeding temperature and pressure were 560 °C and 5×10^{-5} torr, respectively. There are three types of HSG; maximum-grain and high-density (MGHD), small-grain and high-density (SGHD), and small-grain and low density (SGLD). After doping the n^+-poly-Si electrode, wafers were put into a LPCVD furnace to grow an ultrathin nitride $\sim$1.0 nm thick, using NH_3 at 800 °C for 1 h. The purpose of this nitride film is to prevent the oxidation of the poly-Si in the following metal oxidation process and thermal nitridation using NH_3 has become popular for the production of ultrathin nitride films. For safety, the thermal nitridation is usually performed in a LPCVD system. The growth of native oxide is inevitable during loading into the LPCVD furnace. To reduce this native oxide, the wafer was cleaned with an HF-dip. The Co–Ti (5/5 nm) film was deposited on the wafer by sputtering. The base pressure was 7×10^{-3} torr, and the sputtering energy was set at 0.5 keV, using a flow of 120 sccm of Ar, resulting in a deposition rate of 5 and 9 Å for Ti and Co, respectively. Then, wafers were oxidized in the furnace using

0018-9383/04$20.00 © 2004 IEEE

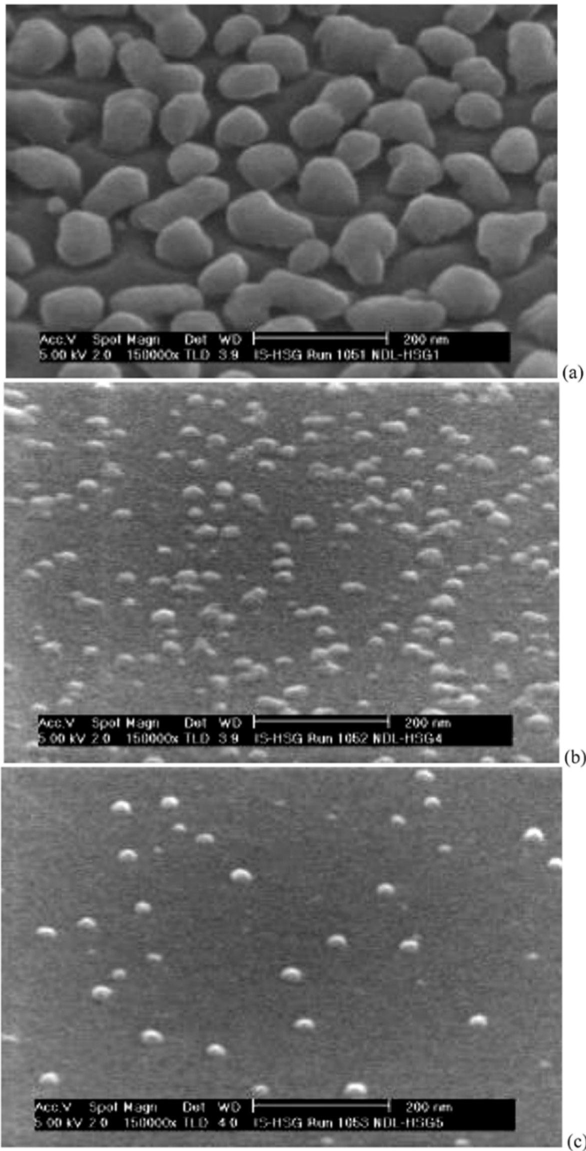

Fig. 2. SEM images for (a) MGHD, (b) SGHD, and (c) SMLD.

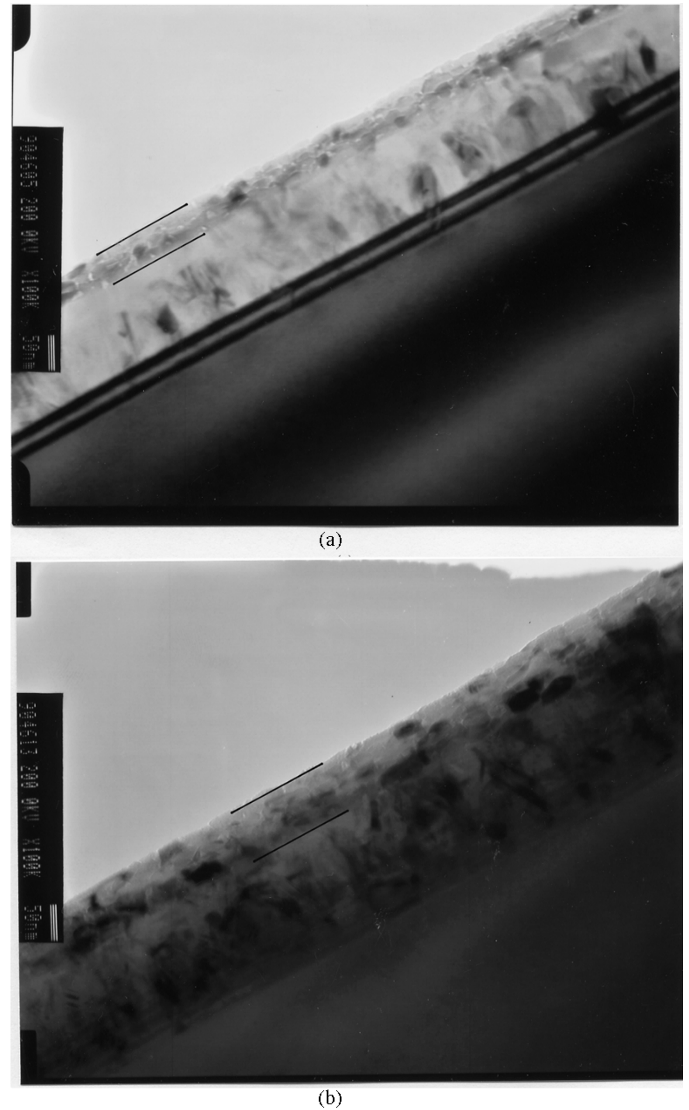

Fig. 3. TEM picture (× 100 k) for samples oxidized (a) at 700 °C and (b) 800 °C. The bar is 50 nm.

O_2/N_2 (5000/5000-cc) at 700 °C and 800 °C for 25 and 10 min, respectively. After that, 150 nm of TiN was sputtered for the top electrode. Scanning electron microscopy (SEM) was used to determine the grain size and density after HSG deposition. Transmission electron microscopy (TEM) was used to get the physical thickness for all samples. Low angle X-ray diffraction (XRD) was used to find the orientation of crystallization of thin films oxidized at elevated temperatures. Finally, the electrical properties of the MIS capacitors were measured at 25, 50, and 100 °C to test their reliability.

III. Result and Discussions

Fig. 2 show the SEM images (150 k times) for MGHD, SGHD, and SGLD samples, respectively. It is clear that the grain size and density were maximized for the MGHD sample. The reflectance measured by ellipsometer was 6.3%, 46.5%, and 48.5% for MGHD, SGHD, and SGLD, respectively. For the small grain samples, reflectance decreases as grain density is increased. But the reflectance of MGHD decreases significantly to 6.3% due to both its rugged surface and high grain density. It was found that MGHD samples exhibited the largest root-mean-square roughness (6.9 nm) after oxidation. The roughness of SGHD (1.7 nm) and SGLD (1.6 nm) layers was nearly the same after oxidation. The resultant thickness of the $CoTiO_3$ film was determined by the TEM technique as shown in Fig. 3. The thickness, including the bottom nitride, was 46.8 nm and 63.8 nm for samples oxidized at 700 °C and 800 °C, respectively. Fig. 4 shows the XRD result after the oxidation of MGHD. The dominant orientation of this $CoTiO_3$ film is (422) for both 700 °C and 800 °C. No significant difference was found for the SGHD and SGLD samples. This implies that the crystallization of $CoTiO_3$ is independent of the bottom HSG electrodes.

The capacitances for these three samples are shown in Fig. 5. Three different areas were used for comparison;1×10^{-4},

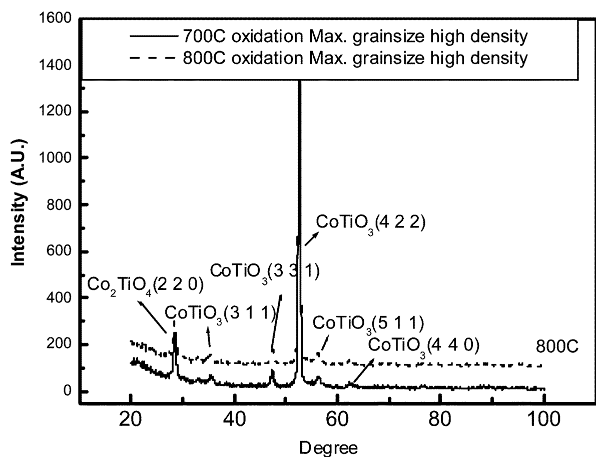

Fig. 4. XRD (2θ) analysis showing that (422) is the dominated orientation.

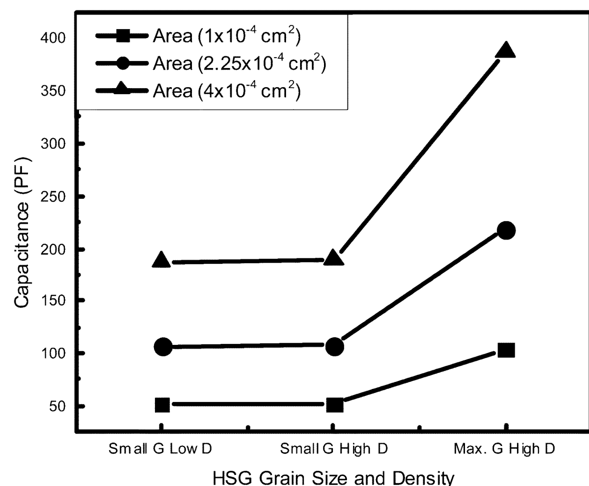

Fig. 5. Capacitance of samples with different grain patterns and different capacitor areas.

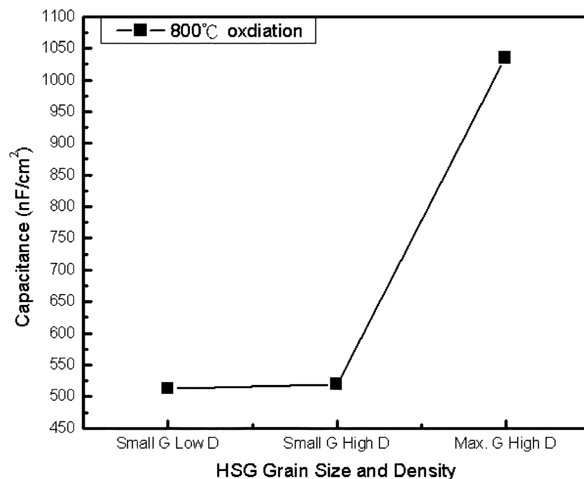

Fig. 6. Capacitance/cm^2 for samples of MGHD, SGHD, and SGLD.

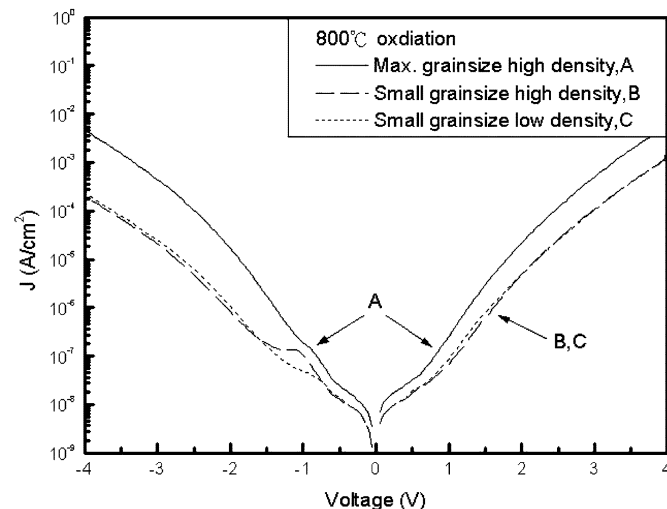

Fig. 7. J–V curves for samples oxidized at 800 °C.

2.25×10^{-4}, and 4×10^{-4} cm^{-2}. For a given area, there is no increase for SGHD compared to SGLD. This implies that the process for small grain and high density does not significantly increase area at all, resulting in no increase in capacitance. However, the MGHD can significantly increase the capacitance. For a given area, the increased capacitance is almost twice the value for MGHD when compared to SGHD and SGLD. Fig. 6 shows the capacitance normalized by the projected area. This capacitance per cm^2 increases significantly for the MGHD sample. The thickness obtained from the TEM measurements for the control sample without the HSG process and the capacitance obtained from the C–V measurements of SGLD samples were used to deduce the accurate dielectric constant of $CoTiO_3$. The resultant dielectric constants for the SGLD samples after oxidation at 700° and 800 °C are about 30, and 35, respectively. Eliminating the thickness of the interfacial oxynitride, the dielectric constant for $CoTiO_3$ can be larger than 50. The increase of the κ-value at high temperature is due to the full oxidation and crystallization of the Co and Ti metal films at high temperature [11].

The current–voltage (I–V) characteristics of three samples with different types of grain sizes and densities are shown in Fig. 7. The current of the MGHD sample exhibits larger leakage current than the others due to an increased effective area. As mentioned before, the effective area is almost the same for small grain size with low density or high density; therefore, the leakage current is almost the same for these two samples. Since the results for samples oxidized at 700 °C are similar to those for samples oxidized at 800 °C, the 700 °C results are not shown. However, it can be seen that the breakdown voltage at positive bias for all samples is smaller than that at negative bias. This is due to the rough interface of the HSG since electrons are injected from the bottom HSG electrode under positive bias. This asymmetric phenomenon is frequently found for the tunneling current of inter-poly oxides in EEPROM devices [12], [13]; i.e., the roughness of the floating gate decreases breakdown voltage and also increases the tunneling current for positive bias on the control gate (when electrons tunnel from the floating gate to the control gate). The current–density voltage (J–V) characteristics of SGLD measured at different temperatures from 25 °C to 100 °C are shown in Fig. 8(a).

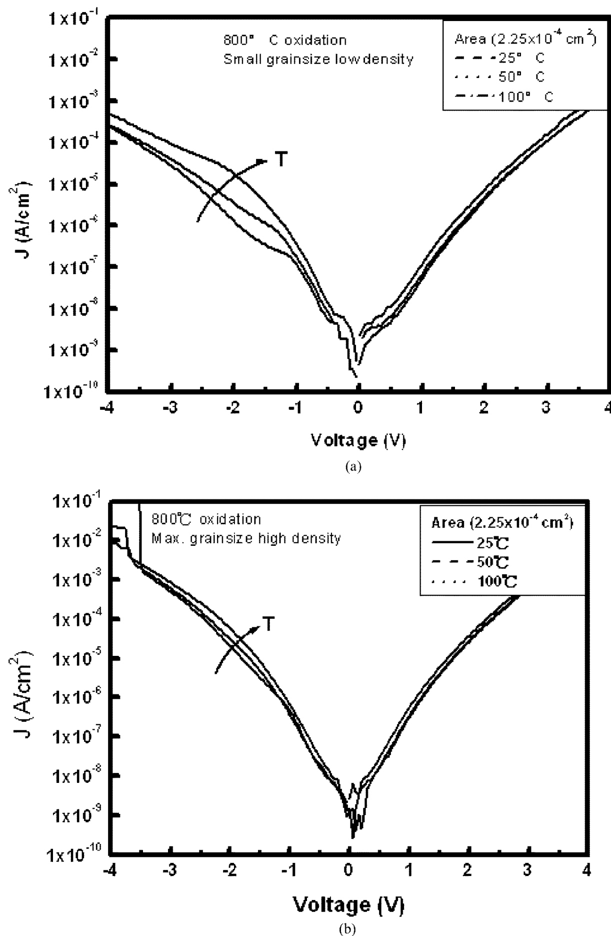

Fig. 8. J–V curves for 800 °C sample measured at 25–100 °C (a) SGLD and (b) MGHD.

It can be seen that under positive bias, no significant leakage occurs, but an increase of current was found for negative bias when the temperature was increased from 25 °C to 100 °C. This phenomenon is also found for all samples of SGHD and SGLD at 700 °C (not shown). As shown in Fig. 1, the sample has an oxynitride on the n^+-poly-Si, followed by the $CoTiO_3$ high-κ dielectric, and the top gate is TiN metal. Hence, it is clear that there exist different barrier heights for the bottom n^+-poly-Si electrode and the top TiN electrode, which causes different tunneling mechanisms. The J–V curves for MGHD samples are shown in Fig. 8(b). Due to significant roughness at the top interface between TiN and $CoTiO_3$, the tunneling current dominates [12], [13]. Hence, the current density at negative bias shows less dependence on temperature compared to the curves in Fig. 8(a). In Fig. 9, a proposed tunneling mechanism for this for TiN–$CoTiO_3/Si_3N_4/n^+$ HSG-poly-Si system is shown. Under positive bias, electrons directly tunnel from the bottom poly-Si gate to the $CoTiO_3$ layer through the ultrathin oxynitride. Since direct tunneling is independent of temperature, there is no significant increase when samples are subjected to positive bias at elevated temperature to 100 °C. On the other hand, under negative bias, electrons do not easily tunnel directly through the thick $CoTiO_3$ film like they do from

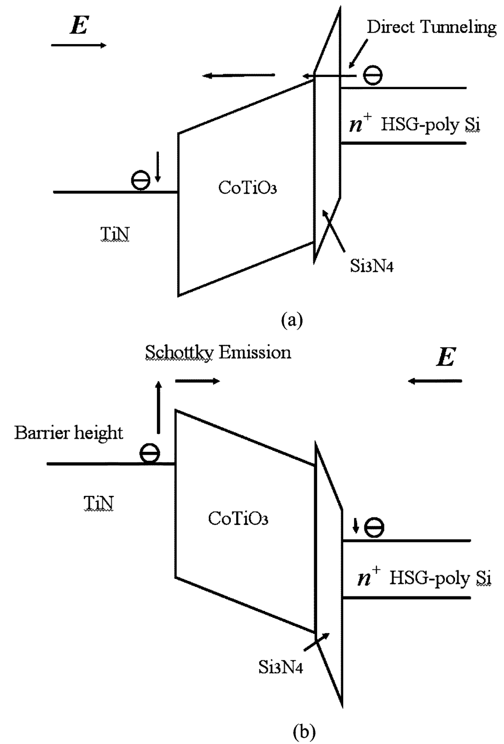

Fig. 9. Tunneling mechanism under (a) positive and (b) negative bias.

the n^+-poly-Si gate. Hence, Schottky emission is dominate at the TiN–$CoTiO_3$ interface, resulting in a change in leakage current with increasing temperature.

IV. Conclusion

We have developed a new high-κ dielectric, $CoTiO_3$ on HSG for DRAM, with a κ value larger than 50. The resultant electrical properties show that this dielectric has stable leakage currents under positive bias when an ultra thin nitride film is used. This system appears very promising for DRAM applications.

References

[1] (2001) International Technology Roadmap for Semiconductors, San Jose, CA. [Online]. Available: http://public.itrs.net/

[2] A. Tsuzumitani, Y. Okuno, J. Shibata, T. Shimizu, K. Yamamoto, and Y. Mori, "Extendibility of Ta_2O_5 metal–insulator–metal capacitor using Ru electrode," *Jpn J. Appl. Phys.*, pt. 1, vol. 39, no. 4B, pp. 2073–2077, 2000.

[3] Q. Lu, D. Park, A. Kalnitsky, C. Chang, C. C. Cheng, S. P. Tay, T. J. King, and C. M. Hu, "Leakage current comparison between ultrathin Ta_2O_5 films and conventional gate dielectrics," *IEEE Electron Device Lett.*, vol. 19, pp. 341–342, Mar. 1998.

[4] J. W. Lee, K. M. Kim, H. S. Song, K. C. Jeong, J. M. Lee, and J. S. Roh, "The property of Ta_2O_5 on chemical vapor deposited Ru film fabricated using tris(2, 4-octanedionato) ruthenium for application to dynamic random access memory capacitor," *Jpn J. Appl. Phys.*, pt. 1, vol. 40, no. 9A, pp. 5201–5205, 2001.

[5] A. Banerjee, R. L. Wise, D. L. Plumton, M. Bevan, M. F. Pas, D. L. Crenshaw, S. Aoyama, and M. M. Mansoori, "Fabrication and performance of selective HSG storage cells for 256 Mb and 1 Gb DRAM applications," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 584–592, Mar. 2000.

[6] D. Ha, D. Shin, G. H. Koh, J. Lee, S. Lee, Y. S. Ahn, H. Jeong, T. Chung, and K. Kim, "A cost effective embedded DRAM integration for high density memory and high performance logic using 0.15 μm technology node and beyond," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1499–1506, Jul. 2000.

[7] A. Banerjee, R. L. Wise, D. L. Plumton, M. Bevan, M. F. Pas, D. L. Crenshaw, S. Aoyama, and M. M. Mansoori, "Fabrication and performance of selective HSG storage cells for 256 Mb and 1 Gb DRAM applications," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 584–592, Mar. 2000.

[8] H. Watanabe, T. Tatsumi, T. Ikarashi, A. Sakai, N. Aoto, and T. Kikkawa, "An advanced technique for fabricating hemispherical-grained (HSG) silicon storage electrodes," *IEEE Trans. Electron Devices*, vol. 42, no. 2, pp. 295–300, Feb. 1995.

[9] M. Sakao, N. Kasai, T. Ishijima, E. Ikawa, and H. Watanabe, "A capacitor-over-bit-line (COB) cell with a hemispherical-grain storage node for 64 Mb DRAM's," in *IEDM Tech. Dig.*, Dec. 1990, pp. 655–655.

[10] H. Watanabe, T. Tatsumi, S. Ohnishi, T. Hamada, I. Honma, and Kikkawa, "A new cylindrical capacitor using hemispherical grained Si (HSG-Su) for 256 Mb DRAM's," in *IEDM Tech. Dig.*, Dec. 1992, pp. 259–259.

[11] T. M. Pan, T. F. Lei, and T. S. Chao, "Comparison of ultrathin $CoTiO_3$ and $NiTiO_3$ high-κ gate dielectrics," *J. Appl. Phys.*, vol. 89, pp. 3447–3452, Mar. 2001.

[12] T. F. Lei, J. Y. Cheng, S. Y. Shiau, T. S. Chao, and C. S. Lai, "Characterization of polysilicon oxides thermally grown and deposited on the polished polysilicon films," *IEEE Trans. Electron Devices*, vol. 45, pp. 912–917, Apr. 1998.

[13] J. H. Chen, T. F. Lei, J. H. Chen, and T. S. Chao, "Characteristics of TEOS polysilicon oxides: Improvement by CMP and high temperature RTA N2/N2o annealing," *J. Electrochem. Soc.*, vol. 147, pp. 4282–4288, Nov. 2000.

Tien-Sheng Chao (SM'00) was born in Penghu, Taiwan, R.O.C. in 1963. He received the Ph.D. degree in electronics engineering from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1992.

He joined the National Nano Device Laboratories, NCTU, as an Associate Researcher in July 1992, and became a Researcher in 1996. He was engaged in developing the thin dielectrics preparations, cleaning processes, and CMOS devices fabrication. He joined the Department of Electrophysics in 2001. His current research interests are in the areas of new high-κ dielectrics for MOS technology, and SOI devices.

Wei-Ming Ku was born in Taipei, Taiwan, R.O.C. on May 5, 1978. He received the B.S. and M.S. degrees in electrical engineering from the National Chung-Hsing University, Taichung, Taiwan, in 2000 and 2002, respectively.

In 2003 he joined the Department of Electrical Engineering. Since then he has been engaged in the research and development of nonvolatile memories.

Hong-Chin Lin, photograph and biography not available at the time of publication.

Dolf Landheer received the Ph.D. in molecular and solid-state physics from the University of Toronto, Toronto ON, Canada, in 1974.

After a postdoctoral fellowship at Imperial College, London, U.K., he worked on electrographic imaging at the Xerox Research Centre, Canada, and then at Delphax Printing Systems, Canada. In 1983, he joined the Institute for Microstructural Sciences, National Research Council of Canada, (NRC-IMS), Ottawa, ON, where he is a Principal Research Officer and Co-ordinator of the project on advanced dielectrics. His current research interests are in the areas of new high-κ dielectrics for MOS technology, insulators for III-V semiconductors, thermal and plasma-enhanced chemical vapor deposition, and chemical and physical characterization of electronic materials. He has published over 170 papers in refereed journals and conference proceedings.

Dr. Landheer is on the committee of the Dielectric Science and Technology Division of The Electrochemical Society, has served on many organizing committees for symposia on silicon oxynitrides and high-κ dielectrics for the MRS and ECS, and is the current Co-chair of the Canadian Semiconductor Technology Conference.

Yu-Yang Wang, photograph and biography not available at the time of publication.

Yukihiro Mori, photograph and biography not available at the time of publication.