HfO_2 MIS Capacitor with Copper Gate Electrode

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***Abstract*—Metal–insulator–semiconductor capacitors were fabricated using atomic vapor deposition HfO_2 dielectric with sputtered copper (Cu) and aluminum (Al) gate electrodes. The counterparts with SiO_2 dielectric were also fabricated for comparison. Bias-temperature stress and charge-to-breakdown (Q_{BD}) test were conducted to examine the stability and reliability of these capacitors. In contrast with the high Cu drift rate in an SiO_2 dielectric, Cu in contact with HfO_2 seems to be very stable. The HfO_2 capacitors with a Cu-gate also depict higher capacitance without showing any reliability degradation, compared to the Al-gate counterparts. These results indicate that HfO_2 with its considerably high density of 9.68 g/cm^3 is acting as a good barrier to Cu diffusion, and it thus appears feasible to integrate Cu metal with the post-gate-dielectric ultralarge-scale integration manufacturing processes.**

***Index Terms*—Bias-temperature stress, copper-gate (Cu-gate) electrode, hafnium dioxide (HfO).**

I. Introduction

WHEN the gate length of MOSFETs is scaled down to a 0.1-μm regime with the corresponding gate oxide thickness thinner than 3 nm, some major problems arise in realizing high-performance ultralarge-scale integration (ULSI) circuits. Specifically, device performance and reliability can be seriously degraded by the intolerably high direct-tunneling leakage current, increased gate resistance, worsened polysilicon gate depletion, and boron penetration [1], [2]. To alleviate these problems, a high dielectric constant (high-κ) gate insulator and metal gate have been proposed to meet the stringent performance requirement [3], [4]. Various high-κ dielectric materials, such as Al_2O_3, Ta_2O_5, HfO_2, and ZrO_2, have been extensively studied [4]–[8]. Among these dielectrics, HfO_2 is very promising for the next-generation gate dielectric of MOSFETs, because of its high dielectric constant, excellent thermal stability, and large band gap, etc. [9], [10].

Recently, Cu has successfully replaced the conventional aluminum alloys as the interconnect metal in the advanced ULSI manufacturing, due to its superior conductivity and better electromigration resistance. Despite its success as the metal interconnect of choice, Cu has still not gained acceptance as the gate electrode of the transistor because the positively charged Cu ions are known to drift very rapidly in thermal oxide under the influence of electric field, and can cause severe reliability degradation in oxide [11].

For the high-κ dielectrics, replacing the conventional polysilicon gate electrode with metal gate has been proposed because of the interface instability between the high-κ dielectrics and polysilicon gate [10], [12]–[14]. However, Cu has never been under consideration, to the best of our knowledge, mainly because of the concern of the rapid Cu ion drift in the dielectric as mentioned above. In this letter, Cu was used for the first time as the metal gate electrode directly on top of a high-κ dielectric, i.e., HfO_2. Based on the results from the bias-temperature stress (BTS) and charge-to-breakdown (Q_{BD}) measurement, the HfO_2-based Cu-gate capacitors show not only enhanced capacitance but also no noticeable reliability degradation compared to Al-gate counterparts. Our results strongly suggest the feasibility of a full Cu process from the gate electrode to the back-end-of-line (BEOL) in future ULSI fabrication.

II. Experimental

Standard 6-in (100) p-type Si wafers, with resistivity of 15–25 Ω-cm, were used in this study. Following a standard RCA cleaning process, a layer of 10-nm-thick HfO_2 using tetrakis diethylamido hafnium precursor was deposited by atomic vapor deposition (AVD) on an AIXTRON Tricent system at a substrate temperature of 400 °C in oxygen ambient. Wafers were subsequently split into two groups. We sputtered 500-nm-thick Cu through a metal mask as the gate electrode for one group, with 500-nm-thick Al for the control group. Finally, all wafers received a 500-nm-thick Al deposition on the wafer backside. The device area is 1.7×10^{-4} cm^2. It is worth noting that control wafers with 10-nm-thick SiO_2 dielectric were also fabricated in this study for comparison. The current–voltage characteristics were measured using a Keithley Model 4200-SCS semiconductor characterization system, and the capacitance was measured using an Agilent 4284A precision LCR meter at a frequency of 100 kHz. Constant current stress (CCS) was conducted for evaluating reliability. In order to investigate the thermal stability of HfO_2 film with Cu electrode, an effective electric field of +1 MV/cm at elevated temperatures ranging from 100 °C to 200 °C was applied to the gate stacks for BTS testing.

III. Results and Discussions

Fig. 1(a) displays typical capacitance–voltage $(C–V)$ characteristics of Cu–SiO_2-Si and Al–SiO_2-Si capacitors, both before and after BTS test, at 150 °C for 1000 s. The applied

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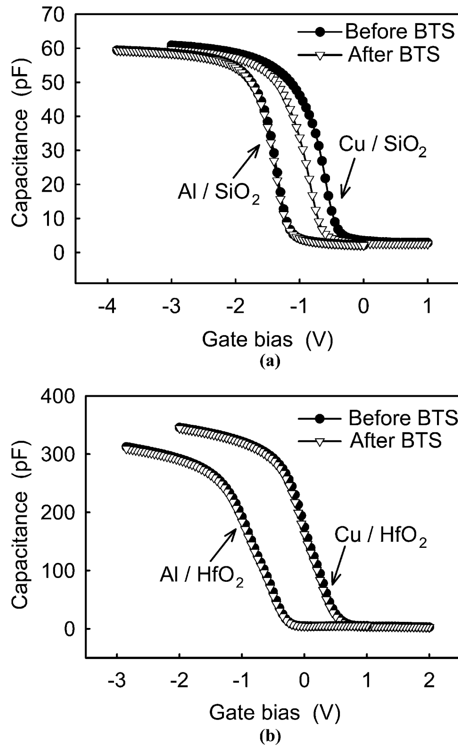


Fig. 1. C–V curves of (a) Cu–SiO_2–Si and Al–SiO_2–Si capacitors and (b) Cu–HfO_2–Si and Al–HfO_2–Si capacitors before and after BTS at 150 °C for 1000 s. The applied field was +1 MV/cm.

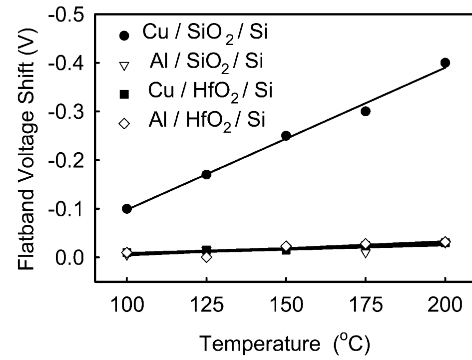
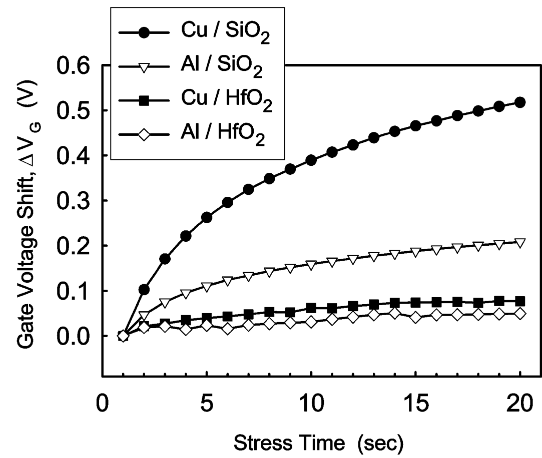


Fig. 2. V_{FB} shifts of Cu–SiO_2–Si, Al–SiO_2–Si, Cu–HfO_2–Si, and Al–HfO_2–Si capacitors after BTS test at +1 MV/cm for 1000 s. The temperatures were varied from 100 °C to 200 °C.



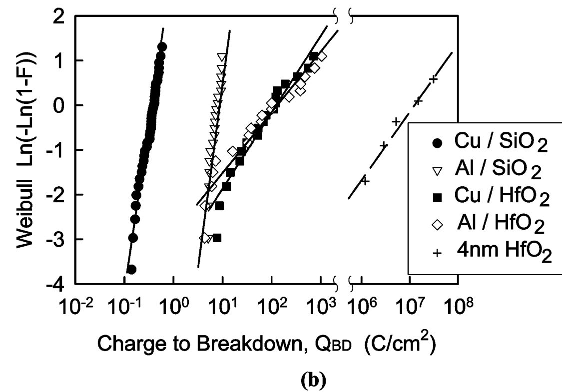


Fig. 3. (a) Gate voltage variation of SiO_2 and HfO_2 capacitors with Cu and Al gate electrodes subjected to CCS as a function of time; (b) cumulative Q_{BD} plots of Cu–HfO_2–Si, Al–HfO_2–Si, Cu–SiO_2–Si, and Al–SiO_2–Si capacitors.

field was +1 MV/cm. A significant negative flatband voltage (V_{FB}) shift of about -0.4 V is observed for the Cu–SiO_2–Si capacitor, indicating that positively bulk charges (i.e., Cu ions) are introduced into the dielectric [15]. In contrast, only negligible V_{FB} shift is found for the Al–SiO_2–Si capacitors after BTS test. It is well known that Al is quite stable in contact with SiO_2. This is because a very thin self-limiting Al_2O_3 layer is formed between the Al electrode and SiO_2, and acts as a good diffusion barrier for further element diffusion and/or reaction [16]. Fig. 1(b) exhibits the C–V characteristics of Cu–HfO_2–Si and Al–HfO_2–Si capacitors before and after BTS test at +1 MV/cm, 150 °C for 1000 s. Quite amazingly, there is essentially no V_{FB} shift observed after BTS. Although a slightly larger V_{FB} value was observed for Cu–HfO_2-Si capacitor, the corresponding work function (4.9 eV) still fell into the required window for p-channel devices. This result indicates that HfO_2 is electrically stable with Cu gate electrode. It is speculated that the stability is due to the considerably high density of HfO_2 (9.68 g/cm^3) [17], which is more than two times that of Al_2O_3 (3.97 g/cm^3). As a result, HfO_2 serves not only as a promising gate dielectric but also an excellent barrier against Cu diffusion, even though the density data quoted above are for bulk materials rather than thin films. Fig. 2 depicts V_{FB} shifts of Cu–HfO_2-Si, Al–HfO_2-Si, Cu–SiO_2–Si, and Al–SiO_2–Si capacitors as a function of temperature ranging from 100 to 200 °C after BTS test. The BTS stress was performed at +1 MV/cm for 1000 s. Clearly, V_{FB} shifts are negligible except for the Cu–SiO_2–Si capacitors. These results imply that HfO_2 can effectively block Cu ion drift at least up to 200 °C.

Fig. 3(a) shows the gate voltage variation as a function of time for the SiO_2 and HfO_2 capacitors with different gate electrodes, when subjected to CCS. The stressing current used was -1 mA/cm^2. The reason why we used such low current density for stressing is owing to the fact that the Q_{BD} is extremely hard to be monitored under the condition of -100 mA/cm^2 for the Cu–SiO_2–Si capacitors when Cu was incorporated. In the case of SiO_2 capacitors, a larger voltage shift observed in the Cu-gate capacitor, compared to the Al-gate counterpart, implies

the incorporation of Cu ions into SiO_2 dielectric during BTS test does result in higher electron trapping rate. By contrast, different metal gates (i.e., Al and Cu) only lead to indiscernible change in gate voltage shift during CCS for the HfO_2-based capacitors. These results suggest that the SiO_2 dielectric is more vulnerable than HfO_2 to Cu diffusion. As a result, the SiO_2 capacitors will breakdown more easily when Cu is employed as the gate electrode. Fig. 3(b) shows the Weibull distributions of the charge-to-breakdown (Q_{BD}) for all four capacitor configurations. Consistent with the results in Fig. 3(a), the value of 63% Q_{BD} for the Cu-gate SiO_2 capacitors is more than one order of magnitude lower than that for the Al-gate SiO_2 capacitors. This severe reliability degradation is the main reason why Cu is excluded from the conventional FEOL processes of silicon-based ULSI manufacturing. However, our finding strongly indicates that this is no longer an issue for the HfO_2 dielectric. From the cumulative Q_{BD} plots of HfO_2 capacitors with the Cu and Al gate electrodes, no significant difference is observed between the two groups, indicating that Cu diffusion has only negligible effects on the reliability of HfO_2-based capacitors. No degradation was observed even though 4-nm-thick HfO_2 was used in Cu–HfO_2–Si capacitor, as shown in Fig. 3(b) [18].

IV. Conclusions

AVD-deposited HfO_2 capacitors using Cu and Al as the gate electrode have been fabricated and investigated for the first time. The counterparts with thermally grown SiO_2 dielectric were also constructed for comparison. Our results clearly show that HfO_2 dielectric depicts superior resistance against Cu diffusion after BTS test, compared to SiO_2. Moreover, the presence of Cu metal in direct contact with HfO_2 has negligible impact on the reliability of the HfO_2 capacitor. The fact that HfO_2 can behave as a good barrier against Cu diffusion is attributed to its considerably high density. This finding is important as it suggests the feasibility of a Cu integration process from the p-channel gate electrode to BEOL interconnect, which will allow the use of the gate electrode as the first-level metal simultaneously, resulting in a simplified process.

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