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Valence-band tunneling induced low frequency noise in ultrathin oxide (15 Å) n -type metal-oxide-semiconductor field effect transistors

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Valence-band tunneling induced low frequency noise in ultrathin oxide (15 Å) *n*-type metal-oxide-semiconductor field effect transistors

J. W. Wu, J. W. You, H. C. Ma, and C. C. Cheng
Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan

C. S. Chang
Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

G. W. Huang
National Nano Device Laboratories, Hsinchu, Taiwan

T. Wang[a)]
Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan

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Low frequency flicker noise in *n*-type metal-oxide-semiconductor field effect transistors (*n*-MOSFETs) with 15 Å gate oxide is investigated. A noise generation mechanism resulting from valence band tunneling is proposed. In strong inversion condition, valence-band electron tunneling takes place and results in the splitting of electron and hole quasi-Fermi levels in the channel. The excess low frequency noise is attributed to electron and hole recombination at interface traps between the two quasi-Fermi levels. Random telegraph signal in a small area device is characterized to support our model. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1827930]

Drain current flicker noise in complementary metal-oxide-semiconductor (CMOS) transistors is an important design parameter for high performance radio frequency (rf) and mixed mode circuits. It will affect the signal-to-noise ratio in operational amplifiers, analog-to-digital, and digital-to-analog converters. In addition, phase noise of voltage-controlled oscillators up-converted from flicker noise is another concern in rf applications.[1]

The origin of low frequency noise in *n*-MOSFETs with relatively thick gate oxides has been extensively studied. A unified noise model based on oxide charge tunnel trapping and detrapping has been adopted.[2] As gate oxide thickness is scaled into direct tunneling domain, oxide trap density is much reduced. In addition, channel electrons would likely tunnel through an ultrathin gate oxide directly without being captured by oxide traps. However, the low frequency noise in ultrathin oxide CMOS devices still exhibits a noticeable level.[3] In this work, the low frequency noise in *n*-MOSFETs with a 15 Å gate oxide is investigated. The electron trapping/detrapping times are characterized from random telegraph signal (RTS) in small area *n*-MOSFETs. The normalized noise power spectral density (S_{id}/I_d^2) is also measured as a monitor of drain current noise, which is considered as a fair index because of the normalization to the drain current. Finally, a new generation/recombination noise mechanism as a result of valence band electron tunneling will be proposed to explain the observed noise behavior.

Figure 1 shows typical RTS patterns in a small area ($W/L=0.16\ \mu m/0.12\ \mu m$)15 Å gate oxide *n*-MOSFET at various gate voltages (V_g) from weak inversion to strong inversion. The drain bias in RTS measurement is 0.1 V to assure a uniform charge distribution in the channel. Due to a single charge trapping/detrapping, the RTS exhibits two levels. τ_H and τ_L in the figure denote the time in high current state (empty trap) and in low current state (occupied trap), respectively. The electron occupation factor of the trap (f_t) can be evaluated as $f_t=\tau_L/(\tau_L+\tau_H)$. Figure 2 shows f_t and corresponding S_{id}/I_d^2 (measured at $V_d=0.1$ V, $f=100$ Hz) vs V_g from weak inversion to strong inversion. In weak inversion region (i.e., $V_g<0.9$ V), τ_L and τ_H corresponds to electron emission and capture time through an interface trap (shown in Fig. 3). As V_g increases, τ_H decreases, τ_L increases and thus f_t increases because of increased channel electron population. As f_t increases to 1, RTS becomes undetectable (Fig. 1) since the trap is always occupied by an electron. Thus, S_{id}/I_d^2 has a peak around $f_t\sim0.5$ in Fig. 2. The observed V_g dependence of τ_L and τ_H in weak inversion is consistent with the findings for thicker gate oxides in other publication.[4] *However, we find that the RTS patterns in strong inversion* ($V_g>1$ V) *exhibit an opposite trend. The* V_g *dependence of* τ_H *and* τ_L *in strong inversion is opposite to that in weak inversion*. Moreover, significant substrate current is noticed for $V_g>1$ V (not shown here) because valence-band electron tunneling occurs and generated holes flow to the substrate.

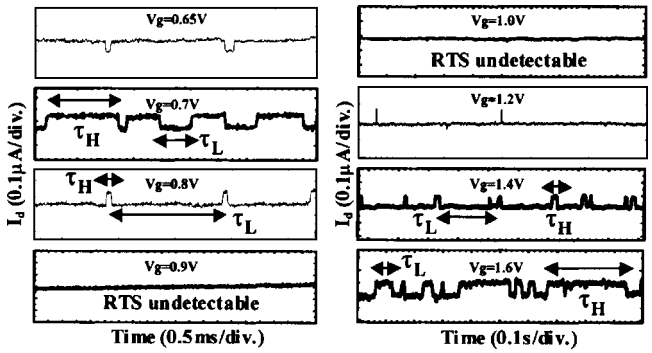

FIG. 1. Typical characteristics of two-level RTS (measured at $V_d=0.1$ V) at various gate voltages in a small area *n*-MOSFET ($W/L=0.16\ \mu m/0.12\ \mu m$, $t_{ox}=15$ Å). RTS is undetectable at $V_g=0.9$ V, and 1 V.

[a)]Electronic mail: twang@cc.nctu.edu.tw

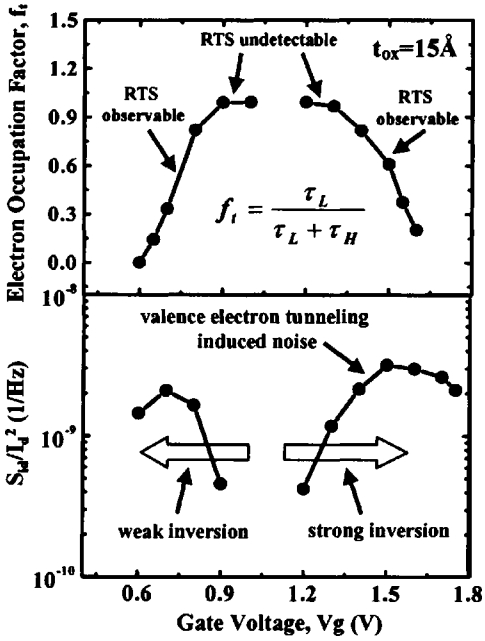

FIG. 2. Electron occupation factor (f_t) and normalized noise power spectral density (measured at V_d=0.1 V and f=100 Hz) vs gate voltage in a small area n-MOSFET (W/L=0.16 μm/0.12 μm, t_{ox}=15 Å). The second noise peak in strong inversion is due to valence-band electron tunneling.

In strong inversion regime, f_t declines with V_g from unity and the noise level shows another peak (Figs. 1 and 2). This means, at a larger V_g, although the energy level of the interface trap is deeper with respect to the electron Fermi level, the chance of the trap being occupied by an electron becomes smaller. The result is quite different from the equilibrium case that f_t should increase as the trap energy becomes more negative with respect to the Fermi level. The possible explanation is illustrated in Fig. 3. A larger V_g causes strong valence electron tunneling and leaves more holes behind in the channel. The nonequilibrium carrier distribution results in the splitting of electron and hole quasi-Fermi-levels. Because of the increased channel hole concentration at a larger V_g, the hole capture time (τ_L) is smaller, leading to a reduced f_t. The second peak of S_{id}/I_d^2 in strong inversion condition ($V_g > 1$ V) in Fig. 2 thus can be well understood.

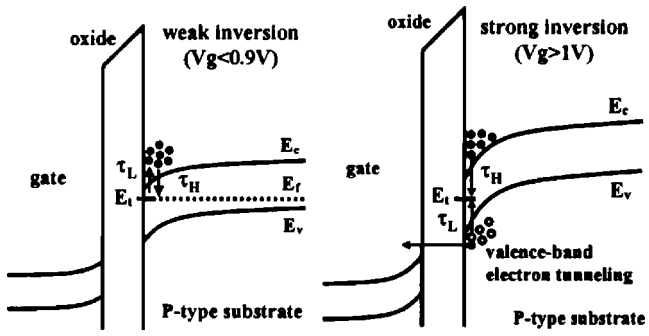

FIG. 3. RTS in weak inversion condition results from electron capture (τ_H) and electron emission (τ_L) at an interface trap; RTS in strong inversion condition results from electron capture (τ_H) and hole capture (τ_L) at an interface trap.

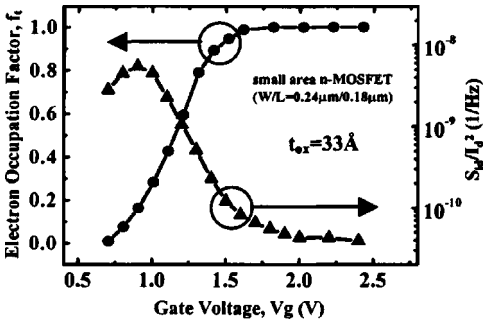

FIG. 4. Electron occupation factor (f_t) and normalized noise power spectral density (measured at V_d=0.1 V and f=100 Hz) vs gate voltage in a small area n-MOSFET (W/L=0.24 μm/0.18 μm) with t_{ox}=33 Å.

For a comparison, the f_t and S_{id}/I_d^2 vs V_g in a thicker gate oxide (33 Å) n-MOSFET are also characterized (Fig. 4). In contrast, the f_t stays at unity in strong inversion. Neither RTS nor the second noise peak is detected since valence-bane tunneling is negligible in such thick gate oxide devices.

In summary, an abnormal noise behavior in ultrathin oxide n-MOSFETs is observed in strong inversion condition. The traditional flicker noise model cannot account for the observed low-frequency noise. The analysis of RTS patterns reveals that the increased channel hole concentration and a Fermi-level splitting due to valence-band electron tunneling is responsible for the excess low-frequency noise.

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