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Influence of measuring environment on the electrical characteristics of pentacene-based thin film transistors

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Abstract

This work concerns the electrical properties and carrier transport behavior of polycrystalline pentacene-based thin film transistors (TFTs) in air and high-vacuum environments. The transistor in a high vacuum outperforms that in air. The dependence of the field-effect mobility on the gate voltage and the drain voltage is considered. A potential barrier model is applied to estimate the trap density of the pentacene transistor. The determined trap density at the grain boundaries of the pentacene film in air exceeds that in a high vacuum. These results show that the increased trap concentration at the grain boundaries in ambient air limits carrier transport.
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1. Introduction

Recently, organic semiconducting materials have been shown to include some of the most popular candidate materials for fabricating of thin film transistors (TFTs) and several electronic and optoelectronic devices. Pentacene, a fused-ring polycyclic aromatic hydrocarbon, is a very promising material for making organic TFTs. Its field-effect mobility of above 1.0 cm^2/V s and its on/off ratio of above 10^8 have been reported [1,2]. These values are similar to those obtained for amorphous silicon TFTs. However, the intrinsic transport mechanism of organic TFTs is not clear yet. Moreover, organic films are very sensitive to the environment and are unstable in air [3–6]. Necliudov et al. [7,8] examined the instabilities of the electrical characteristics and the 1/f noise behaviors of pentacene transistors. They reported that atmospheric moisture causes pentacene TFT degradation. Brown et al. [5] found that the organic transistors in air exhibit stronger hysteresis than those in a vacuum. Organic transistors in air have higher off currents because the oxygen dopant [5,9] and/or moisture interacts with organic films [10,11]. Recently, Zhu et al. [3] presented humidity sensors that use pentacene transistors. Clearly, contact with compounds in air affects the transport characteristics of organic films.

This work considers the electric properties of polycrystalline pentacene TFTs with gold top contacts in air and in a high vacuum. The field-effect mobilities at various gate voltages and drain voltages are examined. The potential barrier model is applied to investigate carrier transport in pentacene TFTs.

2. Experimental details

Fig. 1a schematically depicts a cross-section of a bottom-gate TFT device. First, a 1500 Å layer of Cr was deposited on a glass substrate by sputtering and patterned by photolithography to define the gate electrodes. A layer of silicon dioxide with a thickness 3000 Å was prepared by plasma-

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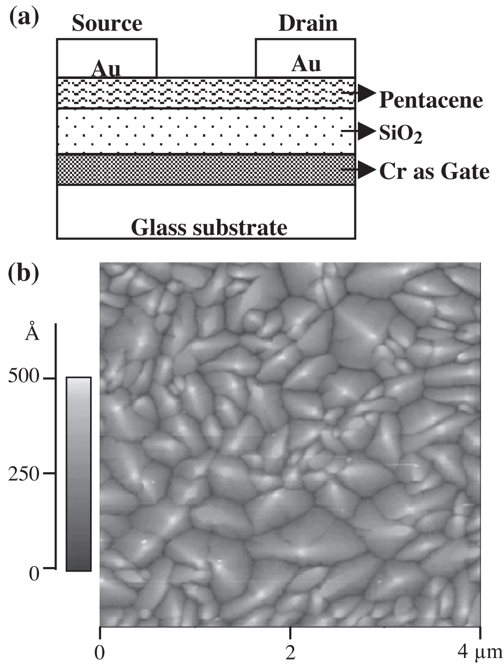

Fig. 1. (a) Schematic diagram of a bottom-gate pentacene transistor with gold top contact. (b) Atomic force microscope image of thermally deposited pentacene film on SiO_2 surface.

enhanced chemical vapor deposition (PECVD), using gases He, O_2 and tetraethylorthosilicate at 800 mTorr and 380 °C. This layer was the gate dielectric. Pentacene was purchased from FLUKA Chemical (97^{+}%) and used without any further purification. The pentacene film with a thickness of 1000 Å was deposited at a rate 0.5 of Å s^{-1} and the substrate was maintained at 70 °C. The pentacene active layer was thermally sublimated in a vacuum at a pressure of 10^{-5} Torr. The pentacene film morphology was characterized using a Seiko Instruments. SPA-500 scanning probe microscope with DF20 tip and operated in non-contact mode at 1 Hz scan rate. The gold source-drain electrodes were deposited on the surface of the pentacene film by shadow mask evaporation. The width and length of the defined channel were 1000 and 100 μm, respectively.

An HP 4155A Precision Semiconductor Parameter Analyzer was used to measure the electrical characteristics of the organic TFTs. The organic TFTs were first characterized in air and then in a vacuum chamber. The pentacene active layer was patterned using a shadow mask around the measured organic TFTs to minimize the drain current leakage.

3. Results and discussion

Fig. 1b shows 4 × 4 μm atomic force microscope of the topology of the pentacene film. The deposited film consisted of homogeneous grains with a mean diameter of around 0.5–1.5 μm.

The effects of the measuring conditions on the performance of the device in air and in a vacuum are investigated. Fig. 2 indicates the output characteristics of a pentacene transistor at various values of gate voltage (V_G). Measurements were made firstly in air and then in a vacuum at 10^{-6} Torr. The output current of a pentacene transistor in a high vacuum is clearly larger than that in air. The magnitude of the maximum saturation in a vacuum is nearly four times that in air.

At low drain voltage (V_{DS}), the drain current (I_D) increases linearly with V_{DS} (linear regime) and is approximately given by using the following equation:

$$I_D = \frac{W\mu C_i}{L}\left(V_G - V_T - \frac{1}{2}V_{DS}\right)V_{DS} \tag{1}$$

where W and L represent the width and length of the channel, respectively; C_i is the capacitance per unit area of the insulating layer; V_T is the threshold voltage, and μ is the field-effect mobility, which can be calculated in the linear regime from the transconductance, using,

$$g_m = \left.\frac{\partial I_D}{\partial I_V}\right|_{V_D=\text{const}} = \frac{WC_i}{L}\mu V_{DS} \tag{2}$$

For $-V_{DS} > -(V_G - V_T)$, I_D tends to saturate (in the saturation regime) because of the pinch-off of the accumulation layer, and is given by the equation,

$$I_{Dsat} = \frac{W\mu_{sat}C_i}{2L}(V_G - V_T)^2 \tag{3}$$

In the saturation regime, μ_{sat} can be calculated from the slope of the plot of $I_D^{1/2}$ against V_G.

Fig. 3 plots the $I_D - V_G$ and $I_D^{1/2} - V_G$ characteristics of a pentacene transistor at a V_{DS} of -100 V. In a high vacuum, the off-current of the pentacene transistor is lower and the

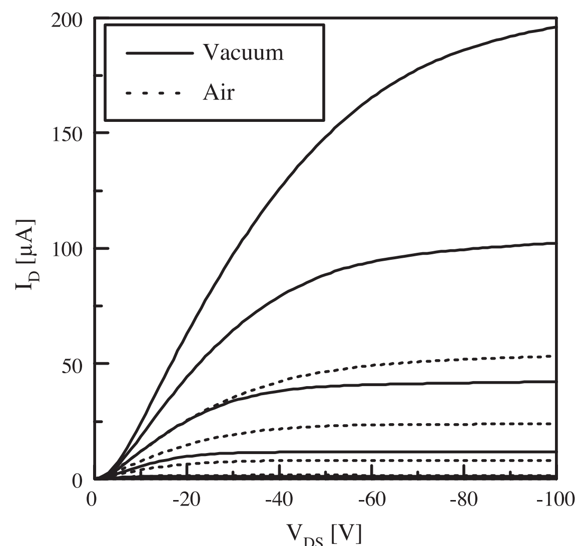

Fig. 2. $I_D - V_{DS}$ characteristics of a pentacene transistor measured in air and in a vacuum. The V_G was varied from -20 to -100 V with -20 V step.

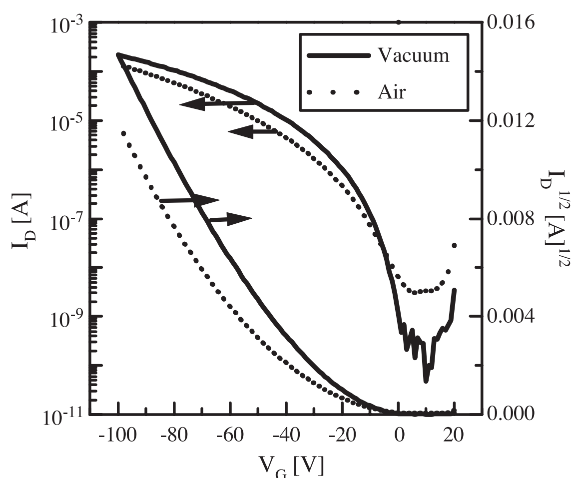

Fig. 3. Log (I_D) – V_G (left axis) and $(I_D)^{1/2}$ – V_G (right axis) characteristics of a pentacene transistor measured in air and in a vacuum with a V_{DS} of – 100 V.

on-current is higher than those in air. Eq. (3) yielded a field-effect mobility of the pentacene transistor as high as 0.43 cm^2/V s in a high vacuum. The modulated on/off ratio is 10^6; the threshold voltage is – 7.26 V and sub-threshold slope is 1.7 V/decade. However, the device in air performed poorly, exhibited a field-effect mobility of around 0.11 cm^2/V s, an on/off ratio of near 10^5, a threshold voltage of – 20 V and a sub-threshold slope of 5 V/decade. The high-vacuum environment markedly improves the performance of the pentacene transistor. Clearly, the charge transport characteristics of pentacene depend strongly on sensitive to the environmental conditions. The obtained results agree with those presented elsewhere [3–7].

In ambient air, the polar molecules H_2O, O_2, and CO_2 could easily diffuse into the organic film [3]. The channel conductivity of the film will be affected by dopants [12], as was verified in the off state. Subsidiary experiments were conducted in which the device was exposed to dry air to demonstrate that the H_2O molecules of air were responsible for the large leakage current. The leakage current in dry air was found to be close to that in a vacuum, indicating that moisture is the main cause of the leakage current. This finding may be explained by the fact that H_2O molecules interact with pentacene film to generate some dissociated species, resulting in ionic conductivity characteristics [10,11]. Apparently, the process is reversible and can be removed in a vacuum or dry air. However, the polar molecules may form extra traps at the grain boundaries, as well be considered below.

The dependence of mobility on gate voltage in various environments is also studied. The dependence of mobility on gate voltage has been reported for most organic TFTs [5,13–15]. Eqs. (1) and (3), applicable to the linear ($V_G - V_T < V_{DS}$) and saturation ($V_G - V_T > V_{DS}$) regimes, respectively, yield the field-effect mobility as a function of $-(V_G - V_T)$, which is plotted in Fig. 4. At a low drain voltage (– 2 V), the mobility of the device in a vacuum is slightly better than that in air. The fall in the mobility with increasing gate voltage is attributable the presence of a contact barrier of pentacene transistors with gold contacts [16–18]. Such a fall in the mobility with increasing V_G has also been observed in the oligothiophene transistor [13]. However, the mobility measured in air gradually approaches that measured in a vacuum as the negative gate voltage increases. At low gate voltage, most accumulated holes are probably trapped at the grain boundaries and the polar molecules, such as H_2O molecules in air interact with the trapped carriers [3], limiting the charge transport. At a high gate voltage, however, the concentration of accumulated holes is very high throughout the channel region and the traps at the grain boundaries are probably filled. Thus, the mobility of the transistor in air differs only slightly from that in a vacuum.

At large V_{DS} (– 20 and – 100 V), the mobility of the devices increases with V_G in a vacuum and in air. Such a quasilinear increase in the mobility with gate bias has also been observed for pentacene transistors [15,16], oligothiophene transistors [13], and, slightly differently, for α-Si transistors [19]. At a V_{DS} of – 20 V, the mobility of the transistor measured in a vacuum is high than that measured in air. One possible explanation is that the traps limit charge transport when the pentacene film is exposed to ambient air. However, at a V_{DS} of – 100 V, the mobility of device in air exhibits a marked increase at $-(V_G - V_T) < 40$ V, to a value near that of device in vacuo at $-(V_G - V_T) > 40$ V. At a higher drain voltage (– 100 V) and a higher gate voltage, the charge density in the channel is relatively uniform and the current increases linearly until it saturates. This phenomenon may explain the fact that the mobility of transistor

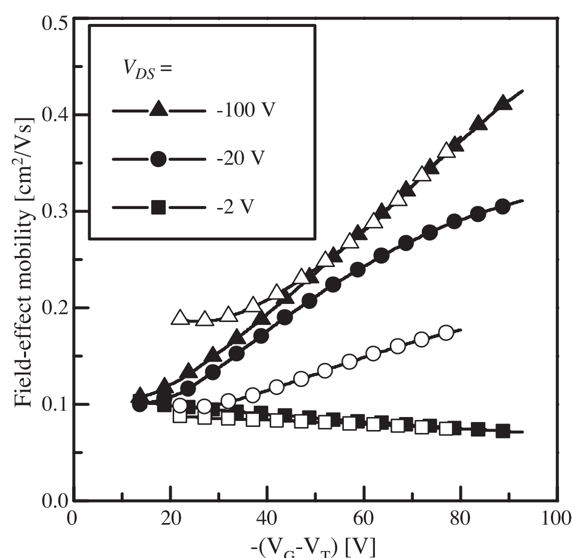

Fig. 4. Variation of the field-effect motilities of a pentacene transistor as a function of $-(V_G - V_T)$. Opened and closed symbols correspond to the data measured in air and in a vacuum, respectively.

in air is almost the same as that in a vacuum at high $-(V_G - V_T)$.

As the drain electric field is increased, the carriers are accelerated and their drift velocity increases. This work addresses the dependence of the mobility on the drain electric field in the pentacene transistor in air and in a vacuum. Eq. (1) yields the mobility as a function of V_{DS}. Fig. 5 plots field-effect mobility versus V_{DS} for various V_G in a vacuum. The mobility at low drain biases increases linearly with the drain bias and eventually saturates at large drain biases. In air, the device exhibits similar behavior but lower mobility at a given drain electric field. Fig. 6 plots the drift velocity, $v = \mu(E)E$, of the holes, as a function of the drain electric field at a V_G of -100 V. In a vacuum, the drift velocity increases linearly with the strength of the electrical field, similar to the carriers in silicon in a low electric field [20]. No high-field saturation of drift velocity was observed over the measurements range considered herein. The drift velocity of the transistor in air was less than that in a vacuum; the drift velocity-electric field characteristics deviate from linearity in a high drain electric field, as shown in Fig. 6. Clearly, the device in air exhibits charge trapping that reduces the drift velocity of the holes.

Thermally evaporated organic materials of interest herein—pentacene and oligothiophene—are polycrystalline and have large grains. Increasing the grain size has been demonstrated to improve the mobility of polycrystalline pentacene [21] and other polycrystalline organic materials [22]. The grain-boundary barrier model is extensively applied to understand carrier transport in such materials. The model assumes that carriers are transported at inter-polygrains by thermionic emission. The concept of grain-boundary potential barriers can be applied to polycrystalline silicon and polycrystalline CdSe [12]. The trap density, N_t, can be determined from a Levinson plot of $\ln[I_D/V_{DS}]$ against $1/V_G$. The Levinson model is based on the predicted transistor drain current in the linear regime, given by

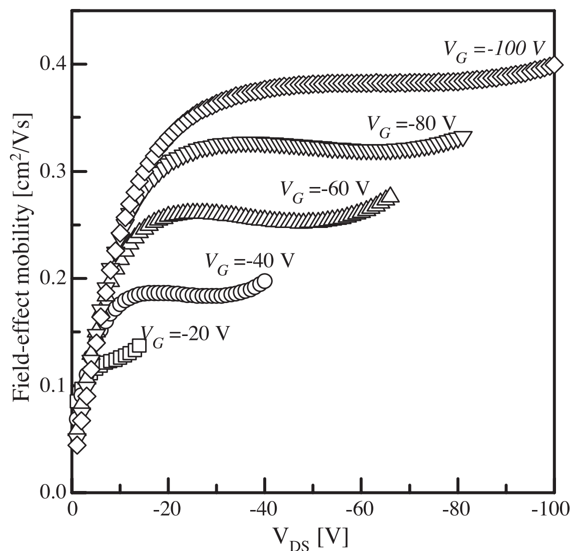

Fig. 5. Variation of the field-effect motilities of a pentacene transistor measured in a vacuum as a function of V_{DS} for $V_G = -100$, -80, -60, -40 and -20 V.

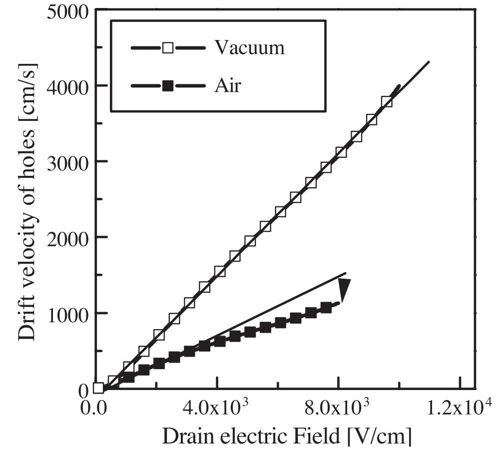

Fig. 6. The drain electric field dependence of the drift velocity of holes in pentacene transistor with a V_G of -100 V. The transistor was measured in air and then in a vacuum. The straight lines act as the reference.

$$I_D = \mu_0 V_{DS} C_i \left(\frac{W}{L}\right) V_G \exp\left(-\frac{E_B}{kT}\right) \tag{4}$$

$$\equiv \mu_0 V_{DS} C_i \left(\frac{W}{L}\right) V_G \exp\left(-\frac{s}{V_G}\right) \tag{5}$$

where E_B is the potential barrier height; μ_0 is the trap-free mobility, and the thermally activated mobility is given by

$$\mu = \mu_0 \exp\left(-\frac{E_B}{kT}\right) \equiv \mu_0 \exp\left(-\frac{s}{V_G}\right) \tag{6}$$

Screening causes E_B to fall as V_G increases [12]. Hence, N_t can be estimated from the slope, s, of the Levinson plot using the formula,

$$s = \frac{q^3 N_t^2 t}{8\varepsilon kT C_i} \tag{7}$$

where t represents the thickness of the semiconducting layer, and ε is the dielectric constant of the semiconductor. Additionally, E_B and μ_0 at constant V_G can be calculated using Eq. (6). Here, we take the ε of pentacene as 4 [23]. Fig. 7 presents a typical Levinson plot of $\ln[I_D/V_{DS}]$ against $1/V_G$ at V_{DS} of -20 V. From the slope of this plot $N_t \sim 6.11 \times 10^{11}$ and 4.89×10^{11} cm^{-2} are estimated for a pentacene transistor in air and in a vacuum, respectively. Then, Eq. (6) yields $E_B = 29.3$ meV and $\mu_0 = 0.56$ cm^2/V s for a device in air at $V_G = -100$ V. In a vacuum, the lower $E_B = 18.8$ meV and higher $\mu_0 = 0.65$ cm^2/V s were obtained at $V_G = -100$ V. The values of N_t and E_B are in good agreement with the values in the literature [6,24]. The value of μ_0 is proportional to the mean velocity of the holes [13]. The holes in a high vacuum have a higher drift velocity than in air. The results are

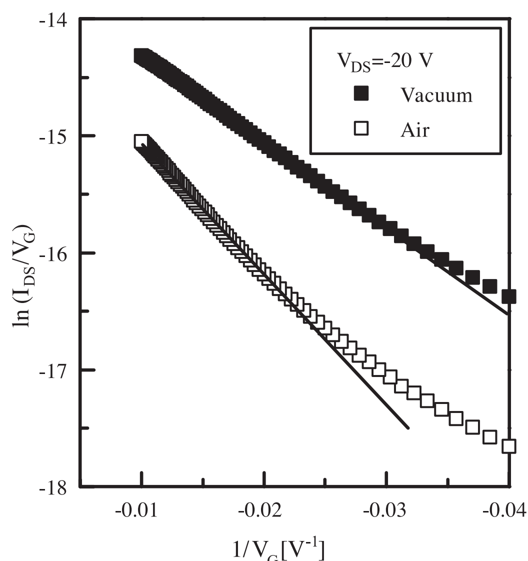

Fig. 7. Plot of $\ln(I_D/V_G)$ versus $(1/V_G)$ for a pentacene transistor measured in air and in a vacuum with a V_{DS} of -20 V.

consistent with those in Fig. 6. Clearly, the pentacene film in air has a higher trap density and higher potential barrier height than in a vacuum. The lower saturation current and higher threshold voltage of the device measured in air ambient showed that the extent of charge trapping is high [25], as this fact was supported by the trap concentration and barrier height obtained from the Levinson plot. The fall in the saturation current [3] and the strong hysteresis [11] of transistors based on pentacene semiconductors when exposed to the moisture in air have already been reported. Zhu et al. [3] also stated that H_2O molecules can easily diffuse into these gaps at the grain boundaries and interact with trapped carriers. In this work, devices were first exposed to air and then placed in a vacuum. They performed better when in a vacuum. Additionally, the saturation current quickly fell under gate bias stress when a device was in air ambient. Interestingly, the original saturation current was fully recovered when the device was pumped in a vacuum chamber for many hours, showing clearly that the air-induced degradation in device performance is a reversible.

4. Conclusion

The electrical properties of the polycrystalline pentacene transistor in air and in a vacuum were studied. The pentacene transistor measured in a high vacuum had greater field-effect mobility, a higher modulated on/off current ratio, a lower threshold voltage, and a better sub-threshold slope than that in air. The poor performance of the device in air follows from the more extensive trapping of carriers in air ambient and the consequent limiting of the charge transport of pentacene transistor. The grain-boundary potential barrier model estimates the potential barrier height and the trap density at the grain boundaries. The model is used to elucidate charge transport in a pentacene transistor under various atmospheric conditions. Moreover, the proposed model offers a satisfactory explanation of the improved performance of pentacene transistors in a high vacuum and facilitates an understanding of the difference between air and vacuum environments in this regard.

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