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Effects of annealing temperature on electrical resistance of bonded *n*-GaAs wafers

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The electrical characteristics and microstructures of *n*-type (100) GaAs bonded interfaces were systematically investigated. Experimental results indicated that GaAs did not bond directly to itself, but via an amorphous oxide layer at 400 °C. When temperatures increased above 400 °C, the oxide bonded area declined and finally disappeared. Electrical resistance decreased with bonding temperature. However, the resistance increased with temperatures exceeding 850 °C. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1823592]

The bonding of III–V semiconductors was developed for two-layer optoelectronic devices.[1–3] Bonding processes are normally performed at elevated temperatures to increase bonding strength and bonded area.[4,5] The most significant problems encountered are excess electrical resistance caused by interfacial defects, bulk defects, and surface defects.[5] Interfacial defects were found to comprise mostly voids and inclusions caused by natural topographical irregularities, surface contamination (including native oxide), and solvent residues or trapped gases between the wafers. The causes of bulk and surface defects are more complex, and the extensive literature in the field reveals that these include dislocations, impurities, vacancies, interstitials, precipitates, and antisite defects. Arsenic antisite defects (arsenic on gallium sites As_{Ga}) and clusters of other defects are generally known as EL2 (a deep donor in GaAs);[6] the concentration of these defects increases with arsenic concentration in the crystal.[7] When wafers were bonded at elevated temperatures, the evaporation rate of arsenic from the surface exceeded that of gallium (about 2.5 times at 827 °C),[8] which decreased the arsenic (and thus the EL2) concentration. If the wafer was semi-insulating, the evaporation of arsenic converted the outer surface from semi-insulating to *p*-type. This reduction of the EL2 (donor) concentration was a major factor that was responsible for the change in the electrical resistance of the GaAs single wafers.[5] This work investigates the origin of electrical resistances by systematically studying the bonding mechanisms, and by performing extensive materials and electrical characterization.

Si doped *n*-type (100) GaAs wafers were used. Wafers were diced into 1×1 cm^2 samples using a diamond saw, and solvent-cleaned in a clean room. Cleaned wafers were pressed against each other in a differential thermal expansion fixture[9] with careful edge-to-edge alignment, such that the crystallographic directions in the plane of the bonded interface were arranged as in a single-crystal zinc-blende lattice. Then, the fixture was loaded into a furnace and was annealed at temperatures from 400 to 850 °C for 2 h in argon ambient.

Two GaAs structures were used in this study—(1) single GaAs wafers and (2) two-layer bonded stacks. The single GaAs wafers were processed under identical thermal conditions and were used to separate the bulk and surface effects from the interfacial effects.

Figure 1 plots current versus voltage (I–V) for single GaAs wafers heat-treated at temperatures between 400 and 850 °C. Processing at temperatures that exceed 700 °C increase the electrical resistances of the heat-treated GaAs above those of the unprocessed GaAs wafers. No interface is involved in single wafer experiments, so the resistances must be increased by bulk and surface defects. Hall effect measurements revealed that the carrier concentration decreased from 4.32×10^{18} to 3.02×10^{16} cm^{-3} as the processing temperature increased from room temperature to 850 °C. When 20 μm was polished away, the carrier concentration increased to 5.95×10^{17} cm^{-3}. The results indicated that changes of carrier concentration were caused mainly by arsenic depletion, as mentioned previously.

In addition to the above-described mechanism, other factors that may affect electrical resistance include the following. (1) The diffusion of As away from the EL2 center to

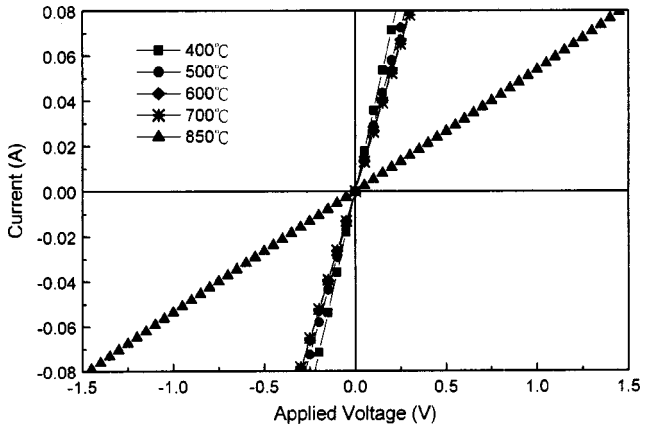

FIG. 1. Current–voltage characteristic of single *n*-type (100) GaAs wafers processed at temperatures from 400 to 850 °C for 2 h in argon ambient.

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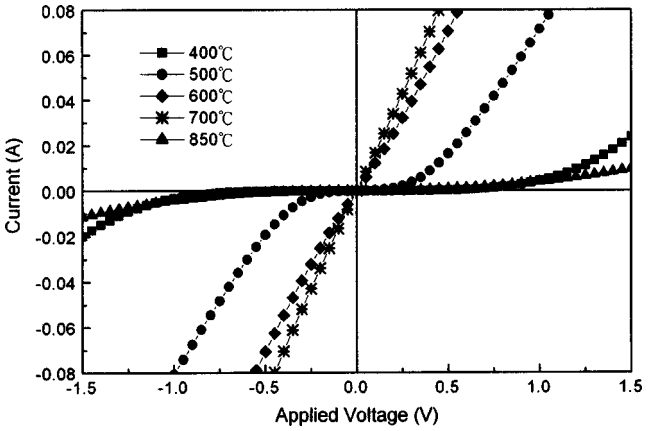

FIG. 2. Current–voltage characteristic of bonded two-layer (100) wafers processed at temperatures from 400 to 850 °C for 2 h in argon ambient.

form large precipitates (leading to *p*-type conversion); (2) the diffusion of impurities inwards from the wafer surfaces (to an extent that increases with temperature and time); and (3) the plastic deformation of GaAs under a fixed compressive load (to an extent that increases with temperature[10–12]), producing a greater density of dislocations. These factors may explain why some degradation in electrical resistance persists even after the As-depleted surfaces (surface defects) were polished away.

Figure 2 plots *I–V* for GaAs wafers bonded at temperatures between 400 and 850 °C. GaAs does not bond at temperatures below 400 °C and the resistance of GaAs bonded at 400 °C was very large. A more or less continuous decrease in resistance was expected with increasing bonding temperature, since mass transport (diffusion, vapor transport, etc.) and reaction rate increase with temperature. However, at temperatures over 850 °C, the increase of the resistance was due mainly to the reduction of the surface carrier concentration caused by incongruent evaporation. Surface polishing reduced the electrical resistance of the bonded wafers; however, the resistance did not return to its original value.

Transmission electron microscopy (TEM) analysis of these specimens indicated that various bonding mechanisms were involved. At 400 °C, GaAs does not bond directly to itself, but via an amorphous oxide layer, as shown in Fig. 3. When the bonding temperature increased, the amorphous oxide layer became discontinuous and local GaAs bonded areas were formed, as shown in Fig. 4. The GaAs bonded areas increased with the bonding temperature. Finally, when processed at 850 °C, most GaAs wafers were found to be bonded directly to themselves. As presented in Fig. 5, no oxide layer was found between GaAs even though a native oxide layer was likely to have formed on the wafer surfaces before they were loaded into the furnace.

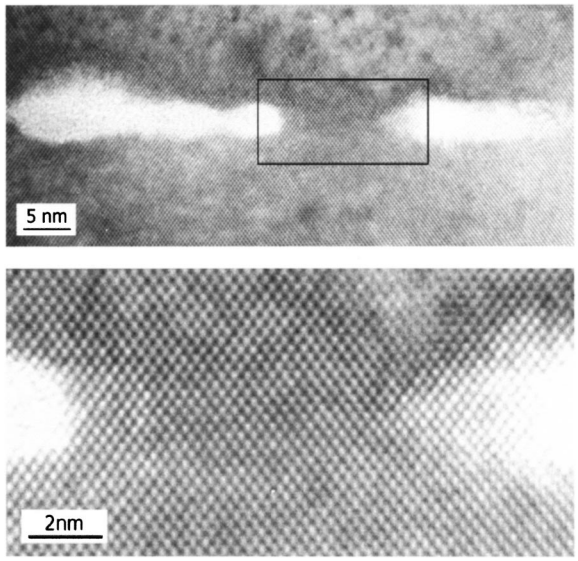

FIG. 4. Cross-sectional high resolution TEM image of a (100) GaAs interface bonded at 500 °C, showing a locally GaAs bonded interface combined with an array of amorphous oxide regions.

The above-mentioned observations of the amorphous oxide layer (oxygen distribution) around the interface were verified by the following methods: energy dispersive x-ray spectroscopy line-scan and high-angle annular-dark field. The oxygen content was found to increase as the distance from the interface decreased.[13]

In related works, Shi *et al.*[14] bonded GaAs wafers at 400 °C for 1 h and then annealed them at 600 °C for various periods. They found that GaAs could be successfully bonded at 400 °C because of the presence of continuous oxide at the interface. During annealing at 600 °C, a drastic change in interface morphology caused by atomic rearrangement led to the formation of a locally GaAs-bonded interface combined with an array of bubblelike amorphous oxide regions. Shi *et al.* believed that the oxide layer became discontinuous because the atomic rearrangement reduced the GaAs/oxide interface energy. However, they made no attempt to bond wafers at temperatures higher than 600 °C.

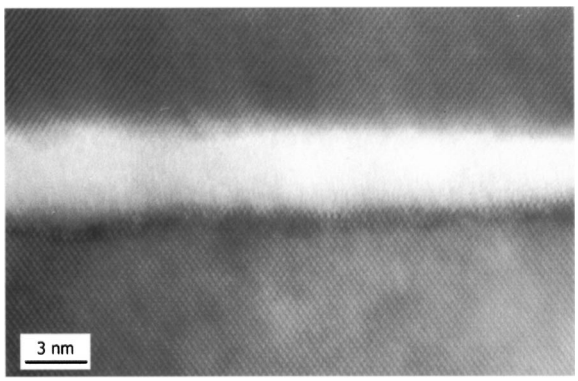

FIG. 3. Cross-sectional high resolution TEM image of a (100) GaAs interface bonded at 400 °C, showing an oxide layer at the interface.

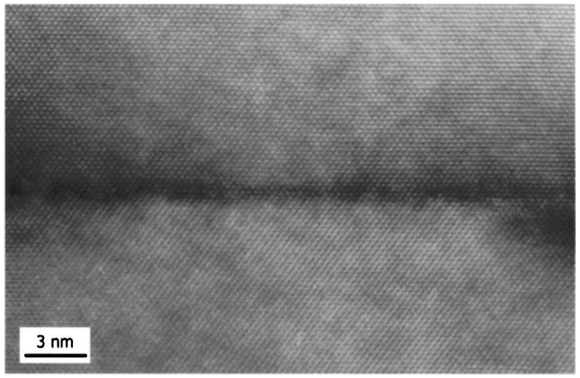

FIG. 5. Cross-sectional high resolution TEM image of a (100) GaAs interface bonded at 800 °C, showing intimate contact between GaAs with no intervening oxide layer.

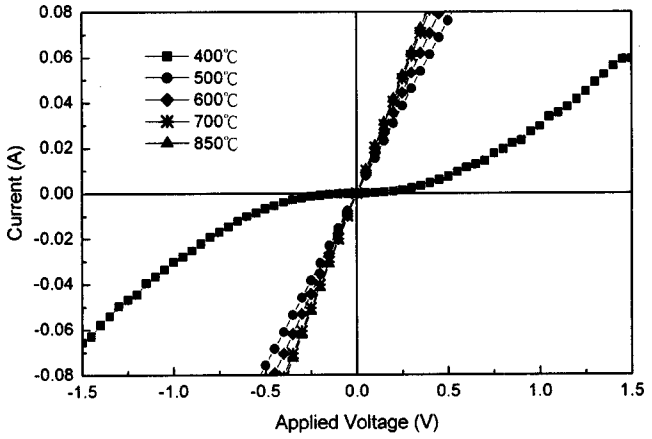

FIG. 6. Current–voltage characteristic of bonded two-layer *p*-type (100) GaAs wafers.

In our work, as the temperature increased above 400 °C, the oxide-bonded areas gradually decreased until they finally disappeared. We posit that this increase of the area of the GaAs bonded interface was due mainly to the indiffusion of oxide into the GaAs wafers, which can be modeled by a one-dimensional diffusion equation based on a reference point at the center of the bonded interface. The diffusion constant of oxygen into GaAs is given by

$$D = 2 \times 10^{-3} \exp(-1.1\ eV/kT)\ \mathrm{cm}^2\ \mathrm{s}^{-1},$$

where T is the bonding temperature and k is the gas constant.[15] When $T=850$ °C, the diffusivity of oxygen in GaAs, D, equals 2.55×10^{-8} $\mathrm{cm}^2\ \mathrm{s}^{-1}$. A typical 2 h diffusion process can affect the oxygen concentration within $\approx\sqrt{Dt}$ ≈ 135 μm of the bonded interface.

The primary function of the oxygen in GaAs was to reduce the donor (Si) concentration through the formation of complexes between oxygen and donors, thereby reducing the carrier concentration.[16–18] The reduction of the carrier concentration at the bonded interface was confirmed using spreading resistance probe (SRP), indicating that the SRP signal (resistance) at the interface was about double that inside the GaAs bulk. In other words, the indiffusion of oxygen into GaAs negatively affects the carrier concentration, indicating that this indiffusion may explain why the some degradation in electrical resistance was detected even after the As-depleted surfaces (surface defects) had been polished away.

For comparison, cleaned *p*-type GaAs samples were pressed against each other and annealed under identical thermal conditions. The resistance was found to fall as the bonding temperature increased, as shown in Fig. 6. These results differed completely from those for *n*-type GaAs. In other words, the indiffusion of oxygen was the major cause of increases of resistance at the *n*-GaAs bonded interface.

In summary, this study examined the relationship between bonding temperatures and electrical characteristics of *n*-type (100) GaAs bonded wafers. Experimental results indicate that GaAs was successfully bonded at 400 °C by continuous oxide at the interface. The GaAs bonded areas increased with the bonding temperature. Finally, when processed at 850 °C, most GaAs wafers were found to be bonded directly to themselves. GaAs bonded areas increased with bonding temperature, so electrical resistance decreased with bonding temperature. However, the resistance increased with temperature over 850 °C due to the reduction of the surface carrier concentration and the indiffusion of oxygen into the GaAs bonded interface.

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